

MOSFET

600V CoolMOS™ C7 Power Device

CoolMOS™ C7 is a revolutionary technology for high voltage power MOSFETs, designed according to the superjunction (SJ) principle and pioneered by Infineon Technologies.

600V CoolMOS™ C7 series combines the experience of the leading SJ MOSFET supplier with high class innovation.

The 600V C7 is the first technology ever with $R_{DS(on)} \cdot A$ below $10\text{Ohm} \cdot \text{mm}^2$.

Features

- Suitable for hard and soft switching (PFC and high performance LLC)
- Increased MOSFET dv/dt ruggedness to 120V/ns
- Increased efficiency due to best in class FOM $R_{DS(on)} \cdot E_{oss}$ and $R_{DS(on)} \cdot Q_g$
- Best in class $R_{DS(on)}$ /package

Benefits

- Increased economies of scale by use in PFC and PWM topologies in the application
- Higher dv/dt limit enables faster switching leading to higher efficiency
- Enabling higher system efficiency by lower switching losses
- Increased power density solutions due to smaller packages
- Suitable for applications such as server, telecom and solar
- Higher switching frequencies possible without loss in efficiency due to low E_{oss} and Q_g

Potential applications

PFC stages and PWM stages (TTF, LLC) for high power/performance SMPS e.g. Computing, Server, Telecom, UPS and Solar.

Product validation

Fully qualified according to JEDEC for Industrial Applications

Please note: For MOSFET paralleling the use of ferrite beads on the gate or separate totem poles is generally recommended.

Table 1 Key Performance Parameters

Parameter	Value	Unit
$V_{DS} @ T_{j,max}$	650	V
$R_{DS(on),max}$	99	mΩ
$Q_{g,typ}$	42	nC
$I_{D,pulse}$	83	A
$I_{D,continuous} @ T_j < 150^\circ\text{C}$	36	A
$E_{oss}@400\text{V}$	4.95	μJ
Body diode di/dt	360	A/μs

Type / Ordering Code	Package	Marking	Related Links
IPA60R099C7	PG-TO 220 FullPAK	60C7099	see Appendix A

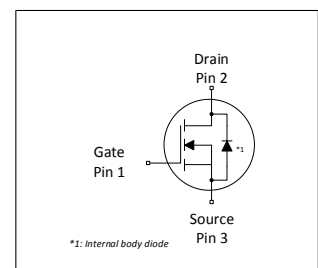


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1 Maximum ratings

at $T_j = 25^\circ\text{C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D	-	-	12 8	A	$T_C=25^\circ\text{C}$ $T_C=100^\circ\text{C}$
Pulsed drain current ²⁾	$I_{D,pulse}$	-	-	83	A	$T_C=25^\circ\text{C}$
Avalanche energy, single pulse	E_{AS}	-	-	97	mJ	$I_D=5\text{A}$; $V_{DD}=50\text{V}$; see table 10
Avalanche energy, repetitive	E_{AR}	-	-	0.49	mJ	$I_D=5\text{A}$; $V_{DD}=50\text{V}$; see table 10
Avalanche current, single pulse	I_{AS}	-	-	5.0	A	-
MOSFET dv/dt ruggedness	dv/dt	-	-	120	V/ns	$V_{DS}=0\dots400\text{V}$
Gate source voltage (static)	V_{GS}	-20	-	20	V	static;
Gate source voltage (dynamic)	V_{GS}	-30	-	30	V	AC ($f>1\text{ Hz}$)
Power dissipation	P_{tot}	-	-	33	W	$T_C=25^\circ\text{C}$
Storage temperature	T_{stg}	-55	-	150	$^\circ\text{C}$	-
Operating junction temperature	T_j	-55	-	150	$^\circ\text{C}$	-
Mounting torque	-	-	-	50	Ncm	M2.5 screws
Continuous diode forward current	I_S	-	-	12	A	$T_C=25^\circ\text{C}$
Diode pulse current ²⁾	$I_{S,pulse}$	-	-	83	A	$T_C=25^\circ\text{C}$
Reverse diode dv/dt ³⁾	dv/dt	-	-	20	V/ns	$V_{DS}=0\dots400\text{V}$, $I_{SD}\leq 7.7\text{A}$, $T_j=25^\circ\text{C}$ see table 8
Maximum diode commutation speed	di/dt	-	-	360	A/ μs	$V_{DS}=0\dots400\text{V}$, $I_{SD}\leq 7.7\text{A}$, $T_j=25^\circ\text{C}$ see table 8
Insulation withstand voltage	V_{ISO}	-	-	2500	V	V_{rms} , $T_C=25^\circ\text{C}$, $t=1\text{min}$

¹⁾ Limited by $T_{j,max}$.

²⁾ Pulse width t_p limited by $T_{j,max}$

³⁾ Identical low side and high side switch

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	3.79	°C/W	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	80	°C/W	leaded
Thermal resistance, junction - ambient for SMD version	R_{thJA}	-	-	-	°C/W	n.a.
Soldering temperature, wavesoldering only allowed at leads	T_{sold}	-	-	260	°C	1.6mm (0.063 in.) from case for 10s

3 Electrical characteristics

at $T_j=25^\circ\text{C}$, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	600	-	-	V	$V_{GS}=0\text{V}$, $I_D=1\text{mA}$
Gate threshold voltage	$V_{(GS)th}$	3	3.5	4	V	$V_{DS}=V_{GS}$, $I_D=0.49\text{mA}$
Zero gate voltage drain current	I_{DSS}	-	-	1	μA	$V_{DS}=600$, $V_{GS}=0\text{V}$, $T_j=25^\circ\text{C}$ $V_{DS}=600$, $V_{GS}=0\text{V}$, $T_j=150^\circ\text{C}$
Gate-source leakage current	I_{GSS}	-	-	100	nA	$V_{GS}=20\text{V}$, $V_{DS}=0\text{V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	0.085 0.190	0.099 -	Ω	$V_{GS}=10\text{V}$, $I_D=9.7\text{A}$, $T_j=25^\circ\text{C}$ $V_{GS}=10\text{V}$, $I_D=9.7\text{A}$, $T_j=150^\circ\text{C}$
Gate resistance	R_G	-	0.82	-	Ω	$f=1\text{MHz}$, open drain

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	1819	-	pF	$V_{GS}=0\text{V}$, $V_{DS}=400\text{V}$, $f=250\text{kHz}$
Output capacitance	C_{oss}	-	33	-	pF	$V_{GS}=0\text{V}$, $V_{DS}=400\text{V}$, $f=250\text{kHz}$
Effective output capacitance, energy related ¹⁾	$C_{o(er)}$	-	63	-	pF	$V_{GS}=0\text{V}$, $V_{DS}=0\dots400\text{V}$
Effective output capacitance, time related ²⁾	$C_{o(tr)}$	-	641	-	pF	$I_D=\text{constant}$, $V_{GS}=0\text{V}$, $V_{DS}=0\dots400\text{V}$
Turn-on delay time	$t_{d(on)}$	-	11.8	-	ns	$V_{DD}=400\text{V}$, $V_{GS}=13\text{V}$, $I_D=9.7\text{A}$, $R_G=5.3\Omega$; see table 9
Rise time	t_r	-	8	-	ns	$V_{DD}=400\text{V}$, $V_{GS}=13\text{V}$, $I_D=9.7\text{A}$, $R_G=5.3\Omega$; see table 9
Turn-off delay time	$t_{d(off)}$	-	54	-	ns	$V_{DD}=400\text{V}$, $V_{GS}=13\text{V}$, $I_D=9.7\text{A}$, $R_G=5.3\Omega$; see table 9
Fall time	t_f	-	4.5	-	ns	$V_{DD}=400\text{V}$, $V_{GS}=13\text{V}$, $I_D=9.7\text{A}$, $R_G=5.3\Omega$; see table 9

Table 6 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{GS}	-	9	-	nC	$V_{DD}=400\text{V}$, $I_D=9.7\text{A}$, $V_{GS}=0$ to 10V
Gate to drain charge	Q_{gd}	-	14	-	nC	$V_{DD}=400\text{V}$, $I_D=9.7\text{A}$, $V_{GS}=0$ to 10V
Gate charge total	Q_g	-	42	-	nC	$V_{DD}=400\text{V}$, $I_D=9.7\text{A}$, $V_{GS}=0$ to 10V
Gate plateau voltage	V_{plateau}	-	5.0	-	V	$V_{DD}=400\text{V}$, $I_D=9.7\text{A}$, $V_{GS}=0$ to 10V

¹⁾ $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400V

²⁾ $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 400V

Table 7 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}	-	0.9	-	V	$V_{GS}=0V, I_F=9.7A, T_j=25^\circ C$
Reverse recovery time	t_{rr}	-	350	-	ns	$V_R=400V, I_F=9.7A, di_F/dt=100A/\mu s$; see table 8
Reverse recovery charge	Q_{rr}	-	4.4	-	μC	$V_R=400V, I_F=9.7A, di_F/dt=100A/\mu s$; see table 8
Peak reverse recovery current	I_{rrm}	-	27	-	A	$V_R=400V, I_F=9.7A, di_F/dt=100A/\mu s$; see table 8

4 Electrical characteristics diagrams

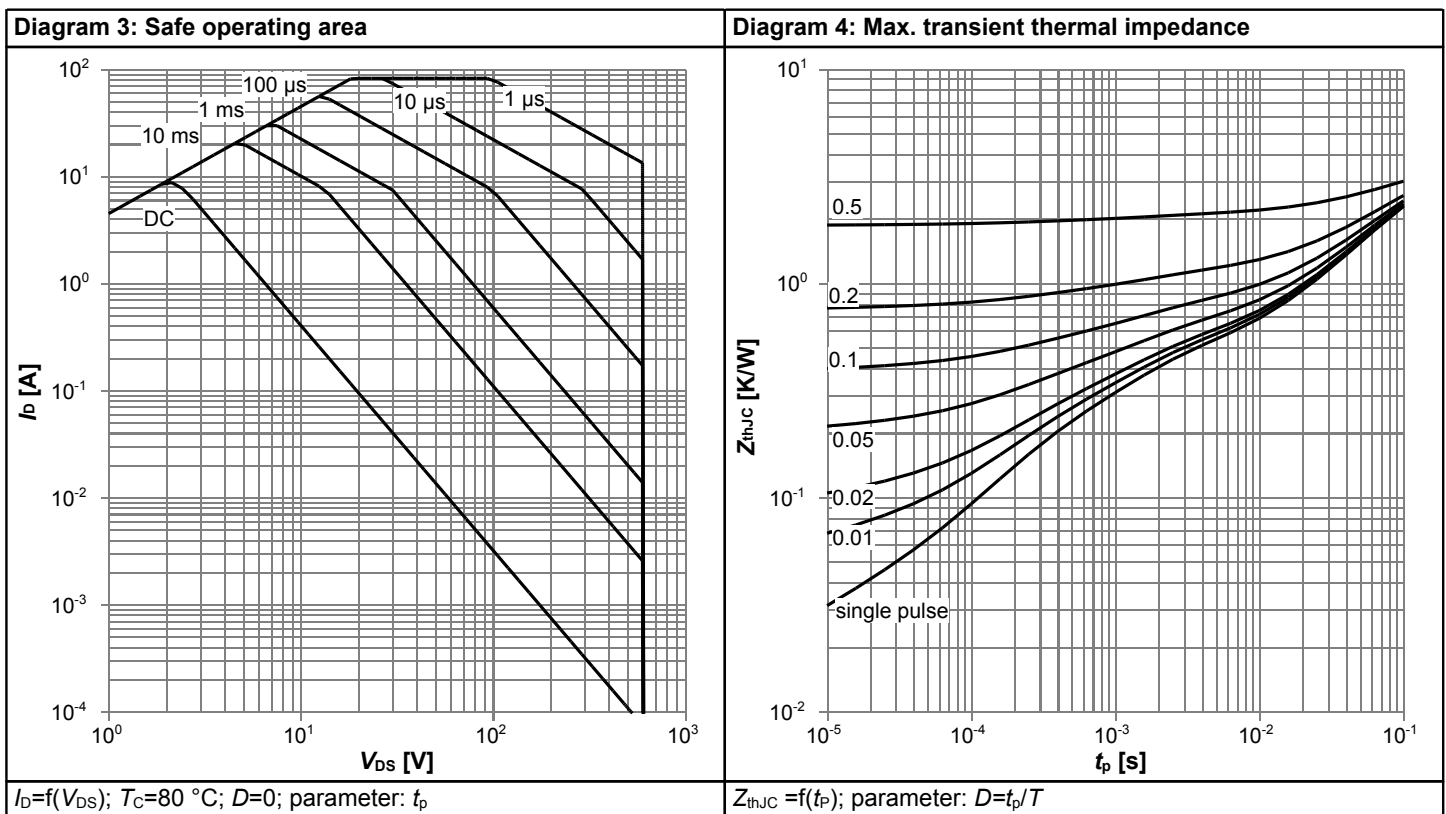
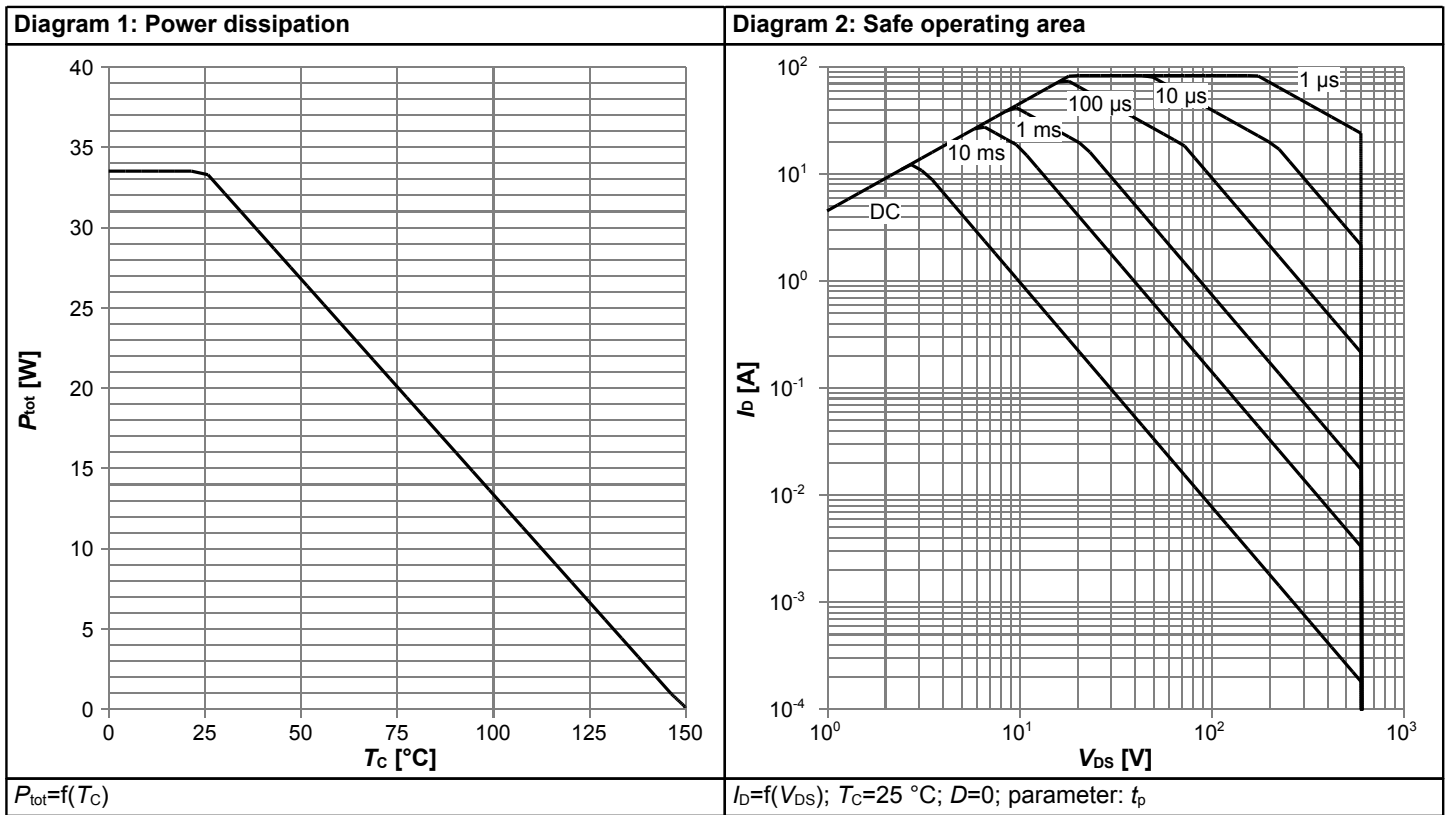
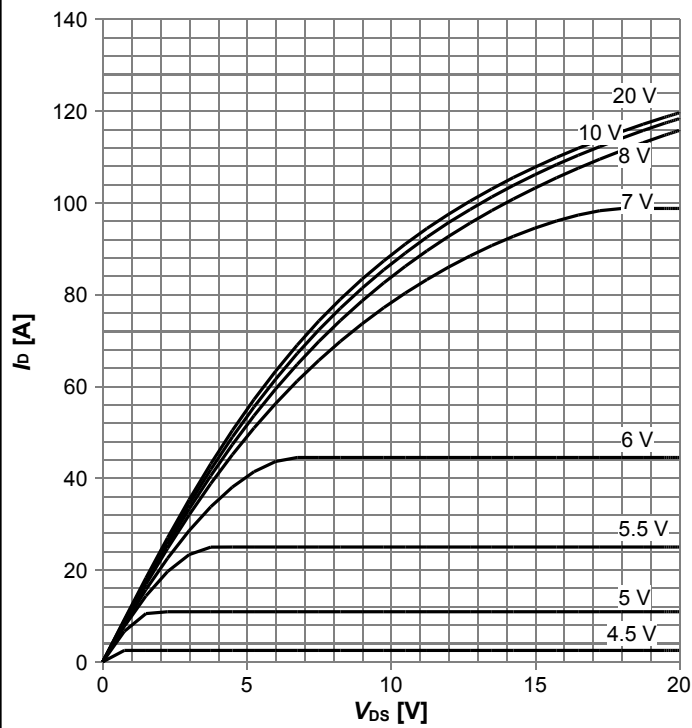
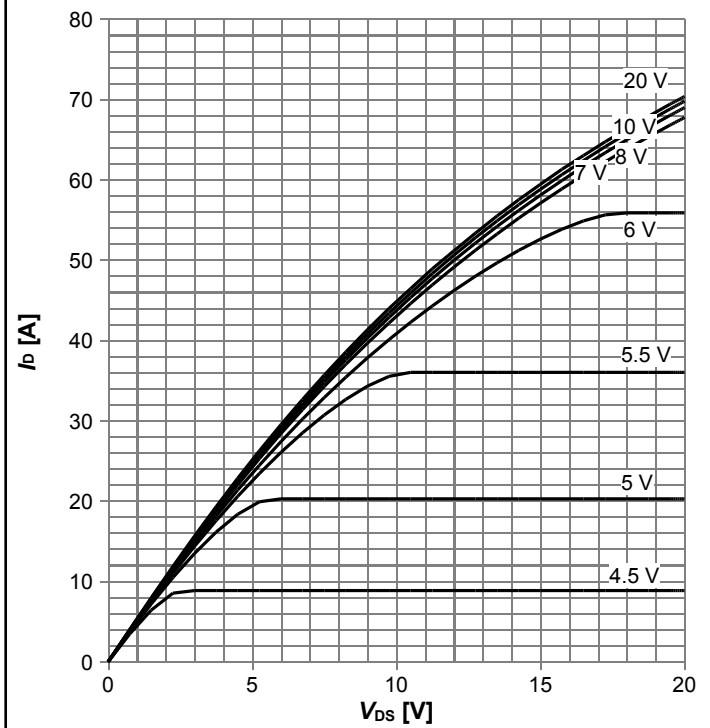


Diagram 5: Typ. output characteristics



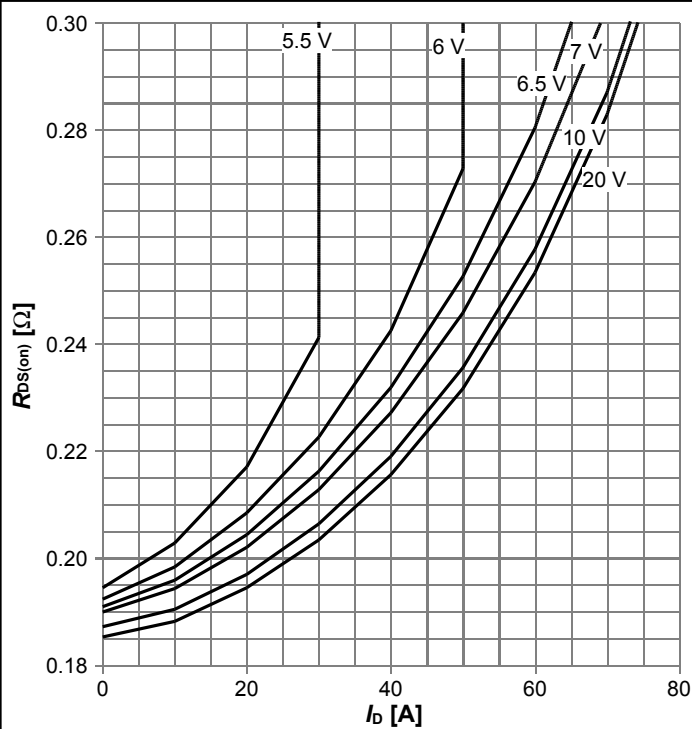
$I_D = f(V_{DS})$; $T_j = 25^\circ\text{C}$; parameter: V_{GS}

Diagram 6: Typ. output characteristics



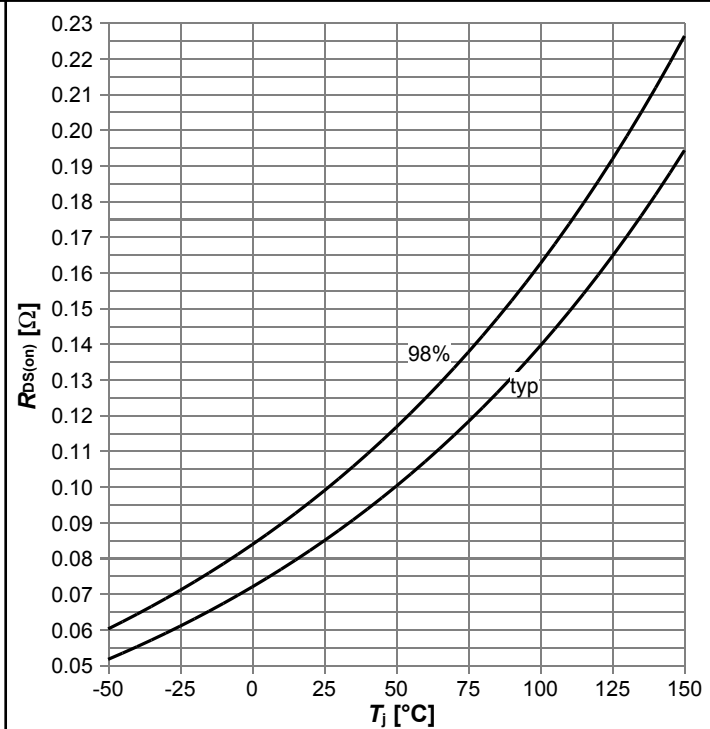
$I_D = f(V_{DS})$; $T_j = 125^\circ\text{C}$; parameter: V_{GS}

Diagram 7: Typ. drain-source on-state resistance



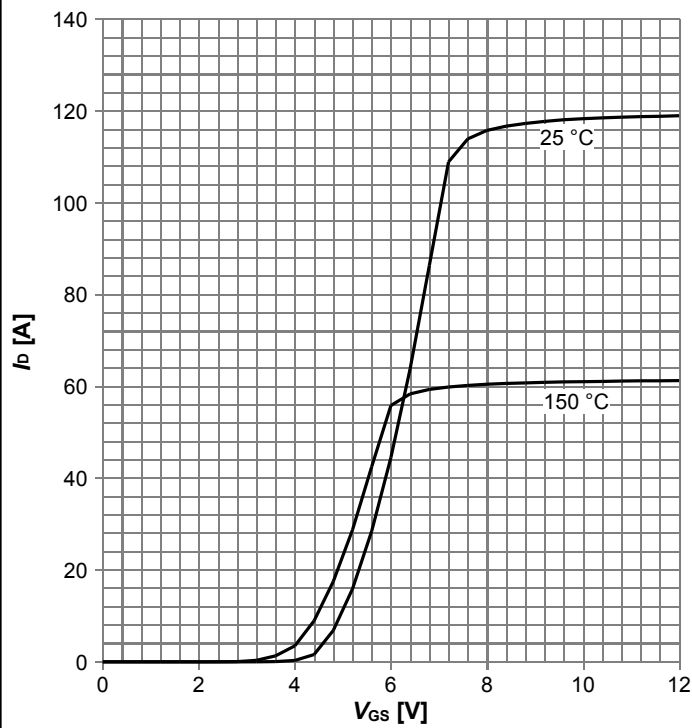
$R_{DS(on)} = f(I_D)$; $T_j = 125^\circ\text{C}$; parameter: V_{GS}

Diagram 8: Drain-source on-state resistance



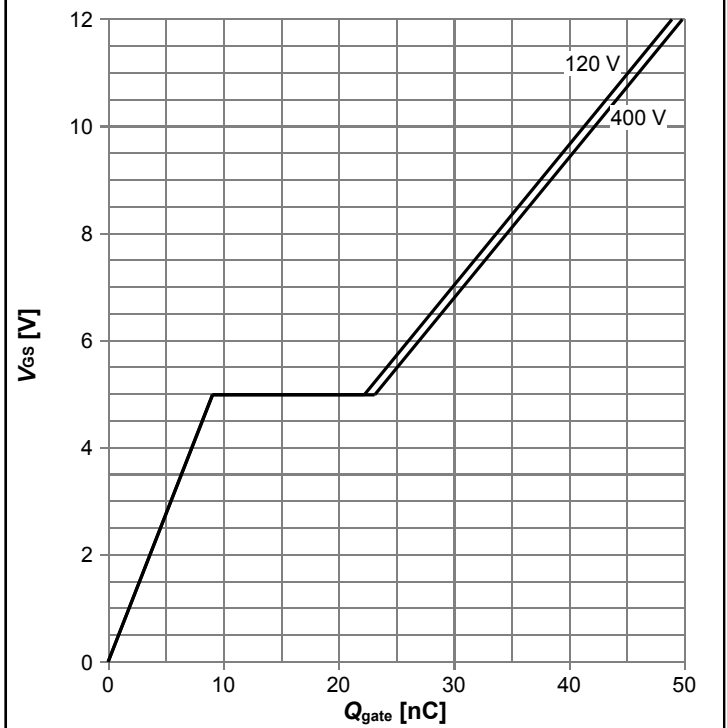
$R_{DS(on)} = f(T_j)$; $I_D = 9.7\text{ A}$; $V_{GS} = 10\text{ V}$

Diagram 9: Typ. transfer characteristics



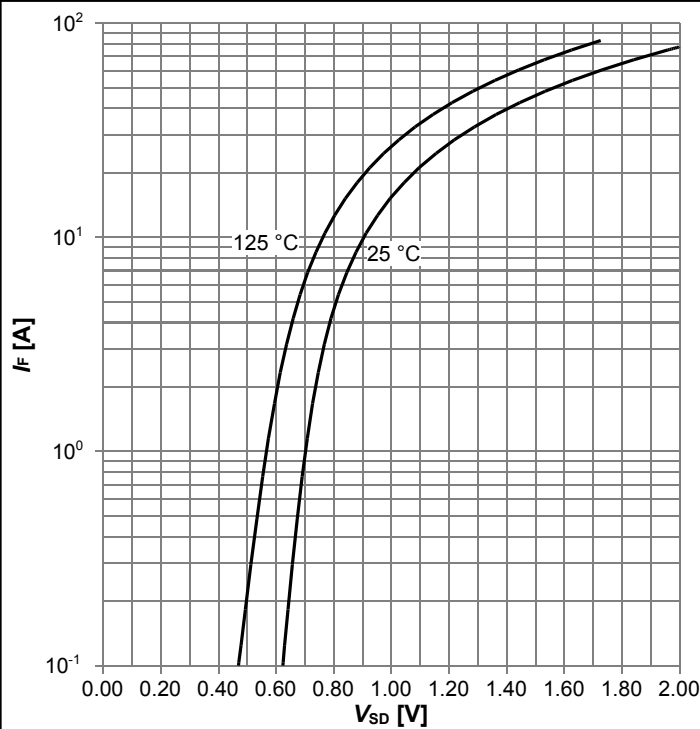
$I_D = f(V_{GS})$; $V_{DS} = 20V$; parameter: T_j

Diagram 10: Typ. gate charge



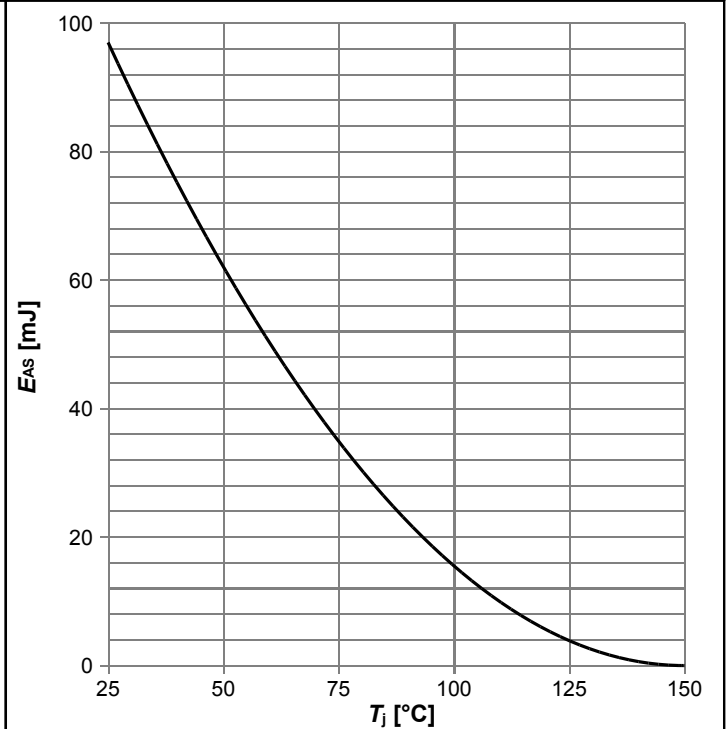
$V_{GS} = f(Q_{gate})$; $I_D = 9.7 A$ pulsed; parameter: V_{DD}

Diagram 11: Forward characteristics of reverse diode



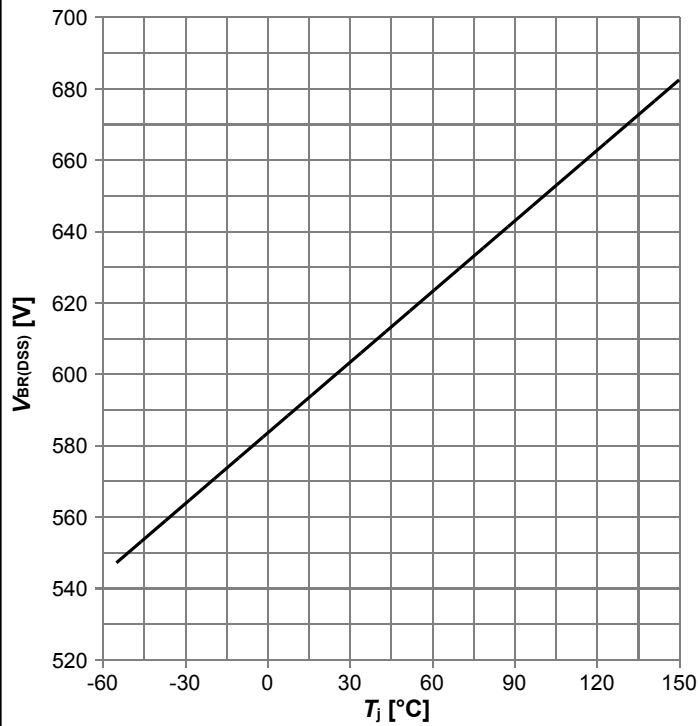
$I_F = f(V_{SD})$; parameter: T_j

Diagram 12: Avalanche energy



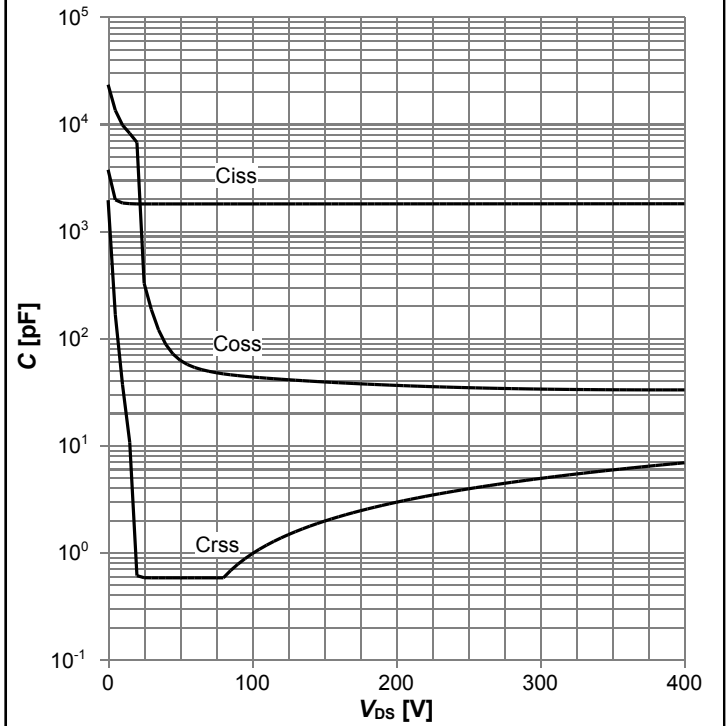
$E_{AS} = f(T_j)$; $I_D = 5.0 A$; $V_{DD} = 50 V$

Diagram 13: Drain-source breakdown voltage



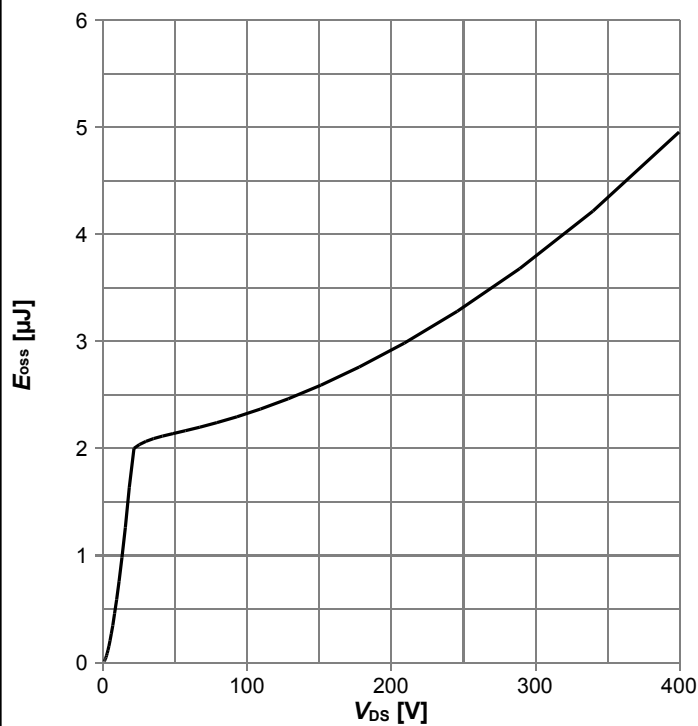
$V_{BR(DSS)}=f(T_j); I_D=1 \text{ mA}$

Diagram 14: Typ. capacitances



$C=f(V_{DS}); V_{GS}=0 \text{ V}; f=250 \text{ kHz}$

Diagram 15: Typ. Coss stored energy



$E_{oss}=f(V_{DS})$

5 Test Circuits

Table 8 Diode characteristics



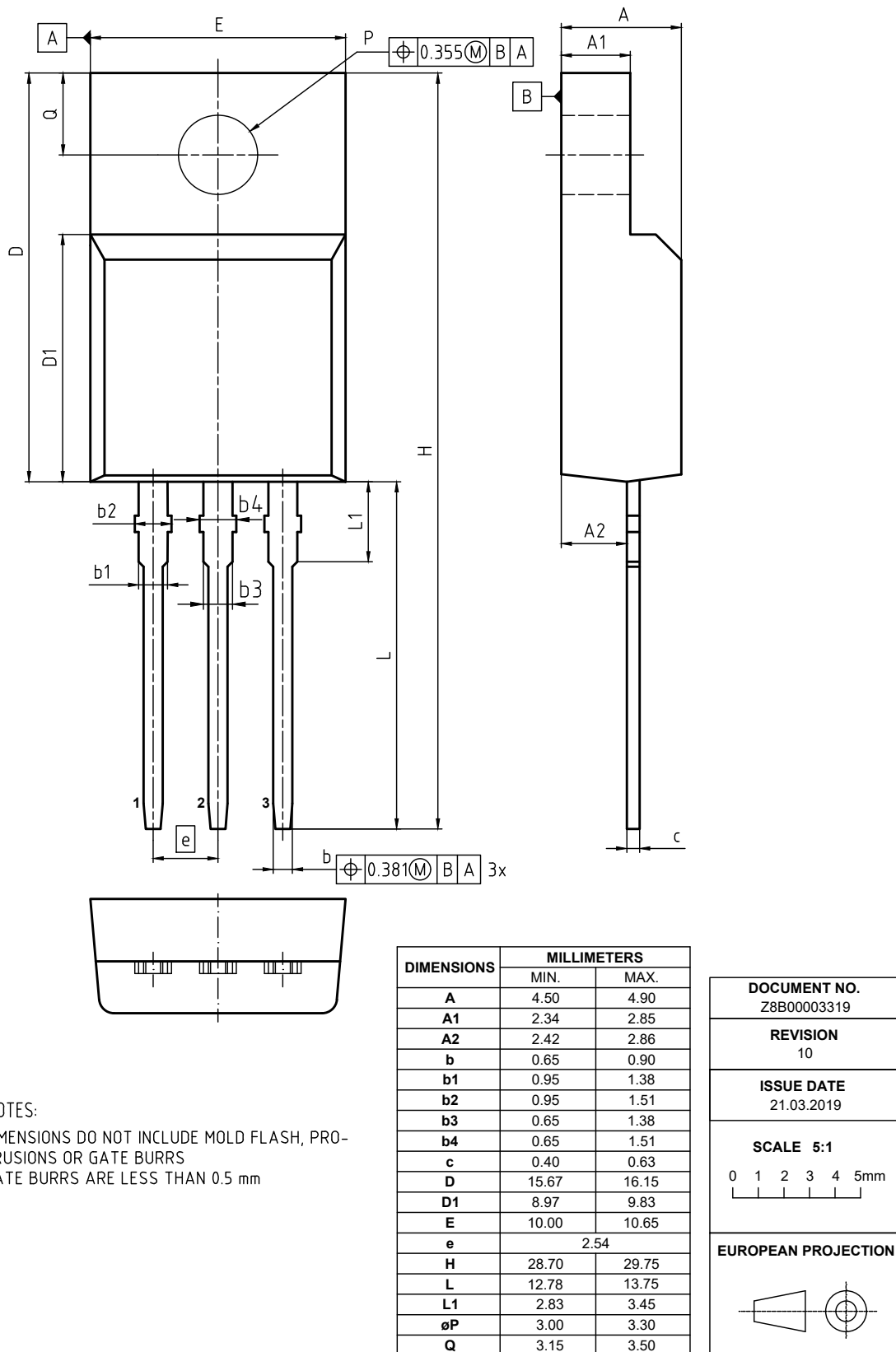
Table 9 Switching times



Table 10 Unclamped inductive load



6 Package Outlines



NOTES:
 DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS
 GATE BURRS ARE LESS THAN 0.5 mm

Figure 1 Outline PG-TO 220 FullPAK, dimensions in mm

7 Appendix A

Table 11 Related Links

- IFX CoolMOS™ C7 Webpage: www.infineon.com
- IFX CoolMOS™ C7 application note: www.infineon.com
- IFX CoolMOS™ C7 simulation model: www.infineon.com
- IFX Design tools: www.infineon.com

Revision History

IPA60R099C7

Revision: 2020-01-29, Rev. 2.1

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2015-08-10	Release of final version
2.1	2020-01-29	Updated package drawing, symbol ID and product validation

Trademarks

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