

NTMSD6N303, NVMSD6N303

Power MOSFET

6 Amps, 30 Volts N-Channel SO-8 FETKY™

The FETKY product family incorporates low $R_{DS(on)}$ MOSFETs packaged with an industry leading, low forward drop, low leakage Schottky Barrier rectifier to offer high efficiency components in a space saving configuration. Independent pinouts for MOSFET and Schottky die allow the flexibility to use a single component for switching and rectification functions in a wide variety of applications.

Features

- These Devices are Pb-Free and are RoHS Compliant
- NVMSD Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable

Applications

- Buck Converter
- Buck-Boost
- Synchronous Rectification
- Low Voltage Motor Control
- Battery Packs
- Chargers
- Cell Phones

MOSFET MAXIMUM RATINGS

($T_J = 25^\circ\text{C}$ unless otherwise noted) (Note 1)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DS}	30	Vdc
Drain-to-Gate Voltage ($R_{GS} = 1.0\text{ M}\Omega$)	V_{DGR}	30	Vdc
Gate-to-Source Voltage - Continuous	V_{GS}	± 20	Vdc
Drain Current - (Note 2)			
- Continuous @ $T_A = 25^\circ\text{C}$	I_D	6.0	Adc
- Single Pulse ($t_p \leq 10\ \mu\text{s}$)	I_{DM}	30	Apk
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ (Note 2)	P_D	2.0	Watts
Single Pulse Drain-to-Source Avalanche Energy - Starting $T_J = 25^\circ\text{C}$ ($V_{DD} = 30\text{ Vdc}$, $V_{GS} = 5.0\text{ Vdc}$, $V_{DS} = 20\text{ Vdc}$, $I_L = 9.0\text{ Apk}$, $L = 10\text{ mH}$, $R_G = 25\ \Omega$)	E_{AS}	325	mJ

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Pulse Test: Pulse Width $\leq 250\ \mu\text{s}$, Duty Cycle $\leq 2.0\%$.
2. Mounted on 2" square FR4 board
(1 in sq, 2 oz. Cu 0.06" thick single sided), 10 sec. max.

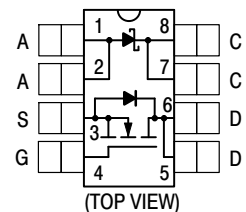


ON Semiconductor®

<http://onsemi.com>

MOSFET
6.0 AMPERES
30 VOLTS
24 m Ω @ $V_{GS} = 10\text{ V}$ (Typ)

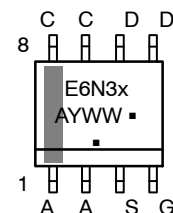
SCHOTTKY DIODE
6.0 AMPERES
30 VOLTS
420 mV @ $I_F = 3.0\text{ A}$



MARKING DIAGRAM & PIN ASSIGNMENT



SO-8
CASE 751
STYLE 18



E6N3 = Device Code
x = Blank or S
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb-Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NTMSD6N303R2G	SO-8 (Pb-Free)	2500/Tape & Reel
NTMSD6N303R2SG	SO-8 (Pb-Free)	2500/Tape & Reel
NVMSD6N303R2G	SO-8 (Pb-Free)	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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SCHOTTKY RECTIFIER MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Peak Repetitive Reverse Voltage DC Blocking Voltage	V_{RRM} V_R	30	Volts
Average Forward Current (Note 3) (Rated V_R) $T_A = 104^\circ\text{C}$	I_O	2.0	Amps
Peak Repetitive Forward Current (Note 3) (Rated V_R , Square Wave, 20 kHz) $T_A = 108^\circ\text{C}$	I_{frm}	4.0	Amps
Non-Repetitive Peak Surge Current (Surge applied at rated load conditions, half-wave, single phase, 60 Hz)	I_{fsm}	30	Amps

THERMAL CHARACTERISTICS – SCHOTTKY AND MOSFET

Thermal Resistance – Junction-to-Ambient (Note 4) – MOSFET	$R_{\theta JA}$	167	°C/W
Thermal Resistance – Junction-to-Ambient (Note 5) – MOSFET	$R_{\theta JA}$	97	
Thermal Resistance – Junction-to-Ambient (Note 3) – MOSFET	$R_{\theta JA}$	62.5	
Thermal Resistance – Junction-to-Ambient (Note 4) – Schottky	$R_{\theta JA}$	197	
Thermal Resistance – Junction-to-Ambient (Note 5) – Schottky	$R_{\theta JA}$	97	
Thermal Resistance – Junction-to-Ambient (Note 3) – Schottky	$R_{\theta JA}$	62.5	
Operating and Storage Temperature Range	T_J, T_{stg}	-55 to +150	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

3. Mounted on 2" square FR4 board (1 in sq, 2 oz. Cu 0.06" thick single sided), 10 sec. max.
4. Mounted with minimum recommended pad size, PC Board FR4.
5. Mounted on 2" square FR4 board (1 in sq, 2 oz. Cu 0.06" thick single sided), Steady State.

SCHOTTKY RECTIFIER ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristics	Symbol	Value		Unit
		$T_J = 25^\circ\text{C}$	$T_J = 125^\circ\text{C}$	
Maximum Instantaneous Forward Voltage (Note 6) $I_F = 100 \text{ mAdc}$ $I_F = 3.0 \text{ Adc}$ $I_F = 6.0 \text{ Adc}$	V_F	$T_J = 25^\circ\text{C}$	$T_J = 125^\circ\text{C}$	Volts
		0.28	0.13	
		0.42	0.33	
		0.50	0.45	
Maximum Instantaneous Reverse Current (Note 6) $V_R = 30 \text{ V}$	I_R	$T_J = 25^\circ\text{C}$	$T_J = 125^\circ\text{C}$	μA mA
		250 -	- 25	
Maximum Voltage Rate of Change $V_R = 30 \text{ V}$	dV/dt	10,000		V/ μs

6. Pulse Test: Pulse Width $\leq 300 \mu\text{s}$, Duty Cycle $\leq 2.0\%$

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MOSFET ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage ($V_{GS} = 0\text{ Vdc}$, $I_D = 250\ \mu\text{A}$) Temperature Coefficient (Positive)	$V_{(BR)DSS}$	30 -	- 30	- -	Vdc mV/ $^\circ\text{C}$
Zero Gate Voltage Drain Current ($V_{DS} = 24\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$, $T_J = 25^\circ\text{C}$) ($V_{DS} = 24\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$, $T_J = 125^\circ\text{C}$)	I_{DSS}	- -	- -	1.0 20	μAdc
Gate-Body Leakage Current ($V_{GS} = \pm 20\text{ Vdc}$, $V_{DS} = 0\text{ Vdc}$)	I_{GSS}	-	-	100	nAdc

ON CHARACTERISTICS (Note 7)

Gate Threshold Voltage ($V_{DS} = V_{GS}$, $I_D = 250\ \mu\text{Adc}$) Temperature Coefficient (Negative)	$V_{GS(th)}$	1.0 -	1.8 4.6	2.5 -	Vdc mV/ $^\circ\text{C}$
Static Drain-to-Source On-State Resistance ($V_{GS} = 10\text{ Vdc}$, $I_D = 6\text{ Adc}$) ($V_{GS} = 4.5\text{ Vdc}$, $I_D = 3.9\text{ Adc}$)	$R_{DS(on)}$	- -	0.024 0.030	0.032 0.040	Ω
Forward Transconductance ($V_{DS} = 15\text{ Vdc}$, $I_D = 5.0\text{ Adc}$)	g_{FS}	-	10	-	Mhos

DYNAMIC CHARACTERISTICS

Input Capacitance	$(V_{DS} = 24\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$, $f = 1.0\text{ MHz}$)	C_{iss}	-	680	950	pF
Output Capacitance		C_{oss}	-	210	300	
Reverse Transfer Capacitance		C_{rss}	-	70	135	

SWITCHING CHARACTERISTICS (Notes 7 & 8)

Turn-On Delay Time	$(V_{DD} = 15\text{ Vdc}$, $I_D = 1\text{ A}$, $V_{GS} = 10\text{ V}$, $R_G = 6\ \Omega$)	$t_{d(on)}$	-	9	18	ns
Rise Time		t_r	-	22	40	
Turn-Off Delay Time		$t_{d(off)}$	-	45	80	
Fall Time		t_f	-	45	80	
Turn-On Delay Time	$(V_{DD} = 15\text{ Vdc}$, $I_D = 1\text{ A}$, $V_{GS} = 4.5\text{ V}$, $R_G = 6\ \Omega$)	$t_{d(on)}$	-	13	30	ns
Rise Time		t_r	-	27	50	
Turn-Off Delay Time		$t_{d(off)}$	-	22	40	
Fall Time		t_f	-	34	70	
Gate Charge	$(V_{DS} = 15\text{ Vdc}$, $V_{GS} = 10\text{ Vdc}$, $I_D = 5\text{ A}$)	Q_T	-	19	30	nC
		Q_1	-	2.4	-	
		Q_2	-	5.0	-	
		Q_3	-	4.3	-	

BODY-DRAIN DIODE RATINGS (Note 7)

Diode Forward On-Voltage	$(I_S = 1.7\text{ Adc}$, $V_{GS} = 0\text{ V}$) $(I_S = 1.7\text{ Adc}$, $V_{GS} = 0\text{ V}$, $T_J = 150^\circ\text{C}$)	V_{SD}	- -	0.75 0.62	1.0 -	Vdc
Reverse Recovery Time	$(I_S = 5\text{ A}$, $V_{GS} = 0\text{ V}$, $dI_S/dt = 100\text{ A}/\mu\text{s}$)	t_{rr}	-	26	-	ns
		t_a	-	11	-	
		t_b	-	15	-	
Reverse Recovery Stored Charge ($I_S = 5\text{ A}$, $dI_S/dt = 100\text{ A}/\mu\text{s}$, $V_{GS} = 0\text{ V}$)		Q_{RR}	-	0.015	-	μC

7. Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$.

8. Switching characteristics are independent of operating junction temperature.

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TYPICAL MOSFET ELECTRICAL CHARACTERISTICS

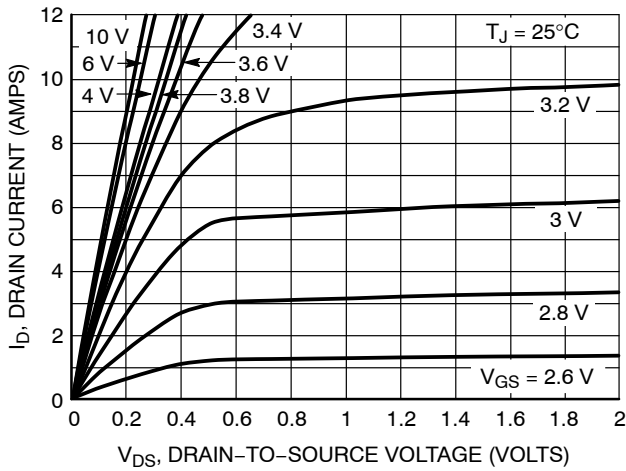


Figure 1. On-Region Characteristics

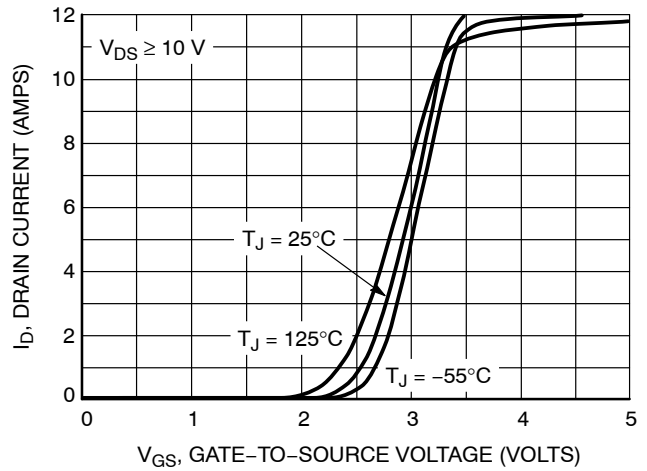


Figure 2. Transfer Characteristics

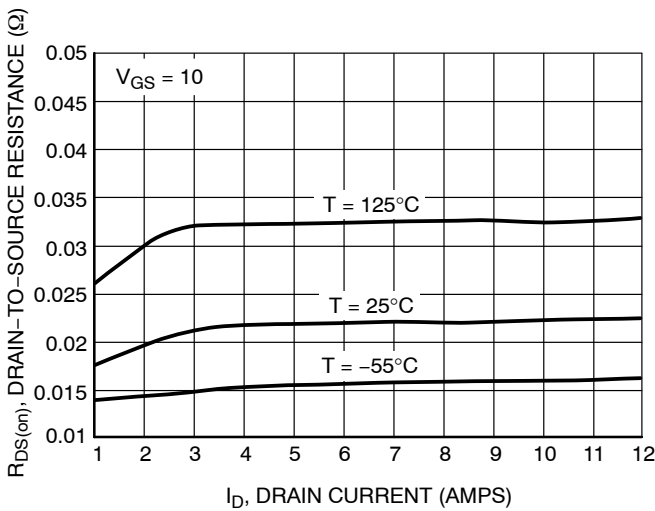


Figure 3. On-Resistance versus Drain Current and Temperature

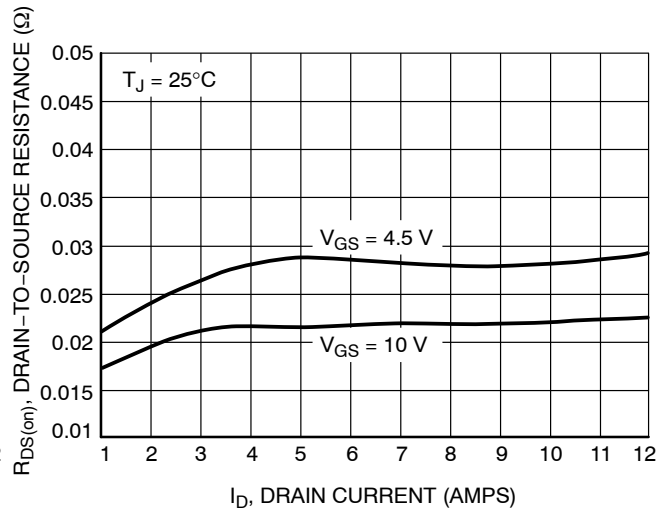


Figure 4. On-Resistance versus Drain Current and Gate Voltage

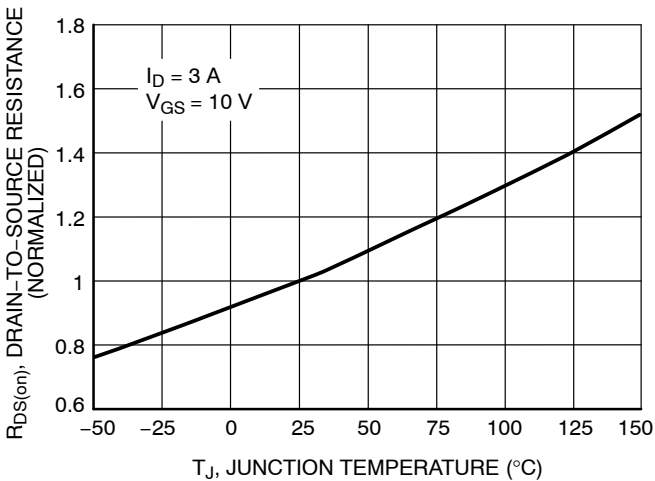


Figure 5. On-Resistance Variation with Temperature

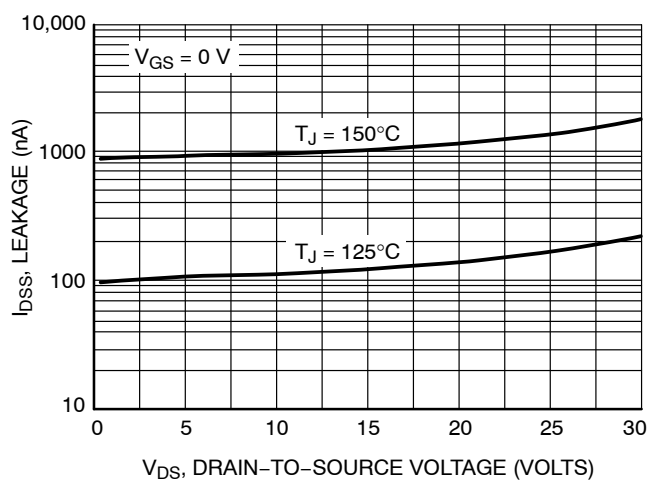


Figure 6. Drain-to-Source Leakage Current versus Voltage

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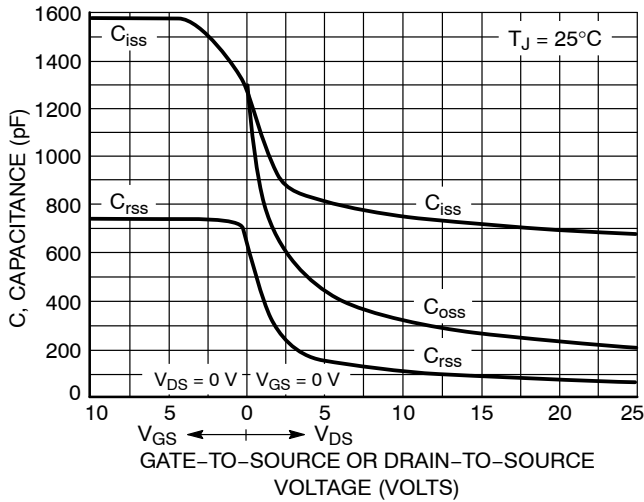


Figure 7. Capacitance Variation

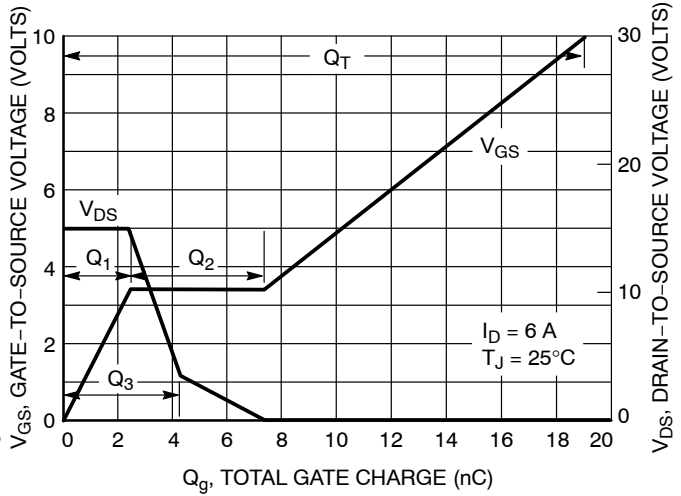


Figure 8. Gate-to-Source and Drain-to-Source Voltage versus Total Charge

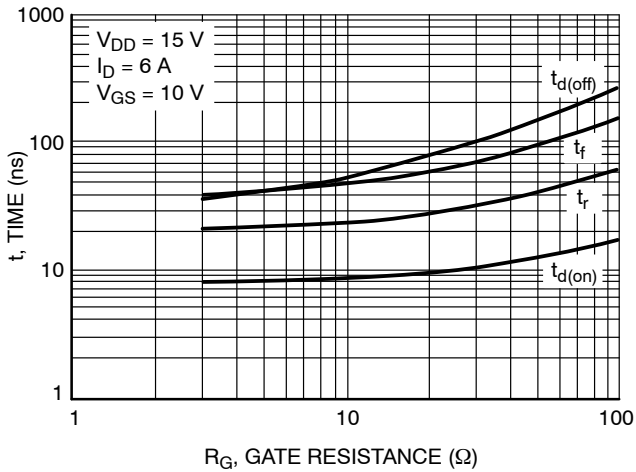


Figure 9. Resistive Switching Time Variation versus Gate Resistance

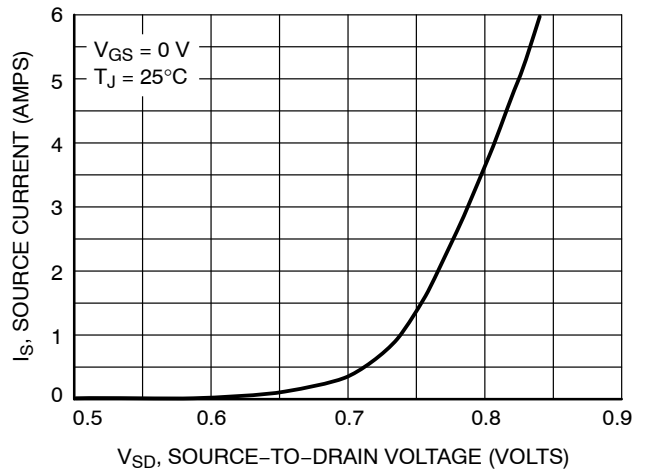


Figure 10. Diode Forward Voltage versus Current

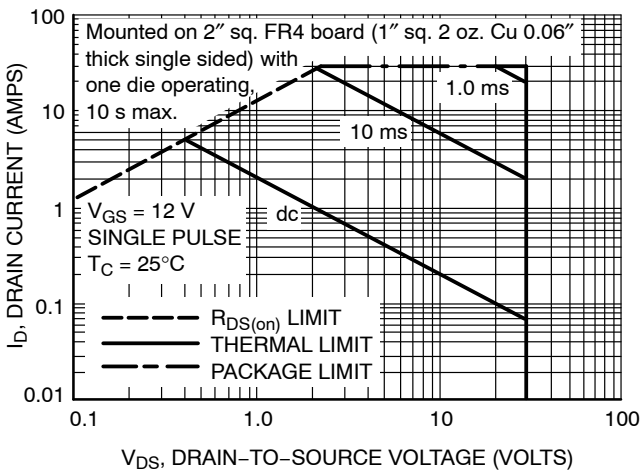


Figure 11. Maximum Rated Forward Biased Safe Operating Area

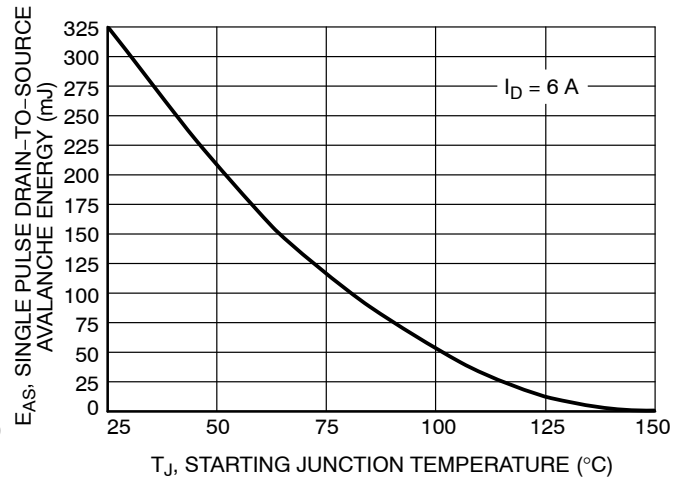


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

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TYPICAL FET ELECTRICAL CHARACTERISTICS

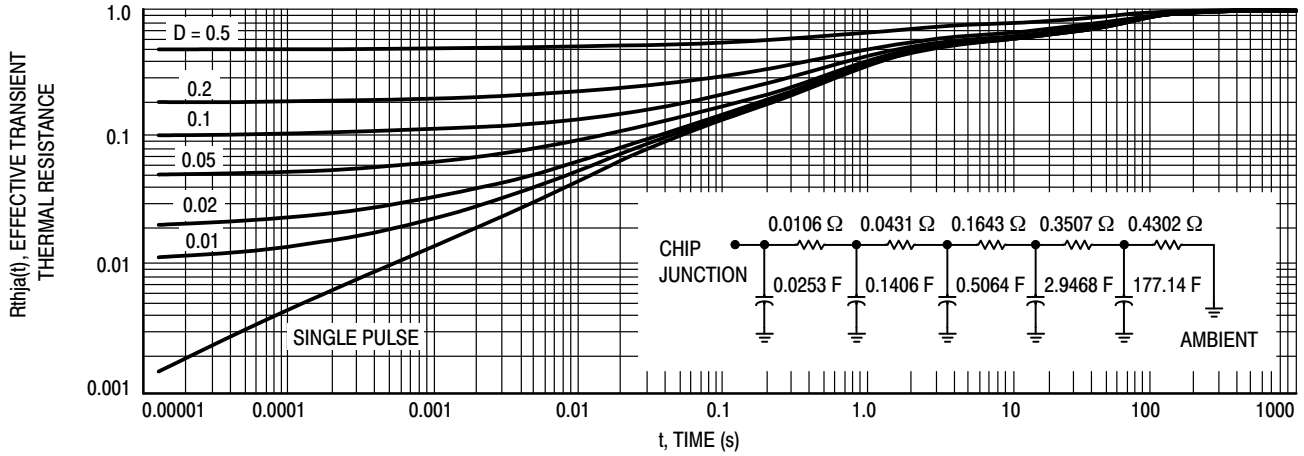


Figure 13. FET Thermal Response

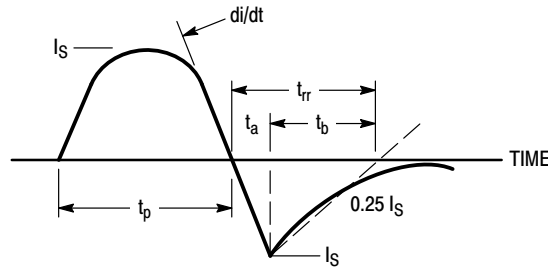


Figure 14. Diode Reverse Recovery Waveform

TYPICAL SCHOTTKY ELECTRICAL CHARACTERISTICS

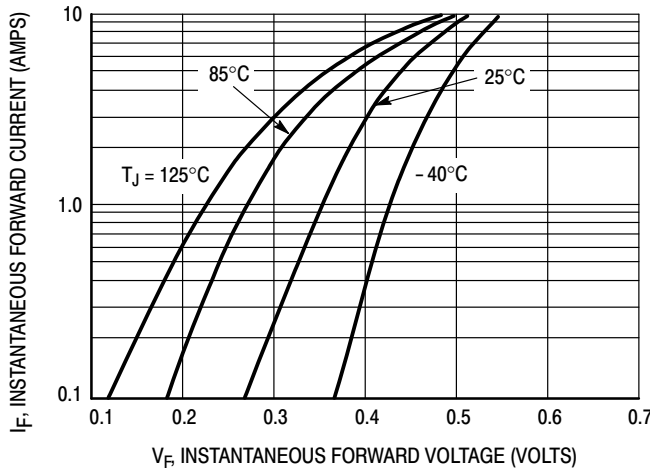


Figure 15. Typical Forward Voltage

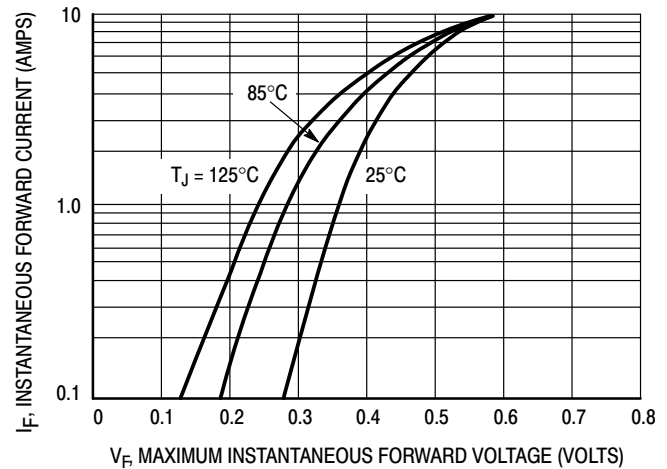


Figure 16. Maximum Forward Voltage

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TYPICAL SCHOTTKY ELECTRICAL CHARACTERISTICS

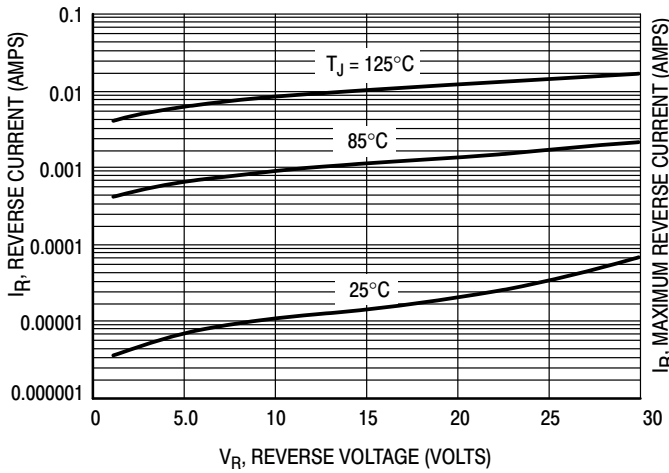


Figure 17. Typical Reverse Current

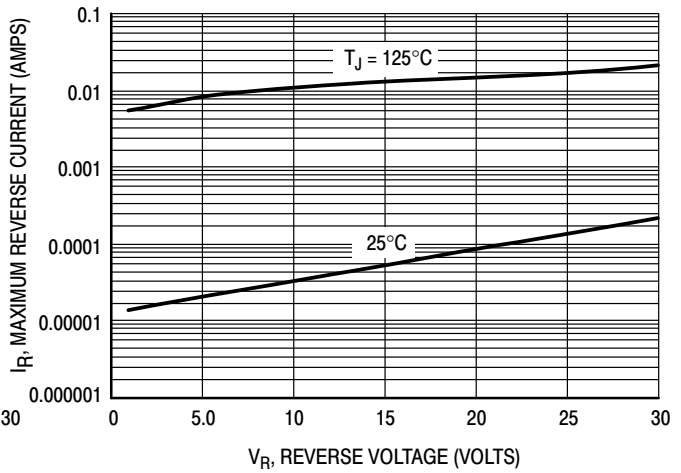


Figure 18. Maximum Reverse Current

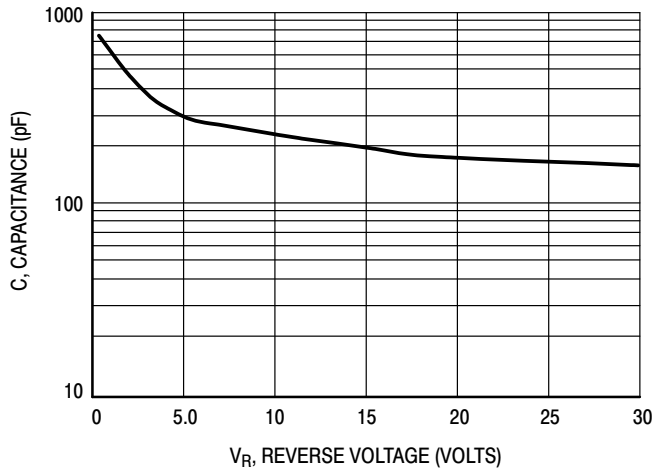


Figure 19. Typical Capacitance

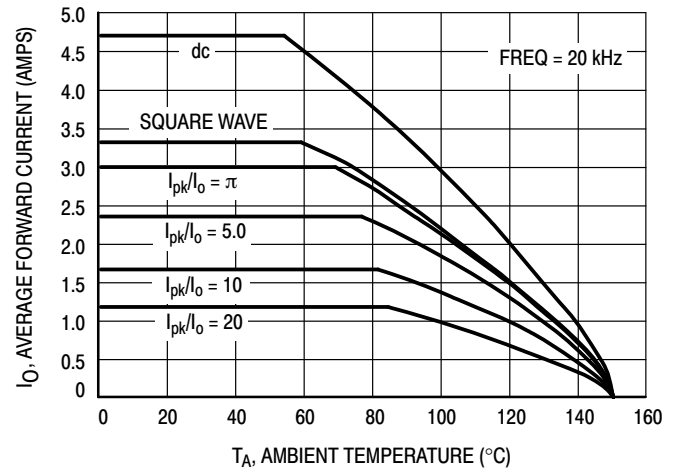


Figure 20. Current Derating

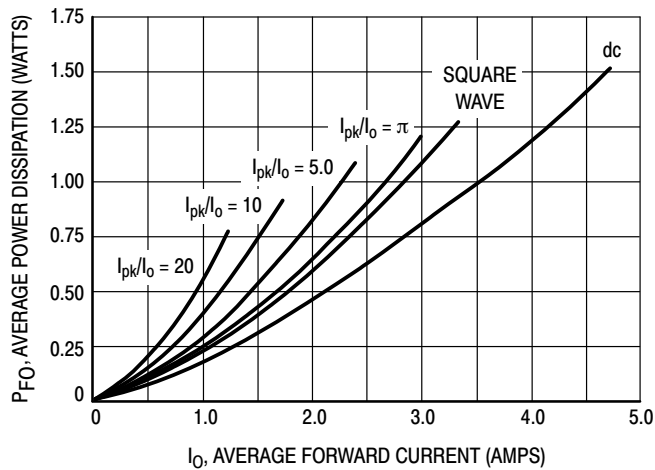


Figure 21. Forward Power Dissipation

NTMSD6N303, NVMSD6N303

TYPICAL SCHOTTKY ELECTRICAL CHARACTERISTICS

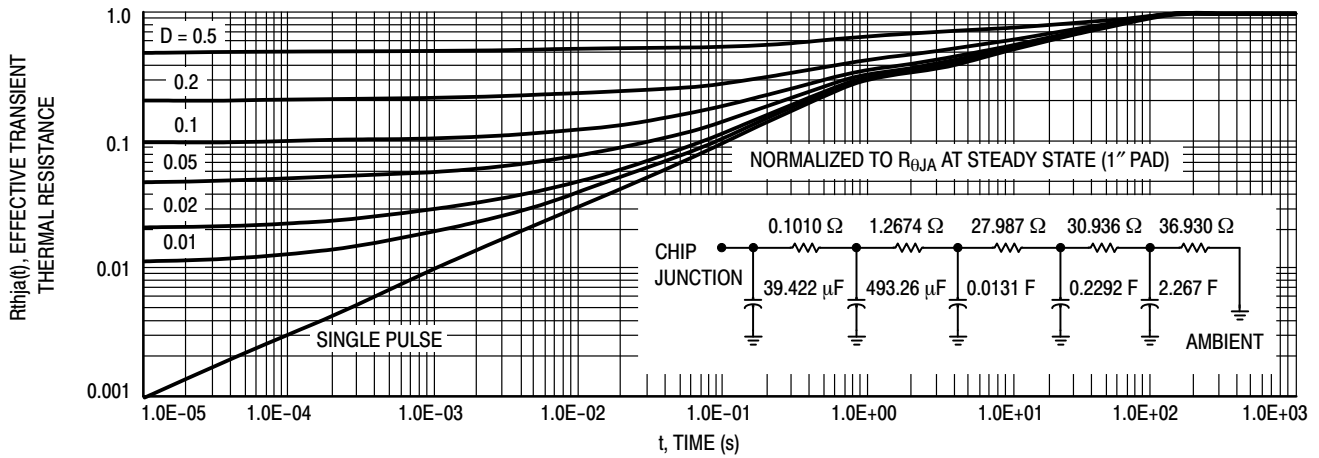
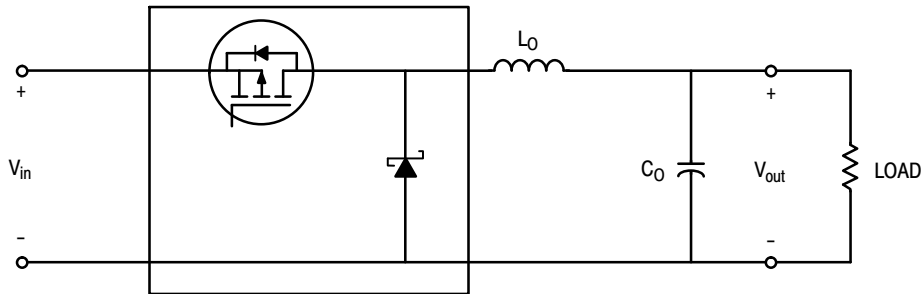


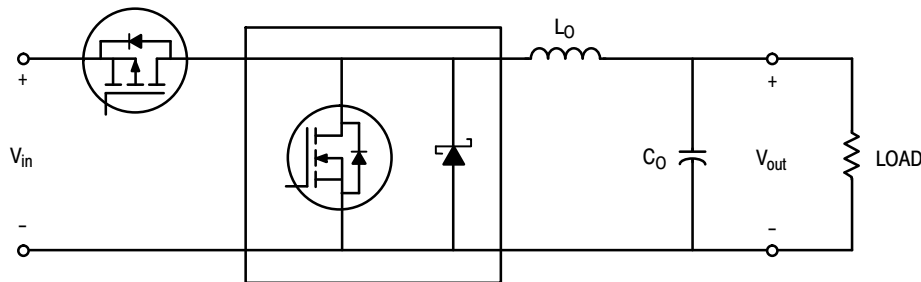
Figure 22. Schottky Thermal Response

TYPICAL APPLICATIONS

STEP DOWN SWITCHING REGULATORS



Buck Regulator

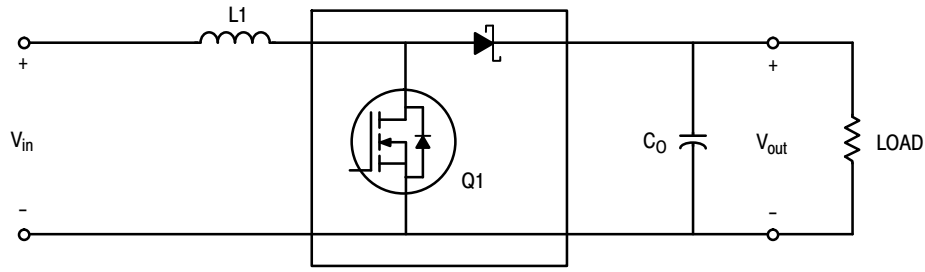


Synchronous Buck Regulator

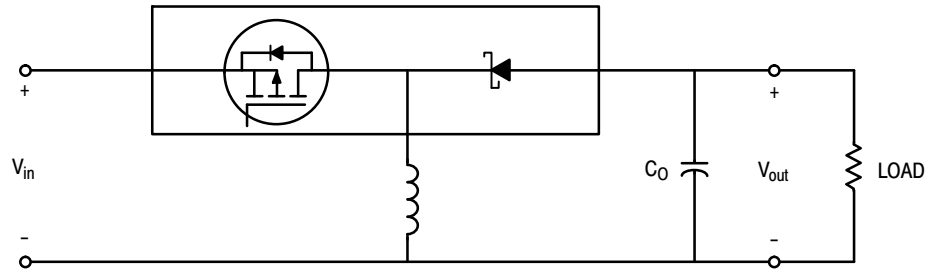
NTMSD6N303, NVMSD6N303

TYPICAL APPLICATIONS

STEP UP SWITCHING REGULATORS

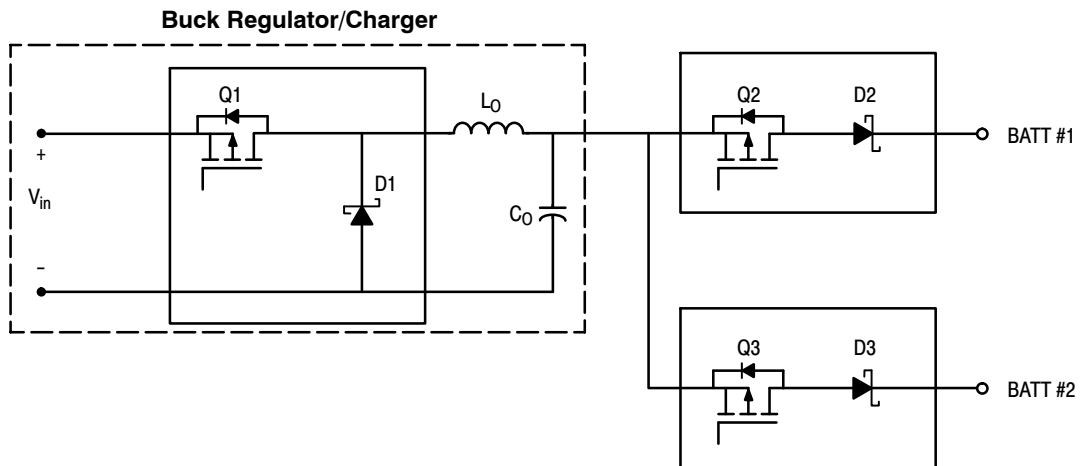


Boost Regulator



Buck-Boost Regulator

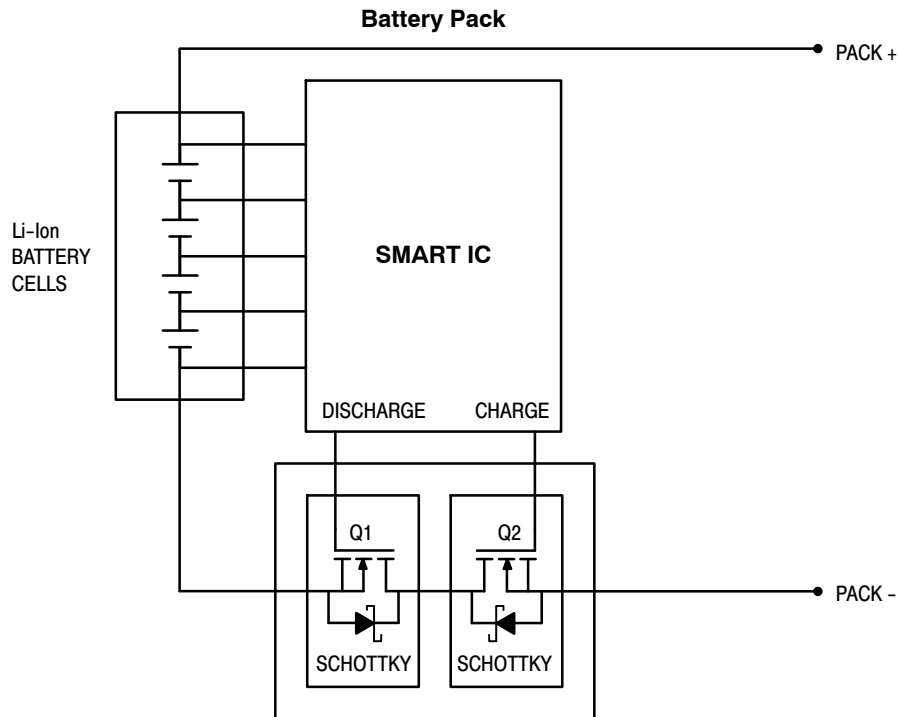
MULTIPLE BATTERY CHARGERS



NTMSD6N303, NVMSD6N303

TYPICAL APPLICATIONS

Li-Ion BATTERY PACK APPLICATIONS



- Applicable in battery packs which require a high current level.
- During charge cycle Q2 is on and Q1 is off. Schottky can reduce power loss during fast charge.
- During discharge Q1 is on and Q2 is off. Again, Schottky can reduce power dissipation.
- Under normal operation, both transistors are on.

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1

SOIC-8 NB
CASE 751-07
ISSUE AK

DATE 16 FEB 2011



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
 5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
 6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

GENERIC MARKING DIAGRAM*



SCALE 6:1 ($\frac{\text{mm}}{\text{inches}}$)



XXXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLES ON PAGE 2

DOCUMENT NUMBER:	98ASB42564B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SOIC-8 NB	PAGE 1 OF 2

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SOIC-8 NB
CASE 751-07
ISSUE AK

DATE 16 FEB 2011

- | | | | |
|---|--|--|--|
| <p>STYLE 1:
 PIN 1. EMITTER
 2. COLLECTOR
 3. COLLECTOR
 4. EMITTER
 5. EMITTER
 6. BASE
 7. BASE
 8. EMITTER</p> | <p>STYLE 2:
 PIN 1. COLLECTOR, DIE, #1
 2. COLLECTOR, #1
 3. COLLECTOR, #2
 4. COLLECTOR, #2
 5. BASE, #2
 6. EMITTER, #2
 7. BASE, #1
 8. EMITTER, #1</p> | <p>STYLE 3:
 PIN 1. DRAIN, DIE #1
 2. DRAIN, #1
 3. DRAIN, #2
 4. DRAIN, #2
 5. GATE, #2
 6. SOURCE, #2
 7. GATE, #1
 8. SOURCE, #1</p> | <p>STYLE 4:
 PIN 1. ANODE
 2. ANODE
 3. ANODE
 4. ANODE
 5. ANODE
 6. ANODE
 7. ANODE
 8. COMMON CATHODE</p> |
| <p>STYLE 5:
 PIN 1. DRAIN
 2. DRAIN
 3. DRAIN
 4. DRAIN
 5. GATE
 6. GATE
 7. SOURCE
 8. SOURCE</p> | <p>STYLE 6:
 PIN 1. SOURCE
 2. DRAIN
 3. DRAIN
 4. SOURCE
 5. SOURCE
 6. GATE
 7. GATE
 8. SOURCE</p> | <p>STYLE 7:
 PIN 1. INPUT
 2. EXTERNAL BYPASS
 3. THIRD STAGE SOURCE
 4. GROUND
 5. DRAIN
 6. GATE 3
 7. SECOND STAGE Vd
 8. FIRST STAGE Vd</p> | <p>STYLE 8:
 PIN 1. COLLECTOR, DIE #1
 2. BASE, #1
 3. BASE, #2
 4. COLLECTOR, #2
 5. COLLECTOR, #2
 6. EMITTER, #2
 7. EMITTER, #1
 8. COLLECTOR, #1</p> |
| <p>STYLE 9:
 PIN 1. EMITTER, COMMON
 2. COLLECTOR, DIE #1
 3. COLLECTOR, DIE #2
 4. EMITTER, COMMON
 5. EMITTER, COMMON
 6. BASE, DIE #2
 7. BASE, DIE #1
 8. EMITTER, COMMON</p> | <p>STYLE 10:
 PIN 1. GROUND
 2. BIAS 1
 3. OUTPUT
 4. GROUND
 5. GROUND
 6. BIAS 2
 7. INPUT
 8. GROUND</p> | <p>STYLE 11:
 PIN 1. SOURCE 1
 2. GATE 1
 3. SOURCE 2
 4. GATE 2
 5. DRAIN 2
 6. DRAIN 2
 7. DRAIN 1
 8. DRAIN 1</p> | <p>STYLE 12:
 PIN 1. SOURCE
 2. SOURCE
 3. SOURCE
 4. GATE
 5. DRAIN
 6. DRAIN
 7. DRAIN
 8. DRAIN</p> |
| <p>STYLE 13:
 PIN 1. N.C.
 2. SOURCE
 3. SOURCE
 4. GATE
 5. DRAIN
 6. DRAIN
 7. DRAIN
 8. DRAIN</p> | <p>STYLE 14:
 PIN 1. N-SOURCE
 2. N-GATE
 3. P-SOURCE
 4. P-GATE
 5. P-DRAIN
 6. P-DRAIN
 7. N-DRAIN
 8. N-DRAIN</p> | <p>STYLE 15:
 PIN 1. ANODE 1
 2. ANODE 1
 3. ANODE 1
 4. ANODE 1
 5. CATHODE, COMMON
 6. CATHODE, COMMON
 7. CATHODE, COMMON
 8. CATHODE, COMMON</p> | <p>STYLE 16:
 PIN 1. EMITTER, DIE #1
 2. BASE, DIE #1
 3. EMITTER, DIE #2
 4. BASE, DIE #2
 5. COLLECTOR, DIE #2
 6. COLLECTOR, DIE #2
 7. COLLECTOR, DIE #1
 8. COLLECTOR, DIE #1</p> |
| <p>STYLE 17:
 PIN 1. VCC
 2. V2OUT
 3. V1OUT
 4. TXE
 5. RXE
 6. VEE
 7. GND
 8. ACC</p> | <p>STYLE 18:
 PIN 1. ANODE
 2. ANODE
 3. SOURCE
 4. GATE
 5. DRAIN
 6. DRAIN
 7. CATHODE
 8. CATHODE</p> | <p>STYLE 19:
 PIN 1. SOURCE 1
 2. GATE 1
 3. SOURCE 2
 4. GATE 2
 5. DRAIN 2
 6. MIRROR 2
 7. DRAIN 1
 8. MIRROR 1</p> | <p>STYLE 20:
 PIN 1. SOURCE (N)
 2. GATE (N)
 3. SOURCE (P)
 4. GATE (P)
 5. DRAIN
 6. DRAIN
 7. DRAIN
 8. DRAIN</p> |
| <p>STYLE 21:
 PIN 1. CATHODE 1
 2. CATHODE 2
 3. CATHODE 3
 4. CATHODE 4
 5. CATHODE 5
 6. COMMON ANODE
 7. COMMON ANODE
 8. CATHODE 6</p> | <p>STYLE 22:
 PIN 1. I/O LINE 1
 2. COMMON CATHODE/VCC
 3. COMMON CATHODE/VCC
 4. I/O LINE 3
 5. COMMON ANODE/GND
 6. I/O LINE 4
 7. I/O LINE 5
 8. COMMON ANODE/GND</p> | <p>STYLE 23:
 PIN 1. LINE 1 IN
 2. COMMON ANODE/GND
 3. COMMON ANODE/GND
 4. LINE 2 IN
 5. LINE 2 OUT
 6. COMMON ANODE/GND
 7. COMMON ANODE/GND
 8. LINE 1 OUT</p> | <p>STYLE 24:
 PIN 1. BASE
 2. EMITTER
 3. COLLECTOR/ANODE
 4. COLLECTOR/ANODE
 5. CATHODE
 6. CATHODE
 7. COLLECTOR/ANODE
 8. COLLECTOR/ANODE</p> |
| <p>STYLE 25:
 PIN 1. VIN
 2. N/C
 3. REXT
 4. GND
 5. IOUT
 6. IOUT
 7. IOUT
 8. IOUT</p> | <p>STYLE 26:
 PIN 1. GND
 2. dv/dt
 3. ENABLE
 4. ILIMIT
 5. SOURCE
 6. SOURCE
 7. SOURCE
 8. VCC</p> | <p>STYLE 27:
 PIN 1. ILIMIT
 2. OVLO
 3. UVLO
 4. INPUT+
 5. SOURCE
 6. SOURCE
 7. SOURCE
 8. DRAIN</p> | <p>STYLE 28:
 PIN 1. SW_TO_GND
 2. DASIC_OFF
 3. DASIC_SW_DET
 4. GND
 5. V_MON
 6. VBULK
 7. VBULK
 8. VIN</p> |
| <p>STYLE 29:
 PIN 1. BASE, DIE #1
 2. EMITTER, #1
 3. BASE, #2
 4. EMITTER, #2
 5. COLLECTOR, #2
 6. COLLECTOR, #2
 7. COLLECTOR, #1
 8. COLLECTOR, #1</p> | <p>STYLE 30:
 PIN 1. DRAIN 1
 2. DRAIN 1
 3. GATE 2
 4. SOURCE 2
 5. SOURCE 1/DRAIN 2
 6. SOURCE 1/DRAIN 2
 7. SOURCE 1/DRAIN 2
 8. GATE 1</p> | | |

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