

# NTS4172N

## Power MOSFET

### 30 V, 1.7 A, Single N-Channel, SC-70

#### Features

- Low On-Resistance
- Low Gate Threshold Voltage
- Halide Free
- This is a Pb-Free Device

#### Applications

- Low Side Load Switch
- DC-DC Converters (Buck and Boost Circuits)
- Optimized for Battery and Load Management Applications in Portable Equipment like Cell Phones, PDA's, Media Players, etc.

**MAXIMUM RATINGS** ( $T_J = 25^\circ\text{C}$  unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	$V_{DSS}$	30	V
Gate-to-Source Voltage	$V_{GS}$	$\pm 12$	V
Continuous Drain Current (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	1.6
		$T_A = 85^\circ\text{C}$	1.13
	$t \leq 5\text{ s}$	$T_A = 25^\circ\text{C}$	1.70
Power Dissipation (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	0.294
		$t \leq 5\text{ s}$	0.350
Pulsed Drain Current	$I_{DM}$	3.4	A
Operating Junction and Storage Temperature	$T_J, T_{stg}$	-55 to 150	$^\circ\text{C}$
Source Current (Body Diode)	$I_S$	0.25	A
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	$T_L$	260	$^\circ\text{C}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

#### THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Ambient – Steady State (Note 1)	$R_{\theta JA}$	425	$^\circ\text{C}/\text{W}$
Junction-to-Ambient – $t \leq 5\text{ s}$ (Note 1)	$R_{\theta JA}$	360	

1. Surface-mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces)

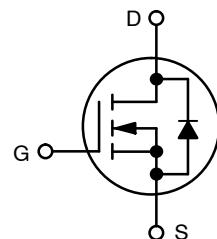


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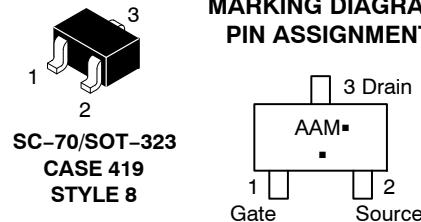
<http://onsemi.com>

$V_{(BR)DSS}$	$R_{DS(on)} \text{ MAX}$	$I_D \text{ MAX}$
30 V	93 m $\Omega$ @ 10 V	1.7 A
	100 m $\Omega$ @ 4.5 V	1.5 A
	140 m $\Omega$ @ 2.5 V	1.0 A

#### SC-70/SOT-323 (3 LEADS)



#### MARKING DIAGRAM/ PIN ASSIGNMENT



AA = Specific Device Code

M = Date Code\*

■ = Pb-Free Package

(Note: Microdot may be in either location)

\* Date code orientation may vary depending upon manufacturing location

#### ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
NTS4172NT1G	SC-70 (Pb-Free)	3000/Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

# NTS4172N

## MOSFET ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(\text{BR})\text{DSS}}$	$V_{\text{GS}} = 0 \text{ V}, I_D = 250 \mu\text{A}$	30			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(\text{BR})\text{DSS}}/T_J$	$I_D = 250 \mu\text{A}$ , Reference to $25^\circ\text{C}$		8.4		$\text{mV}/^\circ\text{C}$
Zero Gate Voltage Drain Current	$I_{\text{DSS}}$	$V_{\text{GS}} = 0 \text{ V}, V_{\text{DS}} = 24 \text{ V}, T_J = 25^\circ\text{C}$ $V_{\text{GS}} = 0 \text{ V}, V_{\text{DS}} = 24 \text{ V}, T_J = 125^\circ\text{C}$			1.0 5.0	$\mu\text{A}$
Gate-to-Source Leakage Current	$I_{\text{GSS}}$	$V_{\text{DS}} = 0 \text{ V}, V_{\text{GS}} = \pm 12 \text{ V}$			$\pm 100$	nA

### ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	$V_{\text{GS}(\text{TH})}$	$V_{\text{GS}} = V_{\text{DS}}, I_D = 250 \mu\text{A}$	0.6	1.0	1.4	V
Negative Threshold Temperature Coefficient	$V_{\text{GS}(\text{TH})}/T_J$			3.1		$\text{mV}/^\circ\text{C}$
Drain-to-Source On-Resistance	$R_{\text{DS}(\text{on})}$	$V_{\text{GS}} = 10 \text{ V}, I_D = 1.7 \text{ A}$		58	93	$\text{m}\Omega$
		$V_{\text{GS}} = 4.5 \text{ V}, I_D = 1.5 \text{ A}$		64	100	
		$V_{\text{GS}} = 2.5 \text{ V}, I_D = 1.0 \text{ A}$		79	140	
Forward Transconductance	$g_{\text{FS}}$	$V_{\text{DS}} = 5.0 \text{ V}, I_D = 1.7 \text{ A}$		4.2		S

### CHARGES, CAPACITANCES AND GATE RESISTANCE

Input Capacitance	$C_{\text{iss}}$	$V_{\text{GS}} = 0 \text{ V}, f = 1.0 \text{ MHz}, V_{\text{DS}} = 15 \text{ V}$		381		pF
Output Capacitance	$C_{\text{oss}}$			39.6		
Reverse Transfer Capacitance	$C_{\text{rss}}$			32.6		
Total Gate Charge	$Q_{\text{G}(\text{TOT})}$	$V_{\text{GS}} = 4.5 \text{ V}, V_{\text{DS}} = 15 \text{ V}, I_D = 1.7 \text{ A}$		4.38		nC
Threshold Gate Charge	$Q_{\text{G}(\text{TH})}$			0.40		
Gate-to-Source Charge	$Q_{\text{GS}}$			0.62		
Gate-to-Drain Charge	$Q_{\text{GD}}$			1.33		
Gate Resistance	$R_G$			4.5		$\Omega$

### SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	$t_{\text{d}(\text{on})}$	$V_{\text{GS}} = 4.5 \text{ V}, V_{\text{DD}} = 15 \text{ V}, I_D = 1.7 \text{ A}, R_G = 3 \Omega$		7.5		ns
Rise Time	$t_r$			4.4		
Turn-Off Delay Time	$t_{\text{d}(\text{off})}$			16.1		
Fall Time	$t_f$			2.2		

### DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	$V_{\text{SD}}$	$V_{\text{GS}} = 0 \text{ V}, I_S = 1.0 \text{ A}$		0.76	1.0	V
Reverse Recovery Time	$t_{\text{RR}}$	$V_{\text{GS}} = 0 \text{ V}, I_S = 1.0 \text{ A}, \frac{dI_S}{dt} = 100 \text{ A}/\mu\text{s}$		7.9		ns
Charge Time	$t_a$			5.0		
Discharge Time	$t_b$			2.9		
Reverse Recovery Charge	$Q_{\text{RR}}$			2.0		nC

2. Surface-mounted on FR4 board using 1 in<sup>2</sup> pad size (Cu area = 1.127 in<sup>2</sup> [2 oz] including traces)

3. Pulse Test: Pulse Width  $\leq 300 \mu\text{s}$ , Duty Cycle  $\leq 2\%$

4. Switching characteristics are independent of operating junction temperatures

## TYPICAL CHARACTERISTICS

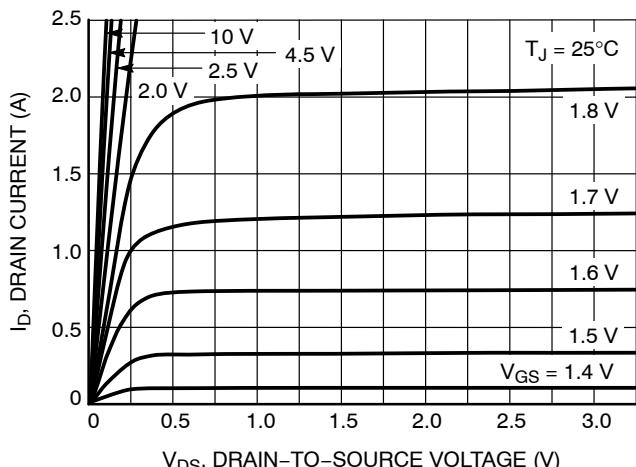


Figure 1. On-Region Characteristics

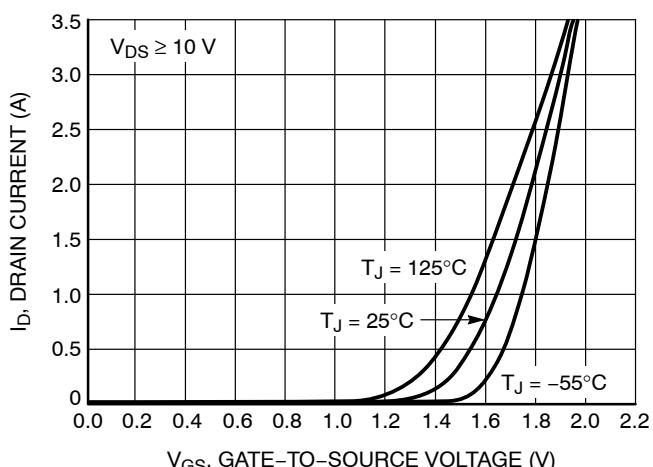


Figure 2. Transfer Characteristics

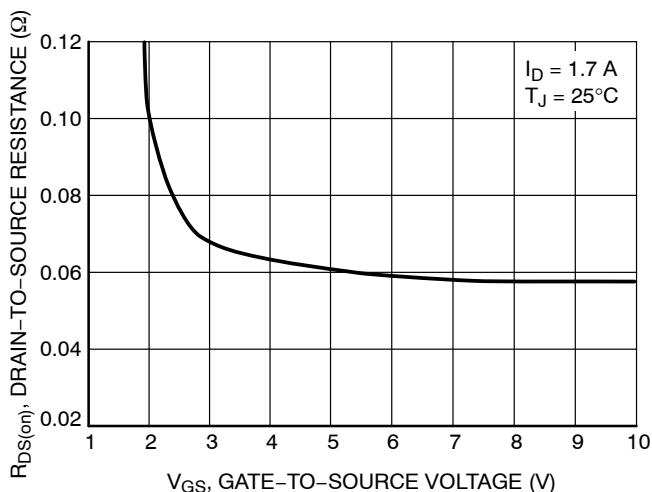


Figure 3. On-Resistance vs. Gate Voltage

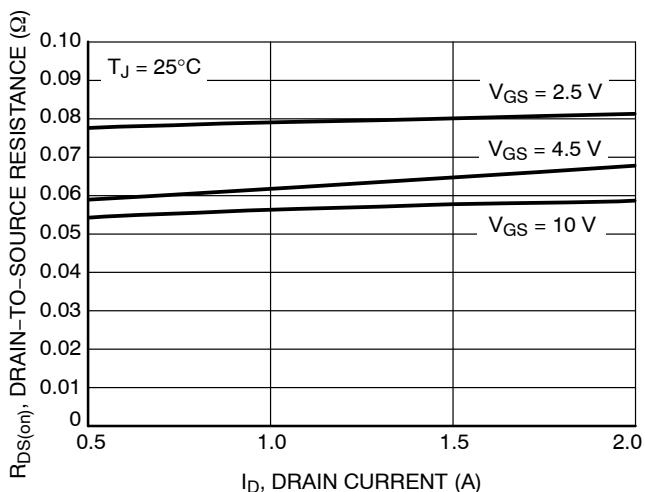


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

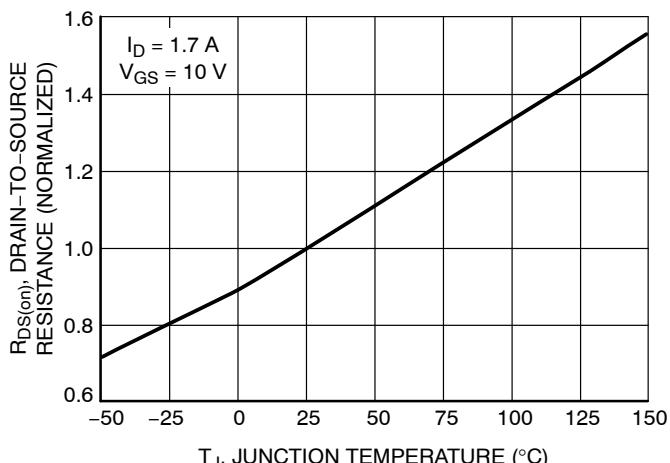


Figure 5. On-Resistance Variation with Temperature

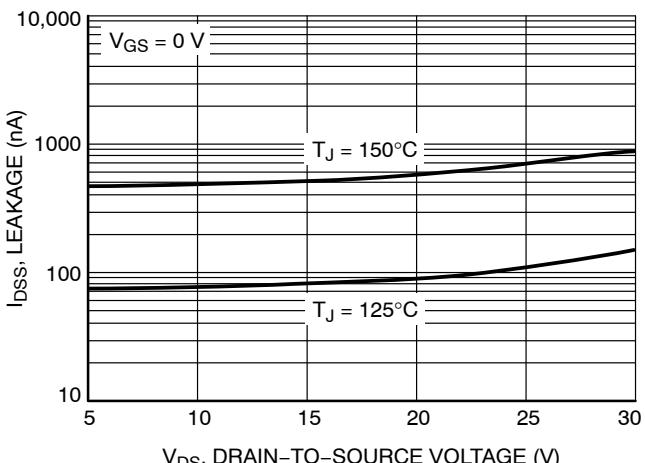


Figure 6. Drain-to-Source Leakage Current vs. Voltage

## TYPICAL CHARACTERISTICS

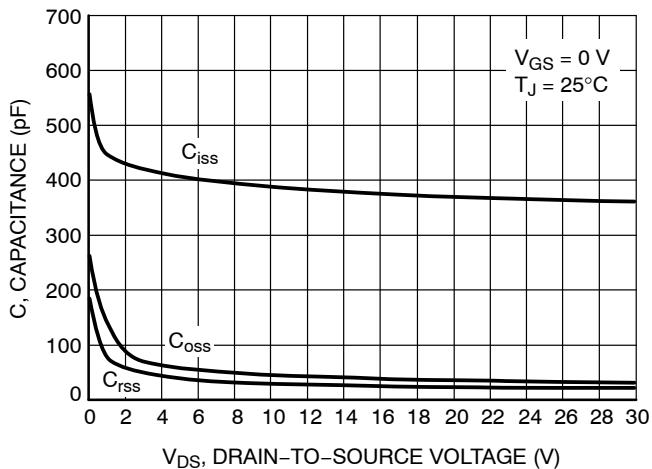


Figure 7. Capacitance Variation

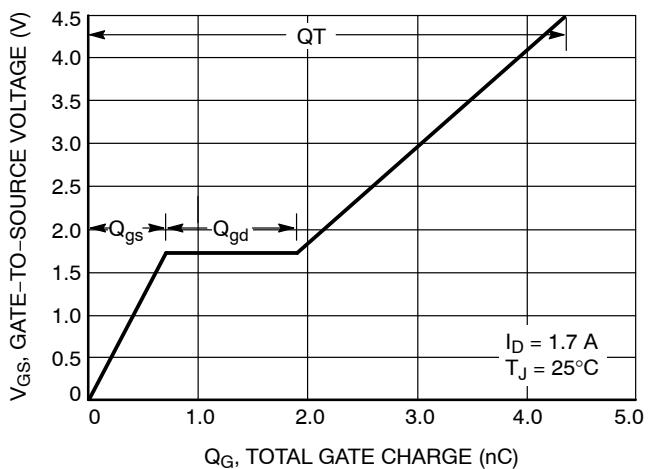


Figure 8. Gate-to-Source Voltage vs. Total Charge

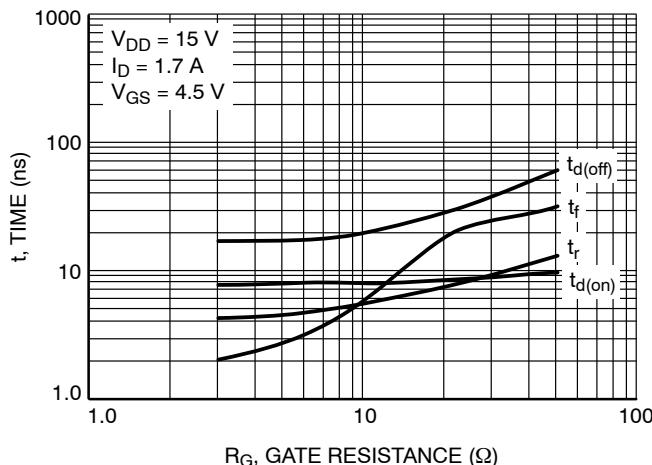


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

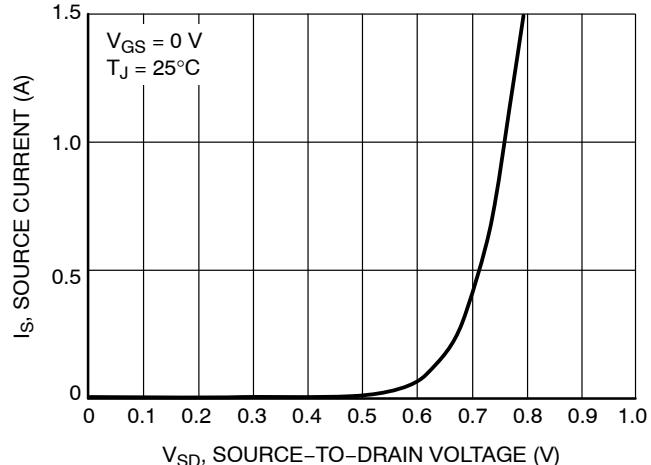
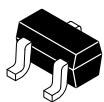


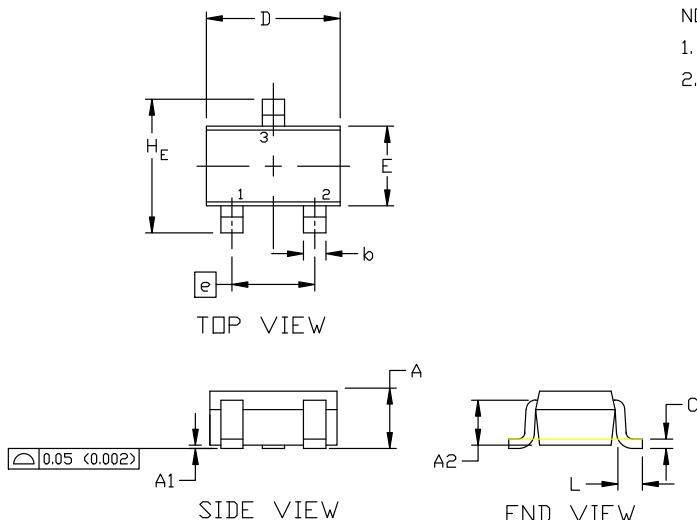
Figure 10. Diode Forward Voltage vs. Current

**MECHANICAL CASE OUTLINE**  
**PACKAGE DIMENSIONS**

**onsemi**<sup>TM</sup>



SCALE 4:1



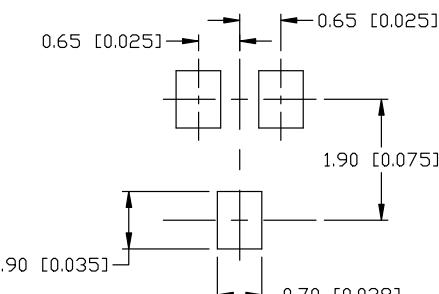
**SC-70 (SOT-323)**  
**CASE 419**  
**ISSUE R**

DATE 11 OCT 2022

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH

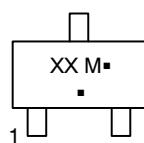
DIM	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.80	0.90	1.00	0.032	0.035	0.040
A1	0.00	0.05	0.10	0.000	0.002	0.004
A2	0.70 REF			0.028 BSC		
b	0.30	0.35	0.40	0.012	0.014	0.016
c	0.10	0.18	0.25	0.004	0.007	0.010
D	1.80	2.00	2.20	0.071	0.080	0.087
E	1.15	1.24	1.35	0.045	0.049	0.053
e	1.20	1.30	1.40	0.047	0.051	0.055
e1	0.65 BSC			0.026 BSC		
L	0.20	0.38	0.56	0.008	0.015	0.022
H <sub>E</sub>	2.00	2.10	2.40	0.079	0.083	0.095



\* For additional information on our Pb-Free strategy and soldering details, please download the [on Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D](#).

**SOLDERING FOOTPRINT**

**GENERIC  
MARKING DIAGRAM**



XX = Specific Device Code  
M = Date Code  
■ = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:  
CANCELLED

STYLE 2:  
PIN 1. ANODE  
2. N.C.  
3. CATHODE

STYLE 3:  
PIN 1. BASE  
2. Emitter  
3. Collector

STYLE 4:  
PIN 1. CATHODE  
2. CATHODE  
3. ANODE

STYLE 5:  
PIN 1. ANODE  
2. ANODE  
3. CATHODE

STYLE 6:  
PIN 1. Emitter  
2. BASE  
3. COLLECTOR

STYLE 7:  
PIN 1. BASE  
2. Emitter  
3. Collector

STYLE 8:  
PIN 1. GATE  
2. SOURCE  
3. DRAIN

STYLE 9:  
PIN 1. ANODE  
2. CATHODE  
3. CATHODE-ANODE

STYLE 10:  
PIN 1. CATHODE  
2. ANODE  
3. ANODE-CATHODE

STYLE 11:  
PIN 1. CATHODE  
2. CATHODE  
3. CATHODE

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