MOSFET - Complementary, POWERTRENCH®

N−Channel: 20 V, 3.8 A, 66 mΩ
P−Channel: −20 V, −2.6 A, 142 mΩ

FDME1034CZT

ON Semiconductor®

www.onsemi.com

General Description

This device is designed specifically as a single package solution for a DC/DC ‘Switching’ MOSFET in cellular handset and other ultra−portable applications. It features an independent N−Channel & P−Channel MOSFET with low on−state resistance for minimum conduction losses. The gate charge of each MOSFET is also minimized to allow high frequency switching directly from the controlling device.

The MicroFET 1.6x1.6 Thin package offers exceptional thermal performance for it’s physical size and is well suited to switching and linear mode applications.

Features

Q1: N−Channel

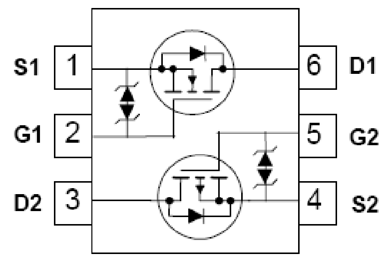
- Max $r_{DS(on)}$ = 66 mΩ at V_{GS} = 4.5 V, I_D = 3.4 A
- Max $r_{DS(on)}$ = 86 mΩ at V_{GS} = 2.5 V, I_D = 2.9 A
- Max $r_{DS(on)}$ = 113 mΩ at V_{GS} = 1.8 V, I_D = 2.5 A
- Max $r_{DS(on)}$ = 160 mΩ at V_{GS} = 1.5 V, I_D = 2.1 A

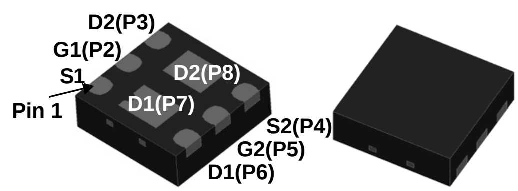
Q2: P−Channel

- Max $r_{DS(on)}$ = 142 mΩ at V_{GS} = −4.5 V, I_D = −2.3 A
- Max $r_{DS(on)}$ = 213 mΩ at V_{GS} = −2.5 V, I_D = −1.8 A
- Max $r_{DS(on)}$ = 331 mΩ at V_{GS} = −1.8 V, I_D = −1.5 A
- Max $r_{DS(on)}$ = 530 mΩ at V_{GS} = −1.5 V, I_D = −1.2 A
- Low Profile: 0.55 mm Maximum in the New Package MicroFET 1.6x1.6 Thin
- Free from Halogenated Compounds and Antimony Oxides
- HBM ESD Protection Level > 1600 V (Note 3)
- This Device is Pb−Free and is RoHS Compliant

Applications

- DC−DC Conversion
- Level Shifted Load Switch



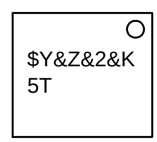


Bottom Top

Note: Center pad of P7 & P8 is a virtual pin number. Actual P7 & P8 is connected to edge pad of P6 & P3 respectively.

UDFN6 1.6x1.6, 0.5P
CASE 517DW

MARKING DIAGRAM



$Y	= ON Semiconductor Logo
&Z	= Assembly Plant Code
&2	= Numeric Date Code
&K	= Lot Code
5T	= Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

MOSFET MAXIMUM RATINGS (T_A = 25°C, Unless otherwise noted)

Symbol	Parameter	Q1	Q2	Units
V_{DS}	Drain to Source Voltage	20	−20	V
V_{GS}	Gate to Source Voltage	±8	±8	V
I_D	Drain Current −Continuous T_A = 25°C (Note 1a)	3.8	−2.6	A
	−Pulsed	6	−6	
P_D	Power Dissipation for Single Operation T_A = 25°C (Note 1a)	1.4		W
	Power Dissipation for Single Operation T_A = 25°C (Note 1b)	0.6		
T_J, T_{STG}	Operating and Storage Junction Temperature Range	−55 to +150		°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Units
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Single Operation) (Note 1a)	90	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Single Operation) (Note 1b)	195	

PACKAGE MARKING AND ORDERING INFORMATION

Device Marking	Device	Package	Shipping†
5T	FDME1034CZT	UDFN6 1.6x1.6, 0.5P (Pb−Free)	5000 units / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

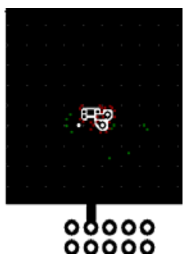
Symbol	Parameter	Test Conditions	Type	Min.	Typ.	Max.	Units
OFF CHARACTERISTICS							
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V I_D = −250 μA, V_{GS} = 0 V	Q1 Q2	20 −20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25°C I_D = −250 μA, referenced to 25°C	Q1 Q2		16 −12		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 16 V, V_{GS} = 0 V V_{DS} = −16 V, V_{GS} = 0 V	Q1 Q2			1 −1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±8 V, V_{DS} = 0 V	All			±10	μA
ON CHARACTERISTICS							
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA V_{GS} = V_{DS}, I_D = −250 μA	Q1 Q2	0.4 −0.4	0.7 −0.6	1.0 −1.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25°C	Q1 Q2		−3 2		mV/°C
$r_{DS(on)}$	Drain to Source On Resistance	V_{GS} = 4.5 V, I_D = 3.4 A V_{GS} = 2.5 V, I_D = 2.9 A V_{GS} = 1.8 V, I_D = 2.5 A V_{GS} = 1.5 V, I_D = 2.1 A V_{GS} = 4.5 V, I_D = 3.4 A, T_J = 125°C	Q1		55 68 85 106 76	66 86 113 160 112	mΩ
		V_{GS} = −4.5 V, I_D = −2.3 A V_{GS} = −2.5 V, I_D = −1.8 A V_{GS} = −1.8 V, I_D = −1.5 A V_{GS} = −1.5 V, I_D = −1.2 A V_{GS} = −4.5 V, I_D = −2.3 A , T_J = 125°C	Q2		95 120 150 190 128	142 213 331 530 190	
g_{FS}	Forward Transconductance	V_{DS} = 4.5 V, I_D = 3.4 A V_{DS} = −4.5 V, I_D = −2.3 A	Q1 Q2		9 7		S
DYNAMIC CHARACTERISTICS							
C_{iss}	Input Capacitance	Q1: V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz Q2: V_{DS} = −10 V, V_{GS} = 0 V, f = 1 MHz	Q1 Q2		225 305	300 405	pF
C_{oss}	Output Capacitance		Q1 Q2		40 55	55 75	pF
C_{rss}	Reverse Transfer Capacitance		Q1 Q2		25 50	40 75	pF
SWITCHING CHARACTERISTICS							
$t_{d(on)}$	Turn−On Delay Time	Q1: V_{DD} = 10 V, I_D = 1 A, V_{GS} = 4.5V, R_{GEN} = 6 Ω Q2: V_{DD} = −10 V, I_D = −1 A, V_{GS} = −4.5 V, R_{GEN} = 6 Ω	Q1 Q2		4.5 4.7	10 10	ns
t_r	Rise Time		Q1 Q2		2.0 4.8	10 10	
$t_{d(off)}$	Turn−Off Delay Time		Q1 Q2		15 33	27 53	
t_f	Fall Time		Q1 Q2		1.7 16	10 29	
Q_g	Total Gate Charge	Q1: V_{DD} = 10 V, I_D = 3.4 A, V_{GS} = 4.5 V Q2: V_{DD} = −10 V, I_D = −2.3 A, V_{GS} = −4.5 V	Q1 Q2		3 5.5	4.2 7.7	nC
Q_{gs}	Gate to Source Gate Charge		Q1 Q2		0.4 0.6		
Q_{gd}	Gate to Drain “Miller” Charge		Q1 Q2		0.6 1.4		

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

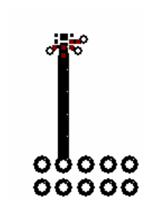
Symbol	Parameter	Test Conditions	Type	Min.	Typ.	Max.	Units
DRAIN−SOURCE DIODE CHARACTERISTICS T_J = 25°C unless otherwise noted.							
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 0.9 A (Note 2) V_{GS} = 0 V, I_S = −0.9 A (Note 2)	Q1 Q2		0.7 −0.8	1.2 −1.2	V
t_{rr}	Reverse Recovery Time	Q1: I_F = 3.4 A, Δi/Δt = 100 A/μs	Q1 Q2		8.5 16	17 29	ns
Q_{rr}	Reverse Recovery Charge	Q2: I_F = −2.3 A, Δi/Δt = 100 A/μs	Q1 Q2		1.4 4.4	10 10	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:
1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR−4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 90 °C/W when mounted on a 1 in^2 pad of 2 oz copper



b. 195 °C/W when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0 %.
3. The diode connected between the gate and source serves only as protection ESD. No gate overvoltage rating is implied.

TYPICAL CHARACTERISTICS (Q1 N−CHANNEL) T_J = 25°C unless otherwise noted.

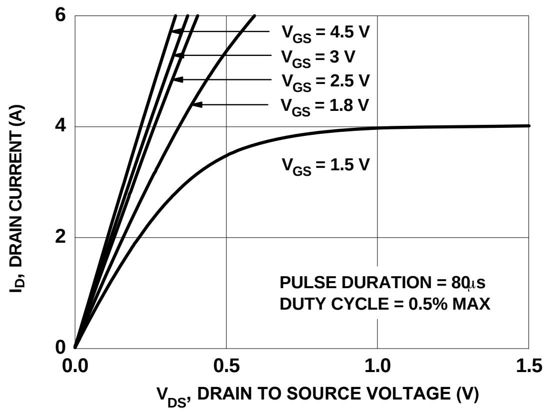


Figure 1. On-Region Characteristics

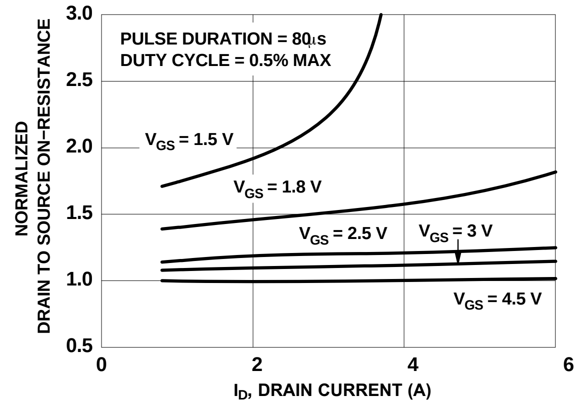


Figure 2. Normalized On−Resistance vs. Drain Current and Gate Voltage

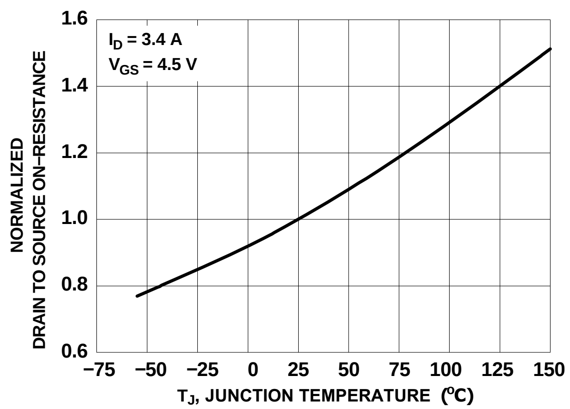


Figure 3. Normalized On Resistance vs. Junction Temperature

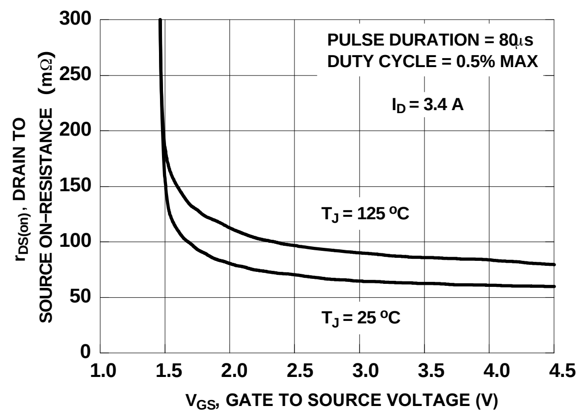


Figure 4. On−Resistance vs. Gate to Source Voltage

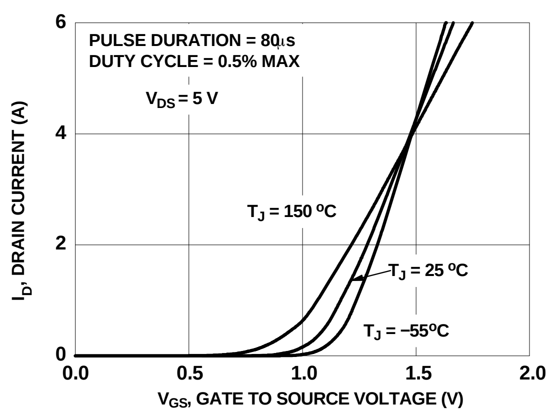


Figure 5. Transfer Characteristics

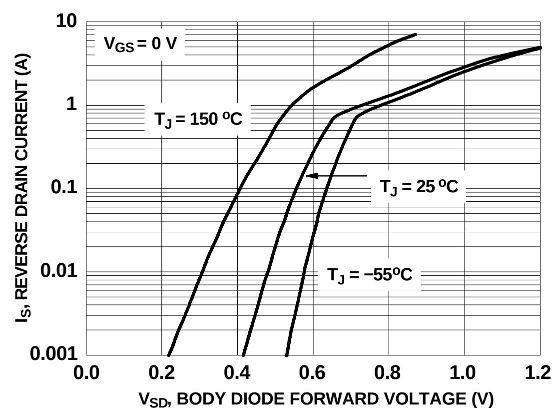


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS (Q1 N−CHANNEL) T_J = 25°C unless otherwise noted.

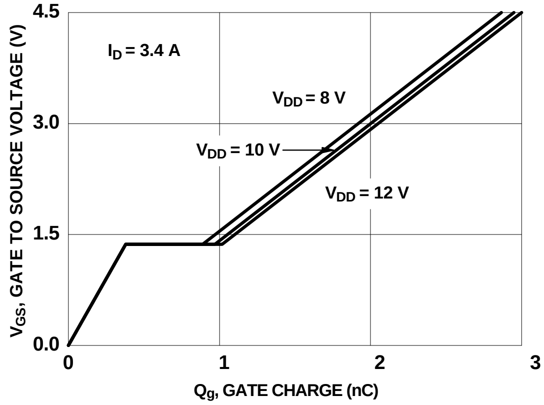


Figure 7. Gate Charge Characteristics

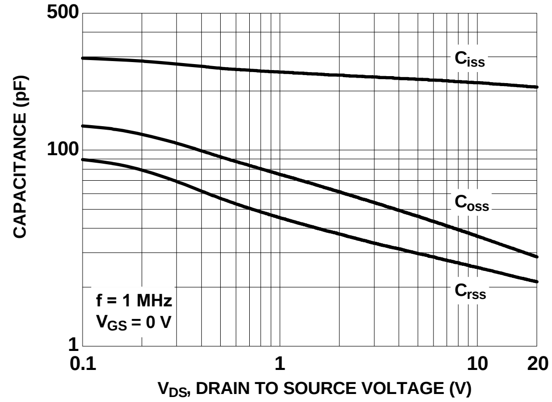


Figure 8. Capacitance vs. Drain to Source Voltage

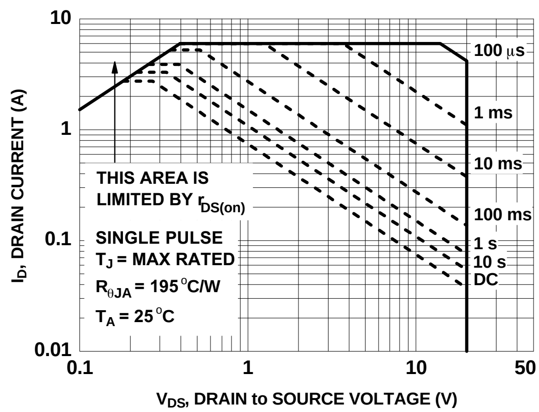


Figure 9. Forward Bias Safe Operating Area

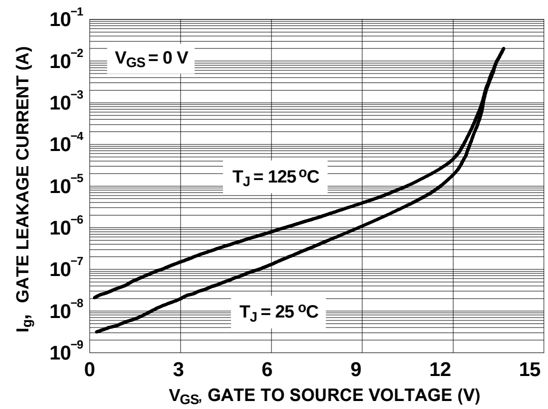


Figure 10. Gate Leakage Current vs. Gate to Source Voltage

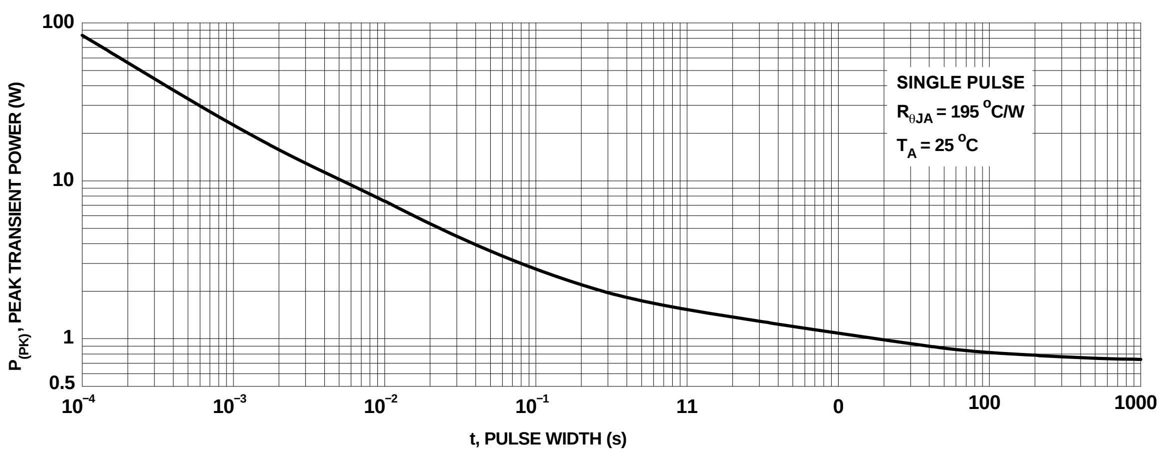


Figure 11. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS (Q1 N−CHANNEL) T_J = 25°C unless otherwise noted.

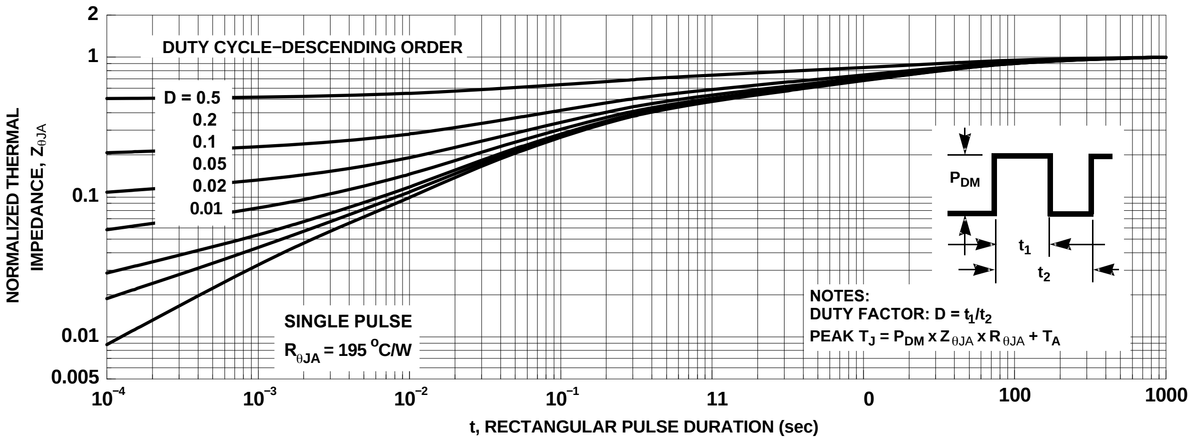


Figure 12. Junction−to−Ambient Transient Thermal Response Curve

TYPICAL CHARACTERISTICS (Q2 P−CHANNEL) T_J = 25°C unless otherwise noted.

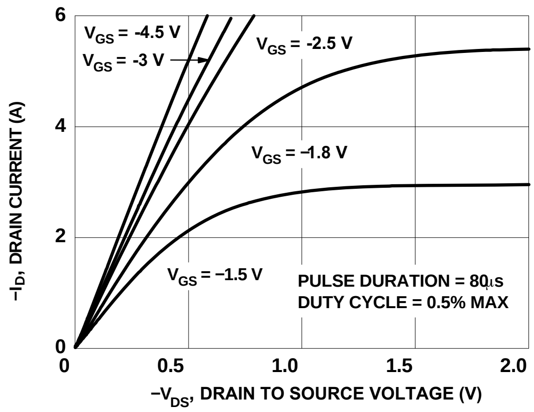


Figure 13. On-Region Characteristics

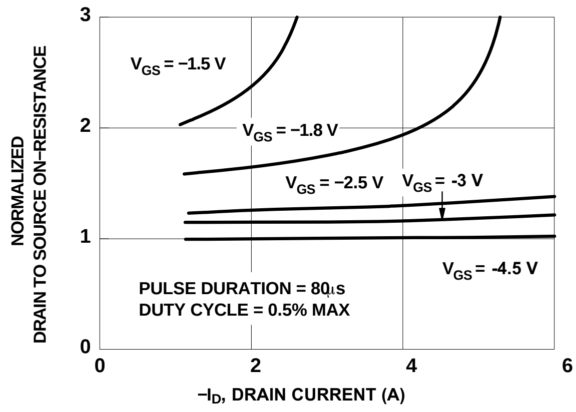


Figure 14. Normalized On−Resistance vs. Drain Current and Gate Voltage

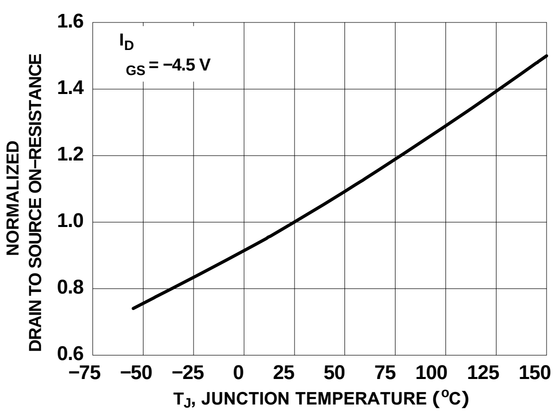


Figure 15. Normalized On−Resistance vs. Junction Temperature

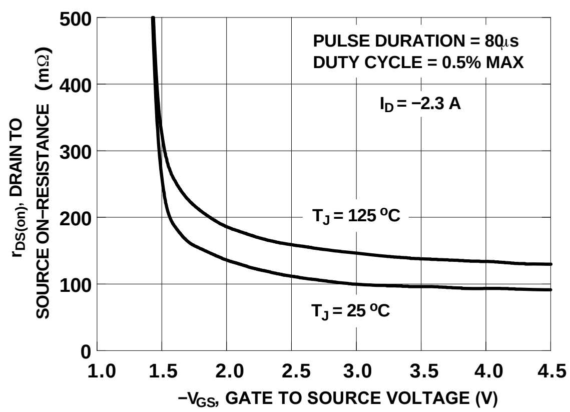


Figure 16. On Resistance vs. Gate to Source Voltage

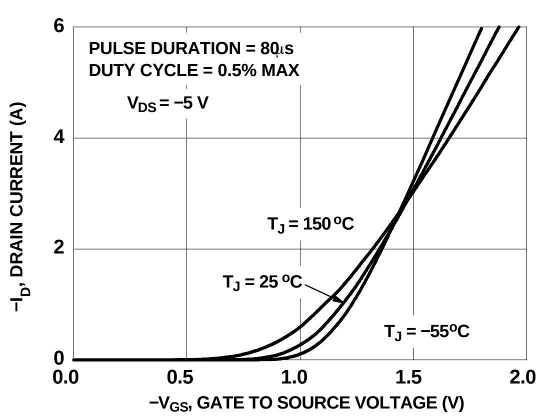


Figure 17. Transfer Characteristics

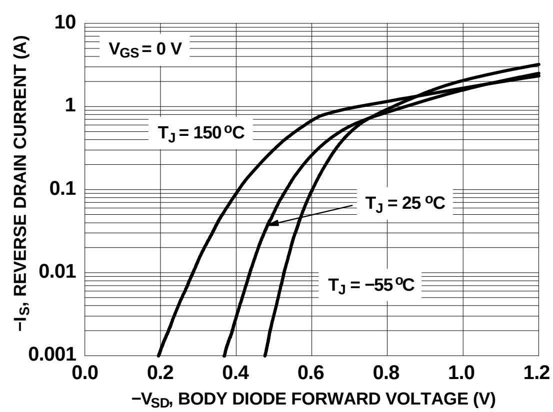


Figure 18. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS (Q2 N−CHANNEL) T_J = 25°C unless otherwise noted.

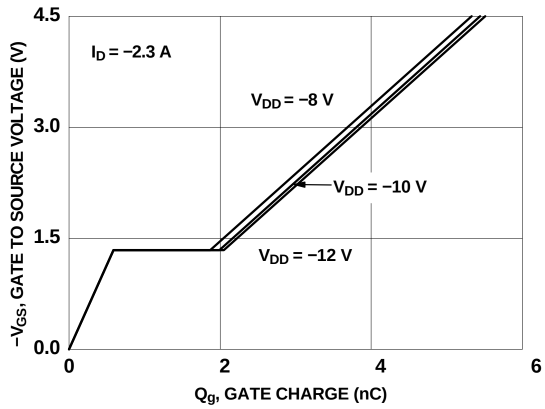


Figure 19. Gate Charge Characteristics

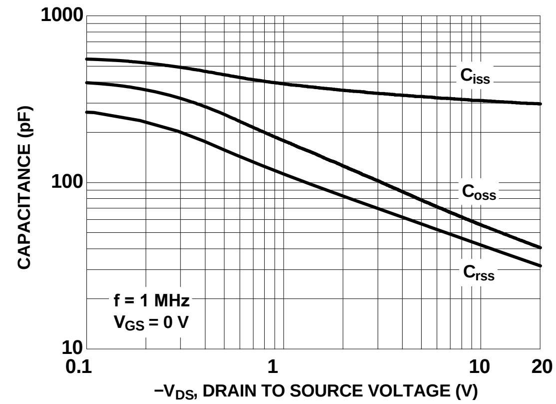


Figure 20. Capacitance vs. Drain to Source Voltage

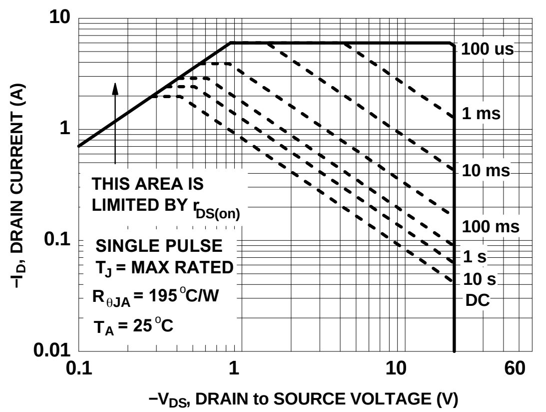


Figure 21. Forward Bias Safe Operating Area

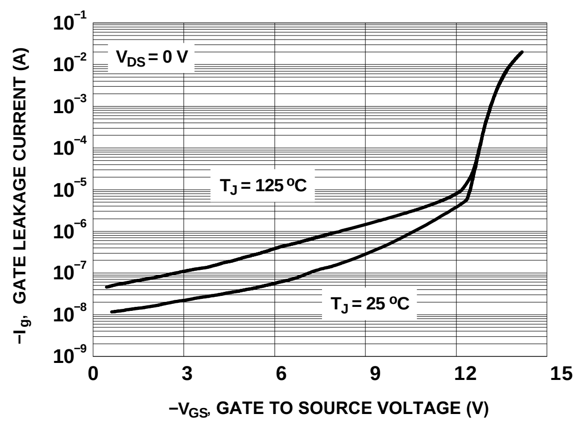


Figure 22. Gate Leakage Current vs. Gate to Source Voltage

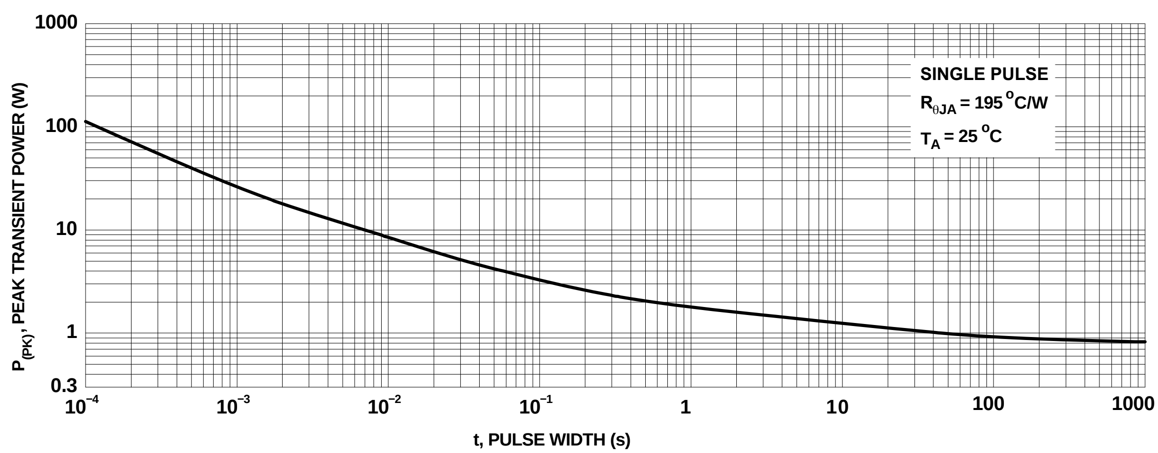


Figure 23. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS (Q2 P−CHANNEL) T_J = 25°C unless otherwise noted.

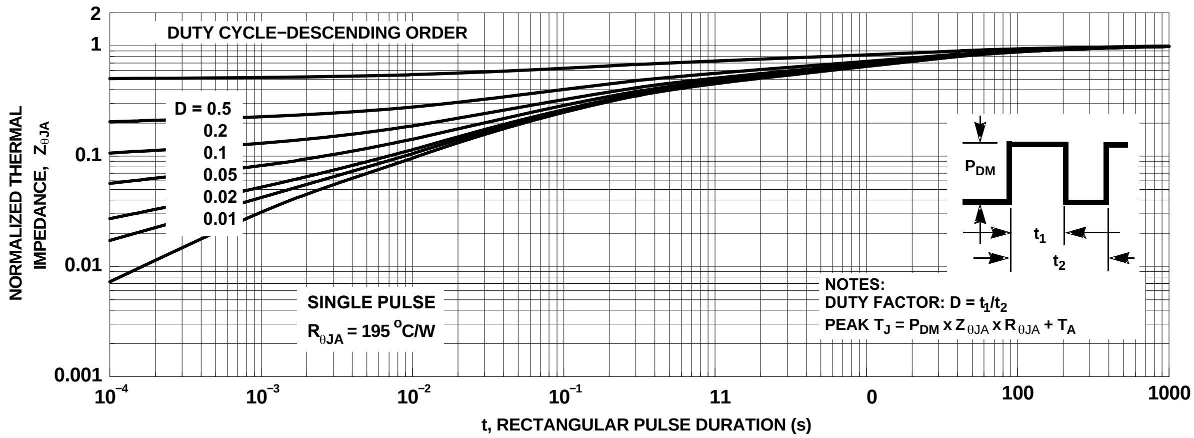


Figure 24. Junction −to−Ambient Transient Thermal Response Curve

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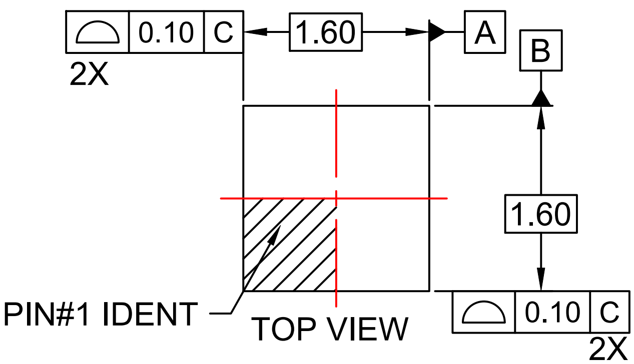
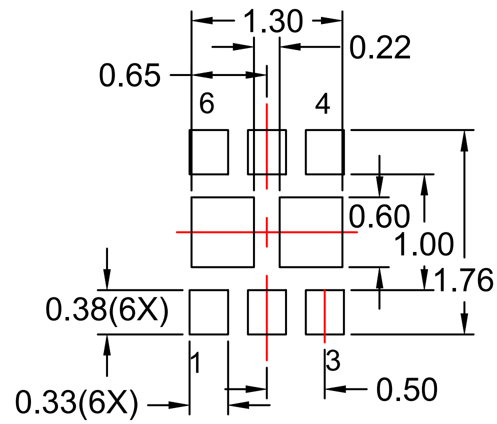
CASE 517DW
ISSUE O

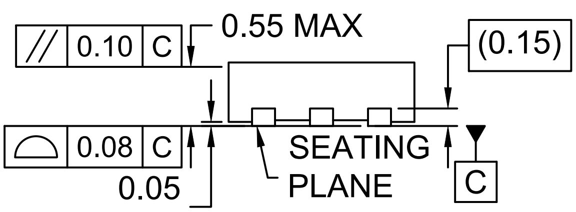
DATE 31 OCT 2016



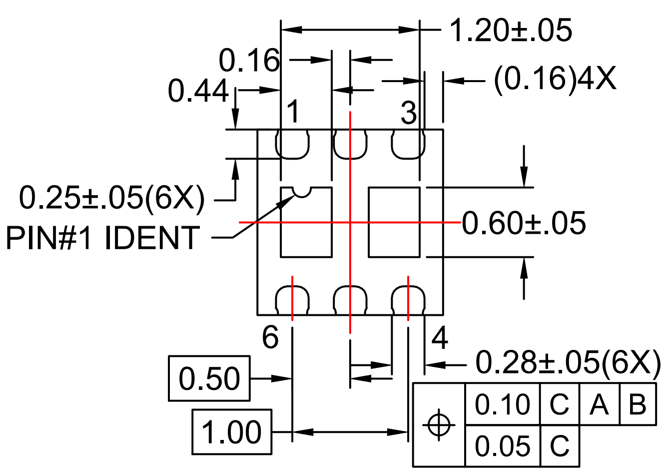
TOP VIEW



RECOMMENDED
LAND PATTERN



SIDE VIEW



BOTTOM VIEW

NOTES:

A. PACKAGE DOES NOT CONFORM TO ANY JEDEC STANDARD.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.

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DESCRIPTION:	UDFN6 1.6x1.6, 0.5P	PAGE 1 OF 1

PUBLICATION ORDERING INFORMATION

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