

MOSFET - Dual P-Channel, POWERTRENCH®

NDC7003P

General Description

These dual P-Channel Enhancement Mode Power Field Effect Transistors are produced using onsemi's proprietary Trench Technology. This very high density process has been designed to minimize on-state resistance, provide rugged and reliable performance and fast switching. This product is particularly suited to low voltage applications requiring a low current high side switch.

Features

- -0.34 A, -60 V $R_{DS(ON)} = 5 \Omega @ V_{GS} = -10 \text{ V}$
 $R_{DS(ON)} = 7 \Omega @ V_{GS} = -4.5 \text{ V}$
- Low Gate Charge
- Fast Switching Speed
- High Performance Trench Technology for Low $R_{DS(ON)}$
- SUPERSOT™ -6 Package: Small Footprint (72% smaller than standard SO-8); Low Profile (1 mm Thick)
- This is a Pb-Free Device

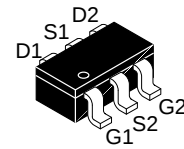
ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V _{DSS}	Drain-Source Voltage	-60	V
V _{GSS}	Gate-Source Voltage	±20	V
I _D	Drain Current - Continuous (Note 1a) - Pulsed	-0.34 -1	A
P _D	Power Dissipation for Single Operation (Note 1a) (Note 1b) (Note 1c)	0.96 0.9 0.7	W
T _J , T _{STG}	Operating and Storage Temperature Range	-55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

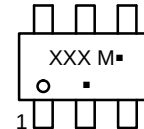
THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Unit
R _{θJA}	Thermal Resistance, Junction to Ambient (Note 1a)	130	°C/W
R _{θJC}	Thermal Resistance, Junction to Case (Note 1)	60	



TSOT23 6-Lead
CASE 419BL

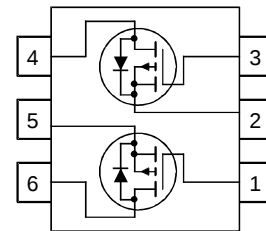
MARKING DIAGRAM



XXX = Specific Device Code
M = Date Code
▪ = Pb-Free Package

(Note: Microdot may be in either location)

PINOUT



SOT-6 (SUPERSOT™ -6)

ORDERING INFORMATION

Device	Package	Shipping†
NDC7003P	TSOT-23-6 (Pb-free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

NDC7003P

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D = -250 μA, V _{GS} = 0 V	-60			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I _D = -250 μA, Referenced to 25°C		-57		V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = -48 V, V _{GS} = 0 V			-1	μA
I _{GSS}	Gate-Body Leakage, Forward	V _{GS} = ±20 V, V _{DS} = 0 V			±100	nA

ON CHARACTERISTICS (Note 2)

V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = -250 μA	-1	-1.9	-3.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I _D = -250 μA, Referenced to 25°C		3.2		mV/°C
R _{DS(on)}	Static Drain-Source On-Resistance	V _{GS} = -10 V, I _D = -0.34 A		1.2	5	Ω
		V _{GS} = -4.5 V, I _D = -0.25 A		1.5	7.5	
		V _{GS} = -10 V, I _D = 0.34 A, T _J = 125°C		1.9	10	
I _{D(on)}	On-State Drain Current	V _{GS} = -10 V, V _{DS} = -10 V	-1			A
g _{FS}	Forward Transconductance	V _{DS} = -10 V, I _D = -0.34 A		700		mS

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	V _{DS} = -25 V, V _{GS} = 0 V, f = 1.0 MHz		66		pF
C _{oss}	Output Capacitance			13		
C _{rss}	Reverse Transfer Capacitance			6		
R _G	Gate Resistance	V _{GS} = 15 mV, f = 1.0 MHz		11.2		Ω

SWITCHING CHARACTERISTICS (Note 2)

t _{d(on)}	Turn-On Delay Time	V _{DD} = -25 V, I _D = -1 A, V _{GS} = -10 V, R _{GEN} = 6 Ω		3.2	6.4	ns
t _r	Turn-On Rise Time			10	20	
t _{d(off)}	Turn-Off Delay Time			8	16	
t _f	Turn-Off Fall Time			1	2	
Q _g	Total Gate Charge	V _{DS} = -25 V, I _D = -0.34 A, V _{GS} = -10 V		1.6	2.2	nC
Q _{gs}	Gate-Source Charge			0.3		
Q _{gd}	Gate-Drain Charge			0.3		

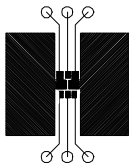
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS

I _S	Maximum Continuous Drain-Source Diode Forward Current				-0.34	A
V _{SD}	Drain-Source Diode Forward Voltage	V _{GS} = 0 V, I _S = -0.34 A (Note 2)		-0.8	-1.4	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

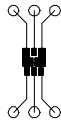
1. R_{θJA} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{θJC} is guaranteed by design while R_{θCA} is determined by the user's board design.

1a



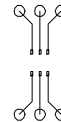
a) 130°C/W when mounted on a 0.125 in² pad of 2oz copper.

1b



b) 140°C/W when mounted on a 0.005 in² pad of 2oz copper.

1c



c) 180°C/W when mounted on a minimum pad.

Scale 1:1 on letter size paper

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0 %.

TYPICAL CHARACTERISTICS

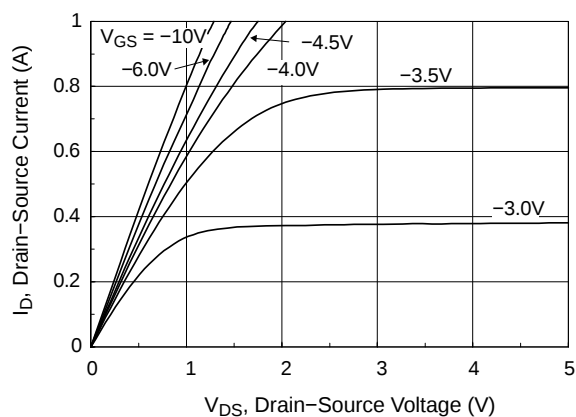


Figure 1. On-Region Characteristics

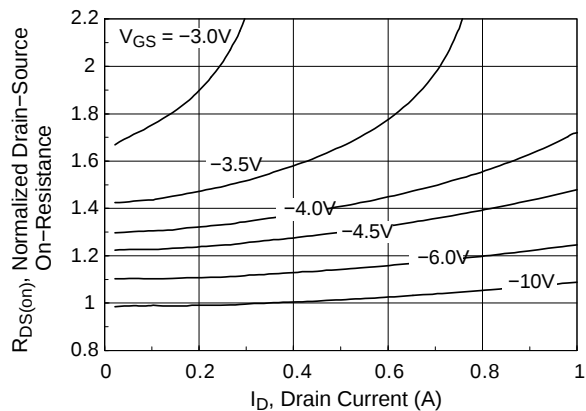


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

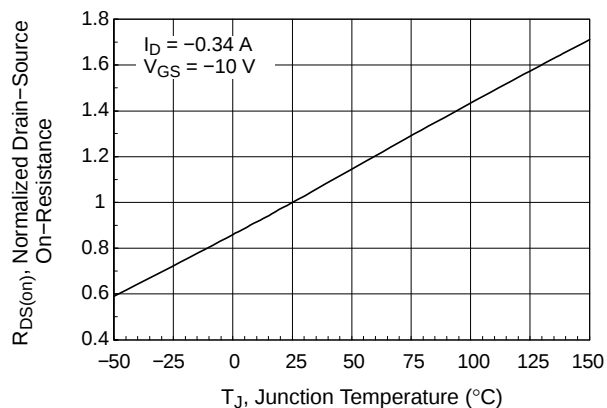


Figure 3. On-Resistance Variation with Temperature

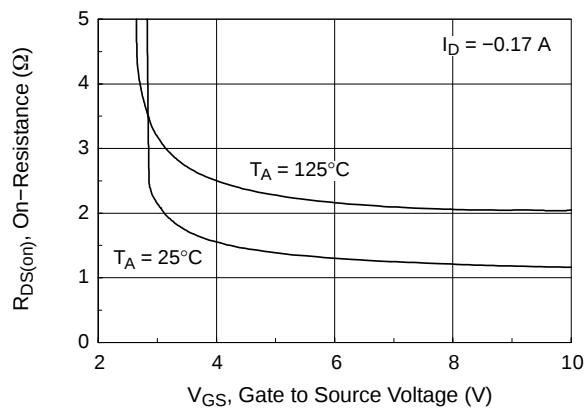


Figure 4. On-Resistance Variation with Gate-to-Source Voltage

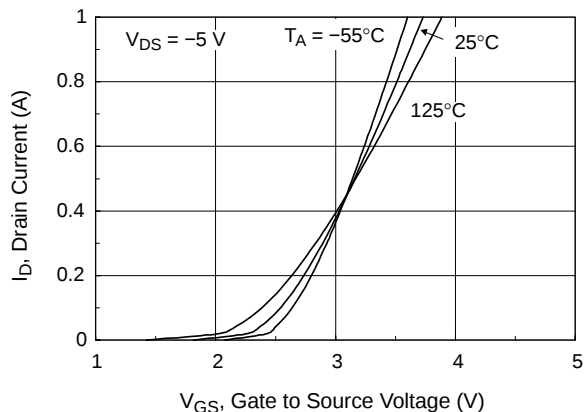


Figure 5. Transfer Characteristics

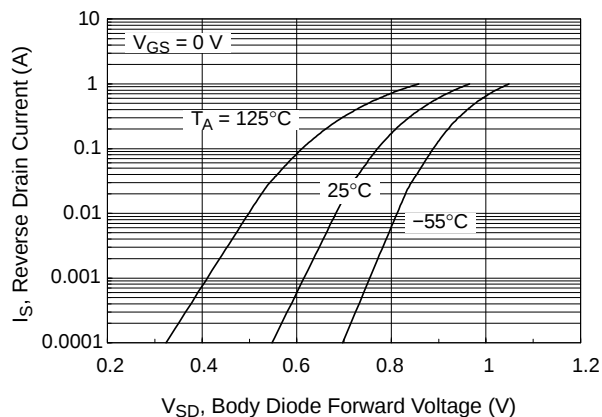


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature

TYPICAL CHARACTERISTICS

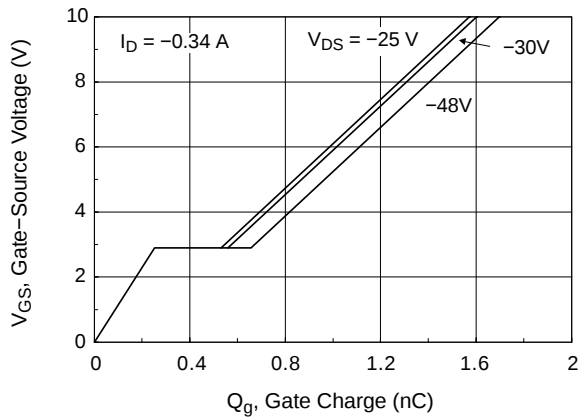


Figure 7. Gate Charge Characteristics

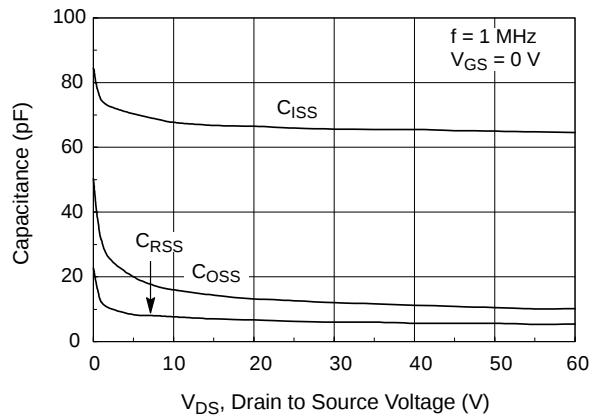


Figure 8. Capacitance Characteristics

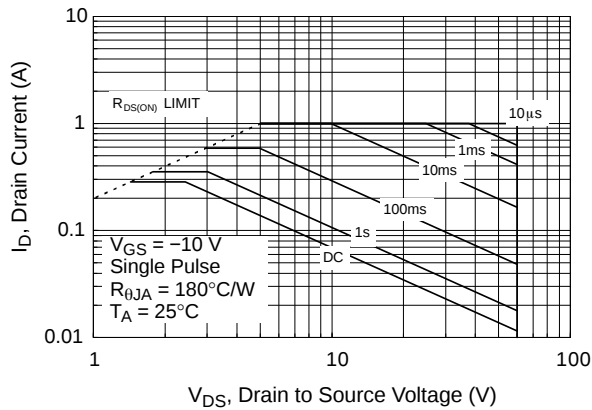


Figure 9. Maximum Safe Operating Area

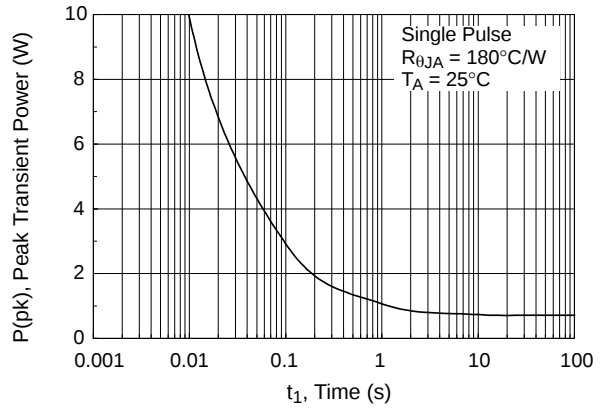


Figure 10. Single Pulse Maximum Power Dissipation

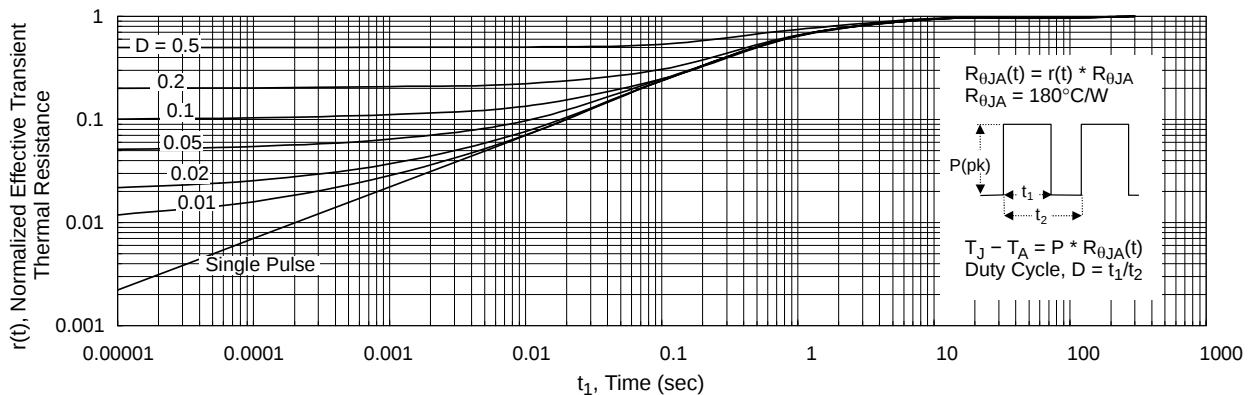


Figure 11. Transient Thermal Response Curve

(Note: Thermal characterization performed using the conditions described in Note 1c.

Transient thermal response will change depending on the circuit board design.)

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

ON Semiconductor®

ON



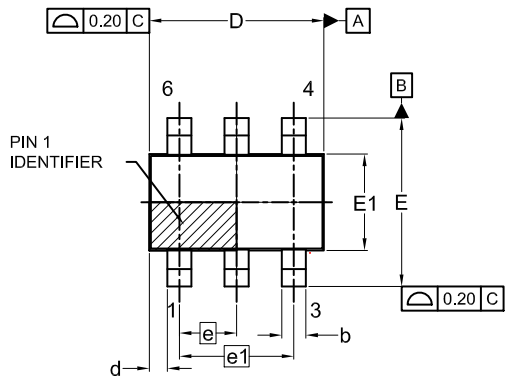
SCALE 2:1

TSOT23 6-Lead

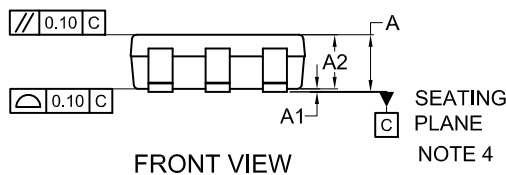
CASE 419BL

ISSUE A

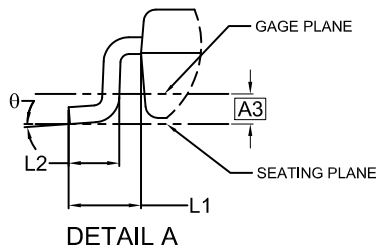
DATE 31 AUG 2020



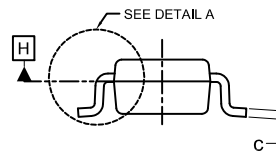
TOP VIEW



FRONT VIEW

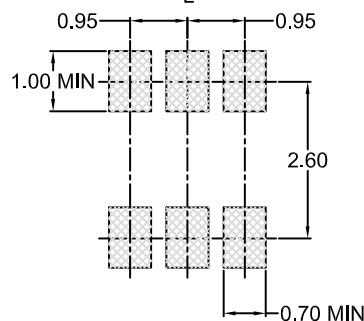


DETAIL A



SIDE VIEW

SYMM



LAND PATTERN
RECOMMENDATION

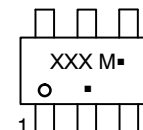
*FOR ADDITIONAL INFORMATION ON OUR
PB-FREE STRATEGY AND SOLDERING DETAILS,
PLEASE DOWNLOAD THE ON SEMICONDUCTOR
SOLDERING AND MOUNTING TECHNIQUES
REFERENCE MANUAL, SOLDERRM/D.

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.25MM PER END. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
4. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	0.05	0.10
A2	0.70	0.85	1.00
A3	0.25 BSC		
b	0.25	0.38	0.50
c	0.10	0.18	0.26
D	2.80	2.95	3.10
d	0.30 REF		
E	2.50	2.75	3.00
E1	1.30	1.50	1.70
e	0.95 BSC		
e1	1.90 BSC		
L1	0.60 REF		
L2	0.20	0.40	0.60
Θ	0°	—	10°

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code

M = Date Code

▪ = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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