

NTQD6866R2

Power MOSFET 6.9 Amps, 20 Volts N-Channel TSSOP-8

Features

- New Low Profile TSSOP-8 Package
- Ultra Low $R_{DS(on)}$
- Higher Efficiency Extending Battery Life
- Logic Level Gate Drive
- Diode Exhibits High Speed, Soft Recovery
- Avalanche Energy Specified
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperatures
- Pb-Free Package is Available

Applications

- Power Management in Portable and Battery-Powered Products, i.e.: Computers, Printers, PCMCIA Cards, Cellular and Cordless Phones
- Battery Applications
- Notebook PC

MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DS}	20	Vdc
Drain-to-Gate Voltage ($R_{GS} = 1.0\text{ M}\Omega$)	V_{DGR}	20	Vdc
Gate-to-Source Voltage – Continuous	V_{GS}	± 12	Vdc
Thermal Resistance – Single Die Junction-to-Ambient (Note 1)	$R_{\theta JA}$	62.5	$^\circ\text{C/W}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$	P_D	2.0	W
Continuous Drain Current @ $T_A = 25^\circ\text{C}$	I_D	6.9	A dc
Pulsed Drain Current (Note 4)	I_{DM}	24	A dc
Thermal Resistance – Single Die Junction-to-Ambient (Note 2)	$R_{\theta JA}$	88	$^\circ\text{C/W}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$	P_D	1.42	W
Continuous Drain Current @ $T_A = 25^\circ\text{C}$	I_D	5.8	A dc
Continuous Drain Current @ $T_A = 70^\circ\text{C}$	I_D	4.6	A dc
Pulsed Drain Current (Note 4)	I_{DM}	20	A dc
Thermal Resistance – Single Die Junction-to-Ambient (Note 3)	$R_{\theta JA}$	132	$^\circ\text{C/W}$
Total Power Dissipation @ $T_A = 25^\circ\text{C}$	P_D	0.94	W
Continuous Drain Current @ $T_A = 25^\circ\text{C}$	I_D	4.7	A dc
Continuous Drain Current @ $T_A = 70^\circ\text{C}$	I_D	3.8	A dc
Pulsed Drain Current (Note 4)	I_{DM}	14	A dc
Operating and Storage Temperature Range	T_J, T_{stg}	-55 to $+150$	$^\circ\text{C}$
Single Pulse Drain-to-Source Avalanche Energy – Starting $T_J = 25^\circ\text{C}$ ($V_{DD} = 20\text{ Vdc}$, $V_{GS} = 5.0\text{ Vdc}$, Peak $I_L = 5.5\text{ Apk}$, $L = 10\text{ mH}$, $R_G = 25\text{ }\Omega$)	E_{AS}	150	mJ
Maximum Lead Temperature for Soldering Purposes for 10 seconds	T_L	260	$^\circ\text{C}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

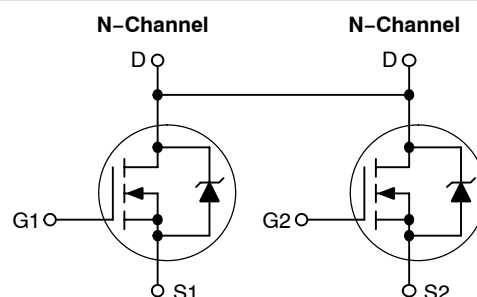
1. Mounted onto a 2" square FR-4 board
(1 in sq, 2 oz Cu 0.06" thick single-sided), $t < 10$ seconds.
2. Mounted onto a 2" square FR-4 board
(1 in sq, 2 oz Cu 0.06" thick single-sided), $t = ss$.
3. Minimum FR-4 or G-10 PCB, $t = \text{steady state}$.
4. Pulse Test: Pulse Width = 300 μs , Duty Cycle = 2%.



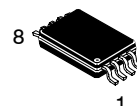
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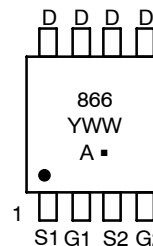
**6.9 AMPERES
20 VOLTS
30 m Ω @ $V_{GS} = 4.5\text{ V}$**



MARKING DIAGRAM & PIN ASSIGNMENT



**TSSOP-8
CASE 948S
PLASTIC**



866 = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
■ = Pb-Free Package

ORDERING INFORMATION

Device	Package	Shipping†
NTQD6866R2	TSSOP-8	4000/Tape & Reel
NTQD6866R2G	TSSOP-8 (Pb-Free)	4000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D

NTQD6866R2

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage (V _{GS} = 0 Vdc, I _D = 250 μAdc) Temperature Coefficient (Positive)	V _{(BR)DSS}	20 –	– 18.5	– –	Vdc mV/°C
Zero Gate Voltage Drain Current (V _{GS} = 0 Vdc, V _{DS} = 20 Vdc, T _J = 25°C) (V _{GS} = 0 Vdc, V _{DS} = 20 Vdc, T _J = 100°C)	I _{DSS}	– –	– –	1.0 10	μAdc
Gate-Body Leakage Current (V _{GS} = ±12 Vdc, V _{DS} = 0 Vdc)	I _{GSS}	–	–	±100	nAdc

ON CHARACTERISTICS

Gate Threshold Voltage (V _{DS} = V _{GS} , I _D = 250 μAdc) Temperature Coefficient (Negative)	V _{GS(th)}	0.6 –	0.9 –2.7	1.2 –	Vdc mV/°C
Static Drain-to-Source On-State Resistance (V _{GS} = 4.5 Vdc, I _D = 6.9 Adc) (V _{GS} = 4.5 Vdc, I _D = 5.8 Adc) (V _{GS} = 2.5 Vdc, I _D = 3.5 Adc) (V _{GS} = 2.5 Vdc, I _D = 2.9 Adc)	R _{DS(on)}	– – – –	0.026 0.025 0.030 0.030	0.032 0.030 0.038 0.038	Ω
Forward Transconductance (V _{DS} = 10 Vdc, I _D = 5.8 Adc)	g _{FS}	–	14	–	Mhos

DYNAMIC CHARACTERISTICS

Input Capacitance	(V _{DS} = 16 Vdc, V _{GS} = 0 Vdc, f = 1.0 MHz)	C _{iss}	–	875	1400	pF
Output Capacitance		C _{oss}	–	325	550	
Reverse Transfer Capacitance		C _{rss}	–	100	175	

SWITCHING CHARACTERISTICS (Note 5)

Turn-On Delay Time	(V _{DD} = 16 Vdc, I _D = 5.8 Adc, V _{GS} = 4.5 Vdc, R _G = 6.0 Ω)	t _{d(on)}	–	10	18	ns
Rise Time		t _r	–	45	80	
Turn-Off Delay Time		t _{d(off)}	–	40	75	
Fall Time		t _f	–	90	150	
Turn-On Delay Time	(V _{DD} = 16 Vdc, I _D = 5.8 Adc, V _{GS} = 4.5 Vdc, R _G = 3.0 Ω)	t _{d(on)}	–	8.0	–	
Rise Time		t _r	–	45	–	
Turn-Off Delay Time		t _{d(off)}	–	35	–	
Fall Time		t _f	–	75	–	
Gate Charge	(V _{DS} = 16 Vdc, V _{GS} = 4.5 Vdc, I _D = 5.8 Adc)	Q _{tot}	–	13	22	nC
		Q _{gs}	–	1.8	–	
		Q _{gd}	–	4.5	–	

BODY-DRAIN DIODE RATINGS

Forward On-Voltage	(I _S = 5.8 Adc, V _{GS} = 0 Vdc) (I _S = 5.8 Adc, V _{GS} = 0 Vdc, T _J = 100°C)	V _{SD}	– –	0.85 0.75	1.0 –	Vdc
Reverse Recovery Time	(I _S = 5.8 Adc, V _{GS} = 0 Vdc, V _{DS} = 20 Vdc dI _S /dt = 100 A/μs)	t _{rr}	–	23	–	ns
		t _b	–	11	–	
		t _a	–	12	–	
Reverse Recovery Stored Charge		Q _{RR}	–	0.013	–	μC

5. Switching characteristics are independent of operating junction temperature.

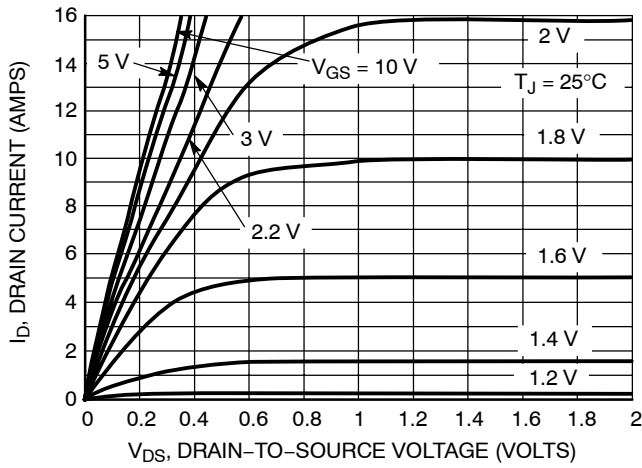


Figure 1. On-Region Characteristics

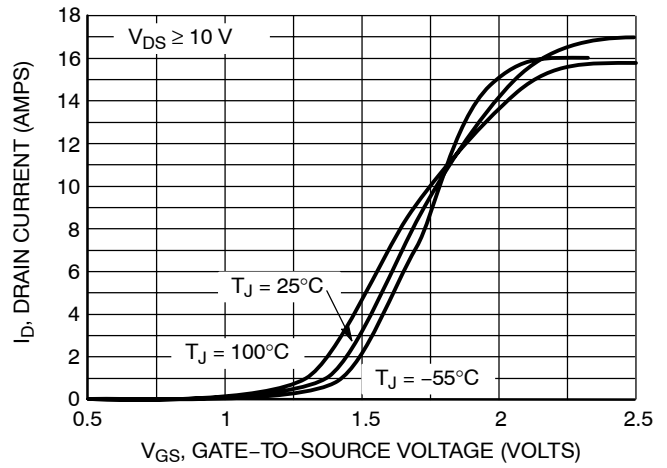


Figure 2. Transfer Characteristics

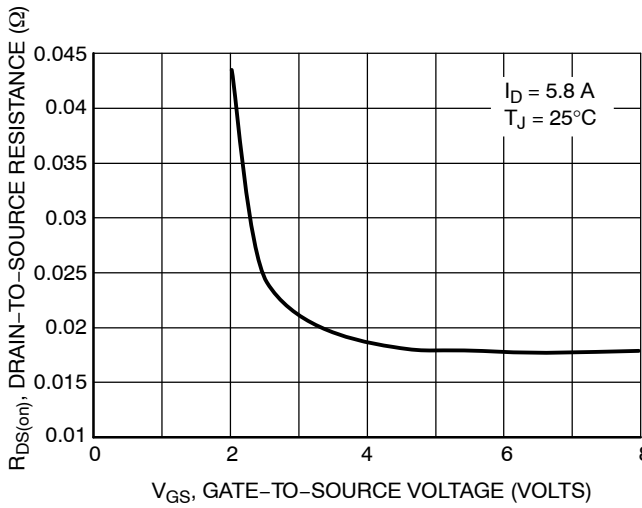


Figure 3. On-Resistance versus Gate-to-Source Voltage

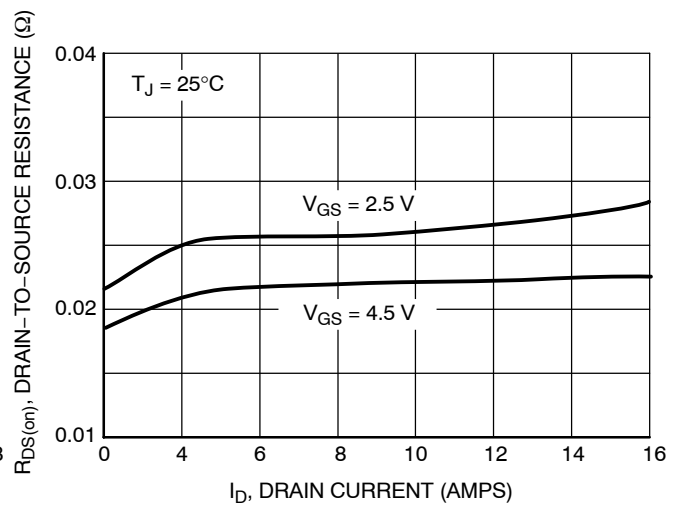


Figure 4. On-Resistance versus Drain Current and Gate Voltage

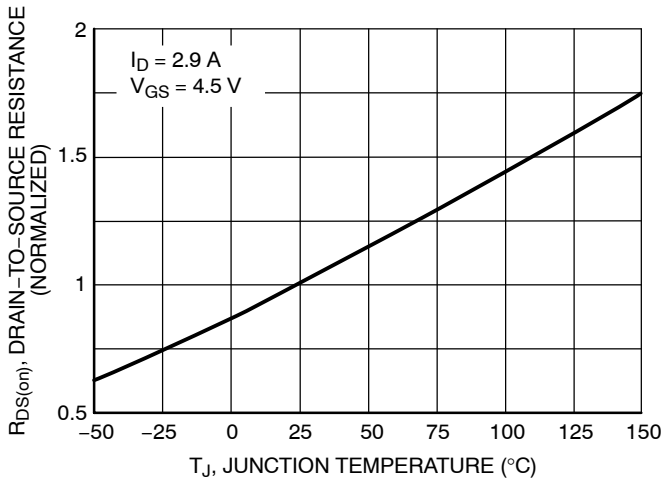


Figure 5. On-Resistance Variation with Temperature

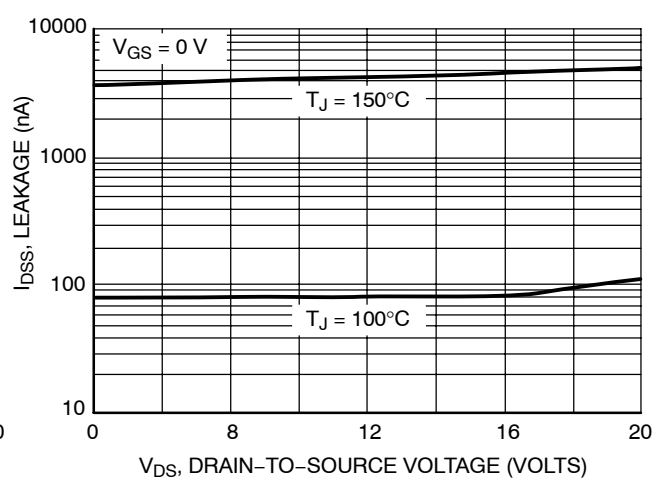


Figure 6. Drain-to-Source Leakage Current versus Voltage

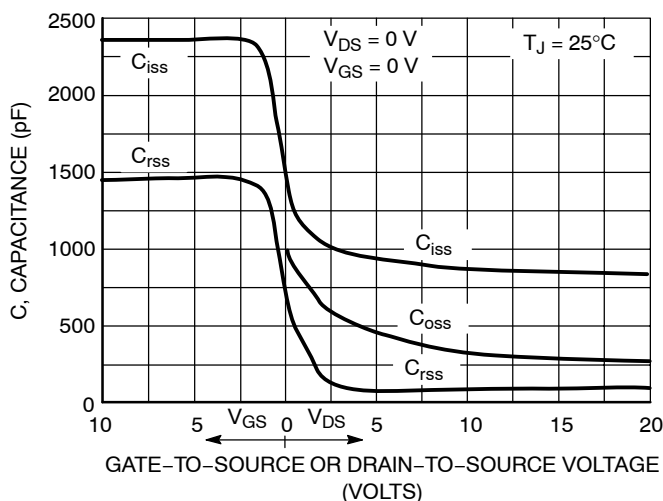


Figure 7. Capacitance Variation

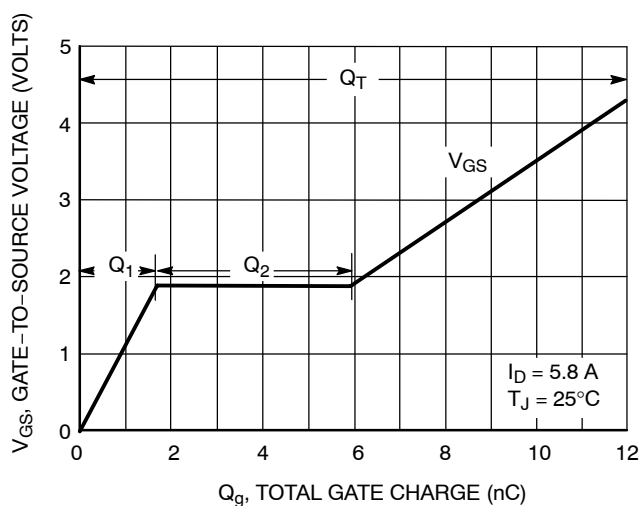


Figure 8. Gate-to-Source Voltage versus Total Charge

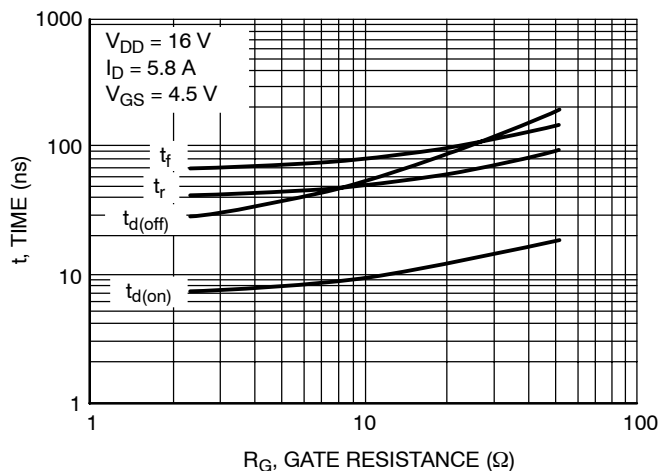


Figure 9. Resistive Switching Time Variation versus Gate Resistance

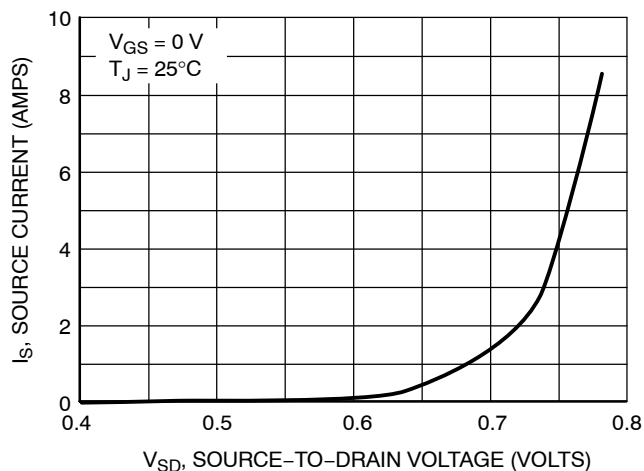


Figure 10. Diode Forward Voltage versus Current

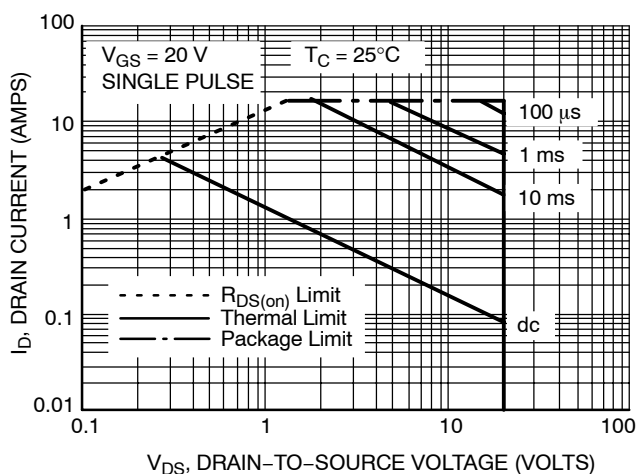


Figure 11. Maximum Rated Forward Biased Safe Operating Area

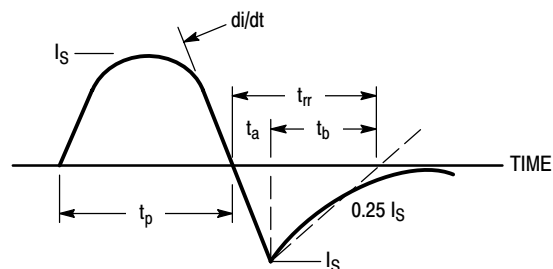


Figure 12. Diode Reverse Recovery Waveform

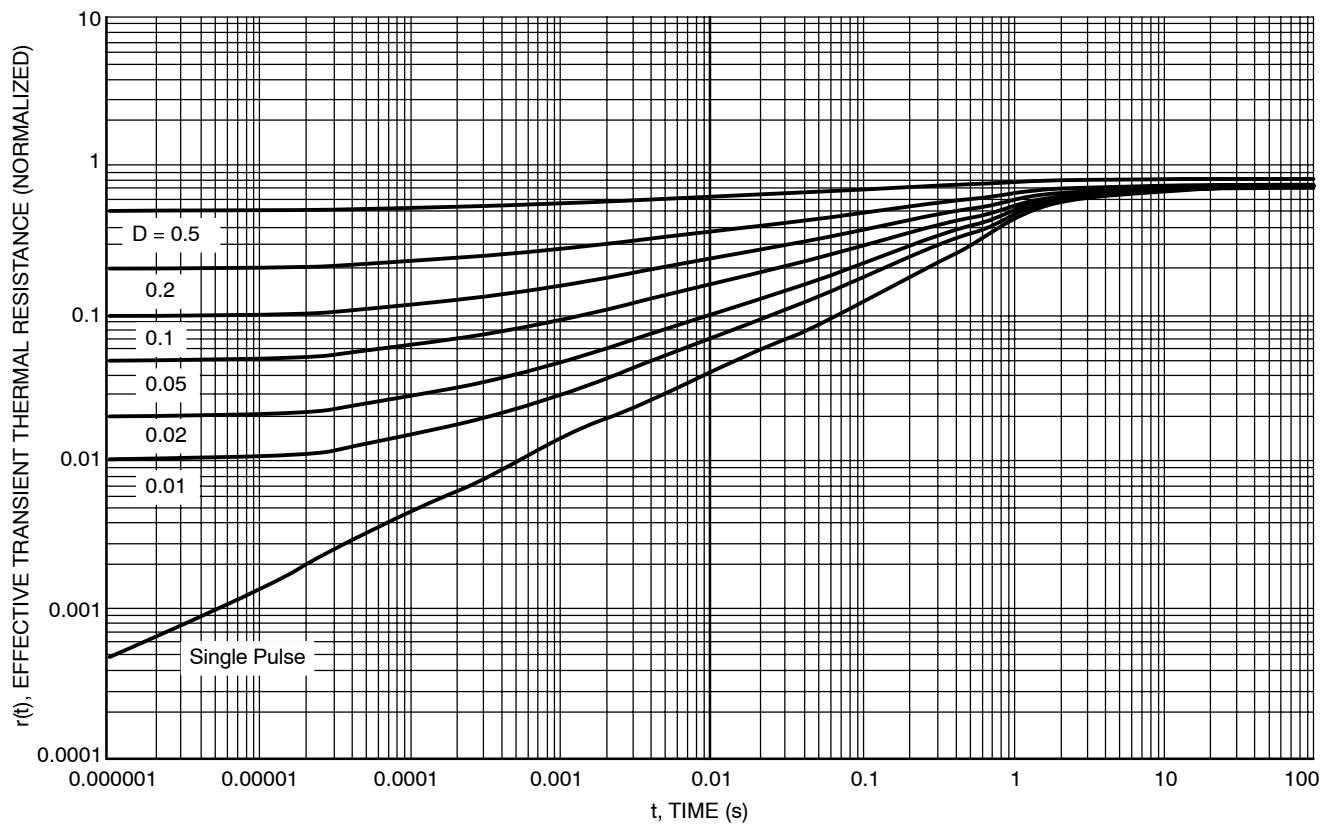


Figure 13. Thermal Response

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

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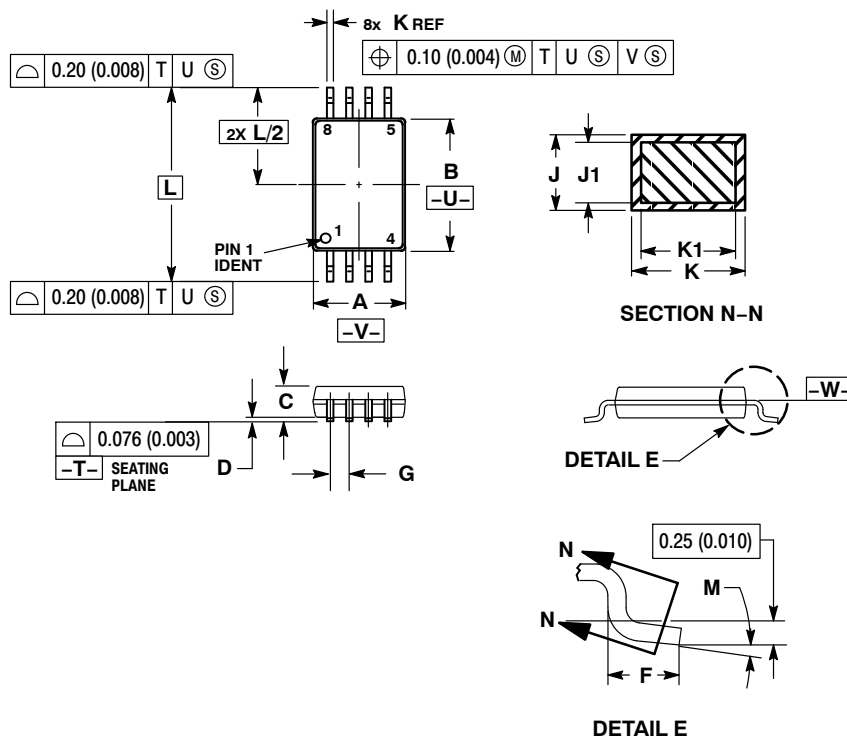
ON



SCALE 2:1

TSSOP-8
CASE 948S-01
ISSUE C

DATE 20 JUN 2008

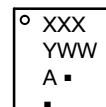


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	4.30	4.50	0.169	0.177
C	---	1.10	---	0.043
D	0.05	0.15	0.002	0.006
F	0.50	0.70	0.020	0.028
G	0.65 BSC		0.026 BSC	
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

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