

NTMD5836NL

Power MOSFET

40 V, Dual N-Channel, SOIC-8

Features

- Asymmetrical N Channels
- Low $R_{DS(on)}$
- Low Capacitance
- Optimized Gate Charge
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

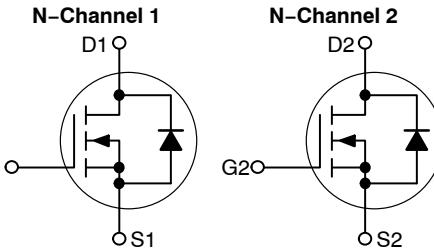
	$V_{(BR)DSS}$	$R_{DS(on)}$ Max	I_D Max (Notes 1 and 2)
Channel 1	40 V	12 m Ω @ 10 V	11 A
		16 m Ω @ 4.5 V	
Channel 2	40 V	20 m Ω @ 10 V	6.5 A
		36.5 m Ω @ 4.5 V	

1. Surface-mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces)
2. Only selected channel is been powered
1W applied on channel 1: $T_J = 1 \text{ W} * 85^\circ\text{C/W} + 25^\circ\text{C} = 110^\circ\text{C}$

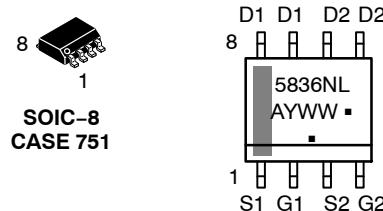


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MARKING DIAGRAM* AND PIN ASSIGNMENT



A = Assembly Location

Y = Year

WW = Work Week

▪ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping [†]
NTMD5836NLR2G	SOIC-8 (Pb-Free)	2500 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D

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MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise stated)

Parameter	Symbol	Ch 1	Ch 2	Unit
Drain-to-Source Voltage	V_{DSS}	40	40	V
Gate-to-Source Voltage	V_{GS}	± 20	± 20	V
Continuous Drain Current $R_{\theta JA}$ (Notes 3 and 4)	Steady State	$T_A = 25^\circ\text{C}$	I_D	9.0
		$T_A = 70^\circ\text{C}$		7.2
Power Dissipation $R_{\theta JA}$ (Notes 3 and 4)		$T_A = 25^\circ\text{C}$	P_D	1.5
		$T_A = 70^\circ\text{C}$		0.9
Continuous Drain Current $R_{\theta JA}$ (Notes 3 and 4)	$t \leq 10\text{s}$	$T_A = 25^\circ\text{C}$	I_D	11
		$T_A = 70^\circ\text{C}$		8.6
Power Dissipation $R_{\theta JA}$ (Notes 3 and 4)		$T_A = 25^\circ\text{C}$	P_D	2.1
		$T_A = 70^\circ\text{C}$		1.3
Pulsed Drain Current	$t_p = 10\ \mu\text{s}$		I_{DM}	43
Operating Junction and Storage Temperature			T_J, T_{STG}	-55 to +150
Source Current (Body Diode)			I_S	10
Single Pulse Drain-to-Source Avalanche Energy ($V_{DD} = 40\text{ V}$, $V_{GS} = 10\text{ V}$, $L = 0.1\text{ mH}$)			E_{AS}	76
			I_{AS}	39
Lead Temperature for Soldering Purposes (1/8" from case for 10s)			T_L	260

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

3. Surface-mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces)

4. Only selected channel is been powered

1W applied on channel 1: $T_J = 1\text{ W} * 85^\circ\text{C/W} + 25^\circ\text{C} = 110^\circ\text{C}$

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Ch 1	Ch 2	Unit	
Junction-to-Ambient Steady State (Notes 5 and 7)	$R_{\theta JA}$	85	86	°C/W	
Junction-to-Ambient – $t \leq 10\text{ s}$ (Notes 5 and 7)	$R_{\theta JA}$	60	65		
Junction-to-Ambient Steady State (Notes 5 and 8)	$R_{\theta JA}$	59			
Junction-to-Ambient Steady State (Notes 6 and 7)	$R_{\theta JA}$	136	136		

5. Surface-mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces)

6. Surface-mounted on FR4 board using 0.155 in sq (100 mm²) pad size

7. Only selected channel is been powered

1W applied on channel 1: $T_J = 1\text{ W} * 85^\circ\text{C/W} + 25^\circ\text{C} = 110^\circ\text{C}$

8. Both channels receive equivalent power dissipation

1 W applied on each channel: $T_J = 2\text{ W} * 59^\circ\text{C/W} + 25^\circ\text{C} = 143^\circ\text{C}$

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ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Ch	Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain-to-Source Breakdown Voltage	$V_{(\text{BR})\text{DSS}}$	$V_{\text{GS}} = 0 \text{ V}, I_{\text{D}} = 250 \mu\text{A}$	Ch 1	40			V
			Ch 2				
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(\text{BR})\text{DSS}} / T_J$		Ch 1		146		$\text{mV}/^\circ\text{C}$
			Ch 2		25		
Zero Gate Voltage Drain Current	I_{DSS}	$V_{\text{GS}} = 0 \text{ V}, V_{\text{DS}} = 40 \text{ V}$	Ch 1			1.0	μA
			Ch 2				
			Ch 1			100	
			Ch 2				
Gate-to-Source Leakage Current	I_{GSS}	$V_{\text{DS}} = 0 \text{ V}, V_{\text{GS}} = \pm 20 \text{ V}$	Ch 1			± 100	nA
			Ch 2				

ON CHARACTERISTICS (Note 9)

Gate Threshold Voltage	$V_{\text{GS}(\text{TH})}$	$V_{\text{GS}} = V_{\text{DS}}, I_{\text{D}} = 250 \mu\text{A}$	Ch 1	1.0	1.8	3.0	V
			Ch 2	1.0	1.8	3.0	
Negative Threshold Temperature Coefficient	$V_{\text{GS}(\text{TH})} / T_J$		Ch 1		6.0		$\text{mV}/^\circ\text{C}$
			Ch 2		6.0		
Drain-to-Source On Resistance	$R_{\text{DS}(\text{on})}$	$V_{\text{GS}} = 10 \text{ V}, I_{\text{D}} = 10 \text{ A}$	Ch 1		9.5	12	$\text{m}\Omega$
		$V_{\text{GS}} = 10 \text{ V}, I_{\text{D}} = 7 \text{ A}$	Ch 2		16.2	20	
		$V_{\text{GS}} = 4.5 \text{ V}, I_{\text{D}} = 10 \text{ A}$	Ch 1		13	16	$\text{m}\Omega$
		$V_{\text{GS}} = 4.5 \text{ V}, I_{\text{D}} = 7 \text{ A}$	Ch 2		25.0	36.5	
Forward Transconductance	g_{FS}	$V_{\text{DS}} = 15 \text{ V}, I_{\text{D}} = 10 \text{ A}$	Ch 1		10.5		S
		$V_{\text{DS}} = 15 \text{ V}, I_{\text{D}} = 7 \text{ A}$	Ch 2		6.0		

CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	C_{ISS}	$V_{\text{GS}} = 0 \text{ V}, f = 1 \text{ MHz}, V_{\text{DS}} = 20 \text{ V}$	Ch 1		2120		pF	
			Ch 2		730			
Output Capacitance	C_{OSS}		Ch 1		315			
			Ch 2		123			
Reverse Transfer Capacitance	C_{RSS}		Ch 1		225			
			Ch 2		84			

9. Pulse Test: pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2\%$

10. Switching characteristics are independent of operating junction temperatures

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ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Ch	Min	Typ	Max	Unit
CHARGES, CAPACITANCES & GATE RESISTANCE							
Total Gate Charge	$Q_{G(\text{TOT})}$	$V_{GS} = 10\text{ V}$, $V_{DS} = 20\text{ V}$, $I_D = 10\text{ A}$	Ch 1		36	50	nC
		$V_{GS} = 10\text{ V}$, $V_{DS} = 20\text{ V}$, $I_D = 7\text{ A}$	Ch 2		16		
		$V_{GS} = 4.5\text{ V}$, $V_{DS} = 20\text{ V}$, CH1: $I_D = 10\text{ A}$, CH2: $I_D = 7\text{ A}$	Ch 1		15	23	
			Ch 2		8.5	11	
			Ch 1		2.4		
			Ch 2		1.0		
Threshold Gate Charge	$Q_{G(\text{TH})}$	$V_{GS} = 4.5\text{ V}$, $V_{DS} = 20\text{ V}$, CH1: $I_D = 10\text{ A}$, CH2: $I_D = 7\text{ A}$	Ch 1		6.9		V
			Ch 2		2.8		
			Ch 1		7.2		
			Ch 2		4.0		
Gate-to-Source Charge	Q_{GS}	$V_{GS} = 4.5\text{ V}$, $V_{DS} = 20\text{ V}$, CH1: $I_D = 10\text{ A}$, CH2: $I_D = 7\text{ A}$	Ch 1		3.2		Ω
			Ch 2		3.3		
Gate-to-Drain Charge	Q_{GD}	$V_{GS} = 4.5\text{ V}$, $V_{DS} = 20\text{ V}$, CH1: $I_D = 10\text{ A}$, CH2: $I_D = 7\text{ A}$	Ch 1		1.2		Ω
			Ch 2		2.1		

SWITCHING CHARACTERISTICS (Note 10)

Turn-On Delay Time	$t_{d(\text{ON})}$	$V_{GS} = 4.5\text{ V}$, $V_{DD} = 20\text{ V}$, CH1: $I_D = 10\text{ A}$, CH2: $I_D = 7\text{ A}$, $R_G = 2.5\text{ Ω}$	Ch 1		16		ns	
Rise Time	t_r		Ch 2		11.5			
			Ch 1		22			
Turn-Off Delay Time	$t_{d(\text{OFF})}$		Ch 2		14			
			Ch 1		26			
Fall Time	t_f		Ch 2		15.5			
			Ch 1		8.5			
			Ch 2		3.5			

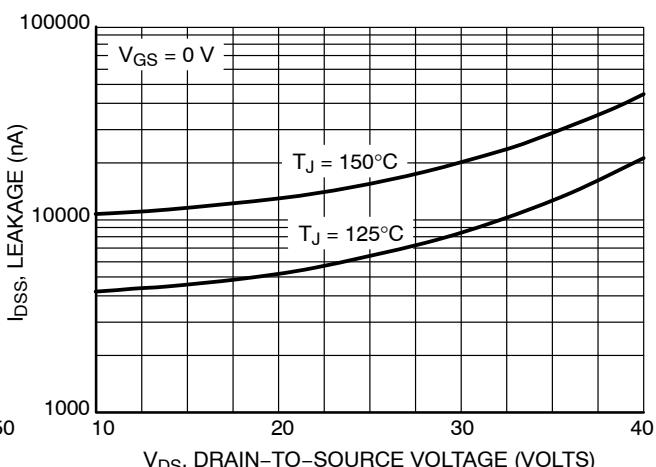
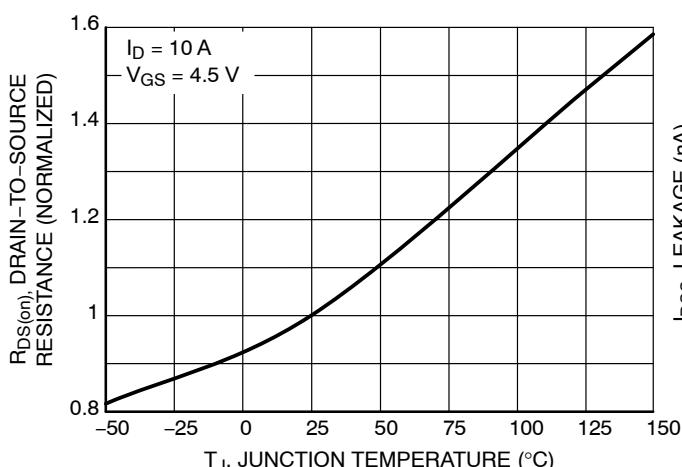
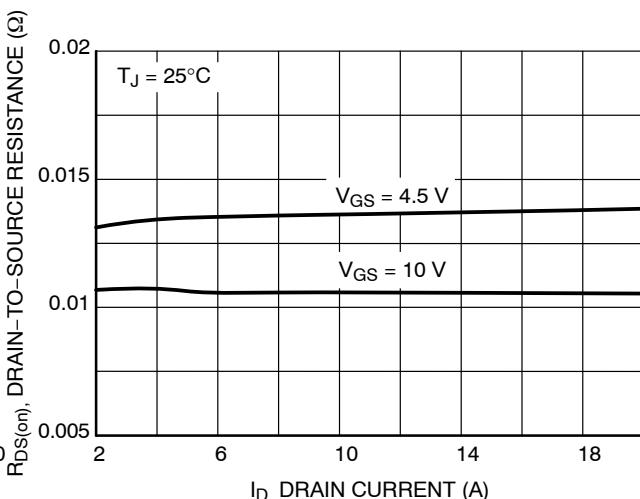
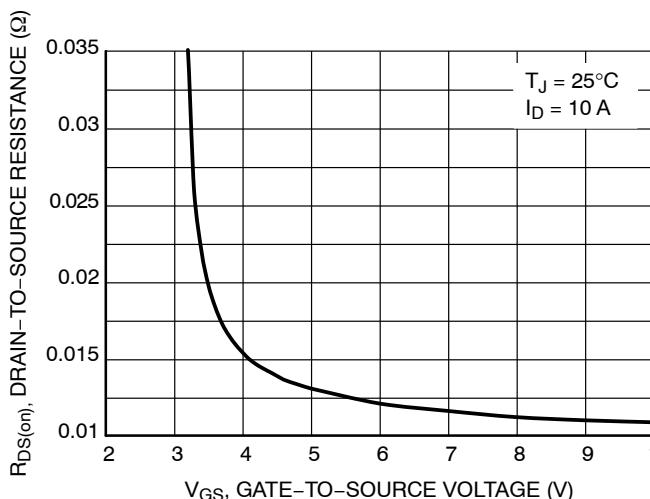
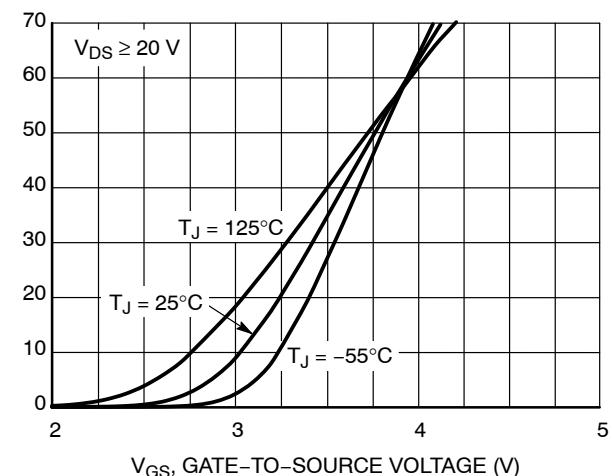
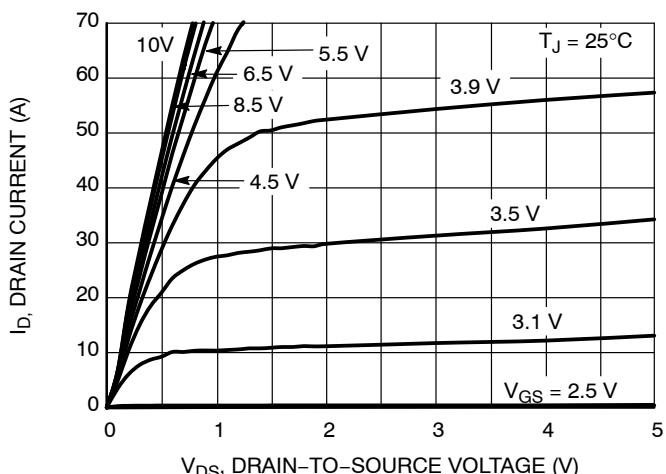
DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{GS} = 0\text{ V}$, CH1: $I_D = 10\text{ A}$, CH2: $I_D = 7\text{ A}$	$T_J = 25^\circ\text{C}$	Ch 1		0.9	1.2	V		
			Ch 2			0.85	1.2			
			$T_J = 125^\circ\text{C}$	Ch 1		0.65				
				Ch 2		0.73				
Reverse Recovery Time	t_{RR}	$V_{GS} = 0\text{ V}$, $dI_{SD}/dt = 100\text{ A}/\mu\text{s}$, CH1: $I_D = 10\text{ A}$, CH2: $I_D = 7\text{ A}$		Ch 1		27		ns		
				Ch 2		17				
Charge Time	T_a			Ch 1		14				
				Ch 2		11				
Discharge Time	T_b			Ch 1		13				
				Ch 2		6.0				
Reverse Recovery Charge	Q_{RR}			Ch 1		19		nC		
				Ch 2		9.0				

9. Pulse Test: pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$

10. Switching characteristics are independent of operating junction temperatures

TYPICAL PERFORMANCE CURVES



TYPICAL PERFORMANCE CURVES

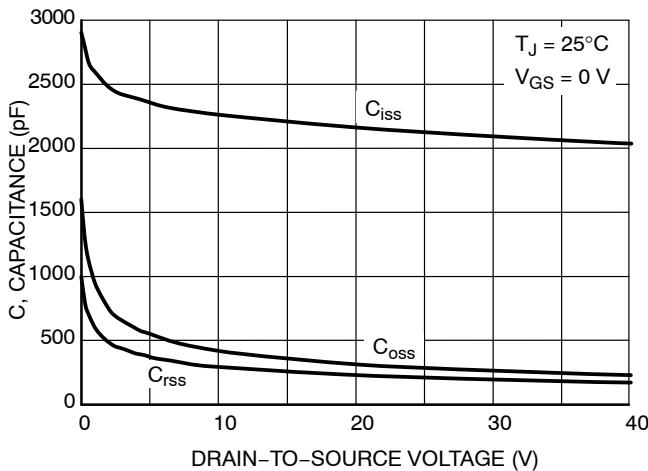


Figure 7. Capacitance Variation – Channel 1

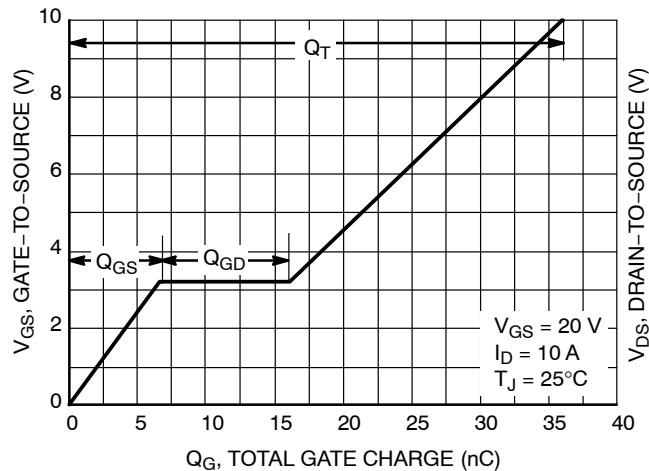


Figure 8. Gate-To-Source and Drain-To-Source Voltage vs. Total Charge – Channel 1

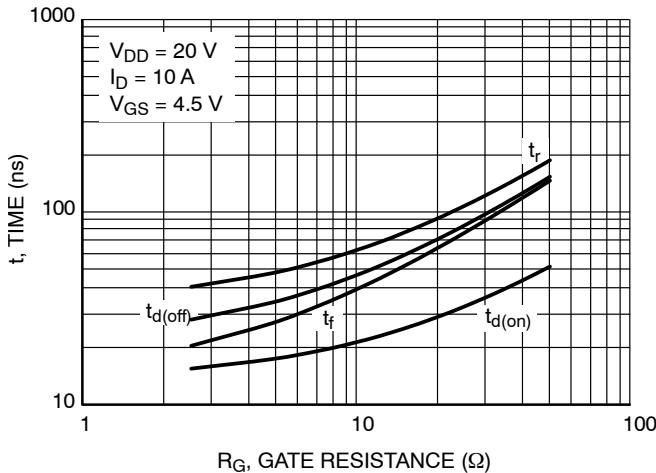


Figure 9. Resistive Switching Time Variation vs. Gate Resistance – Channel 1

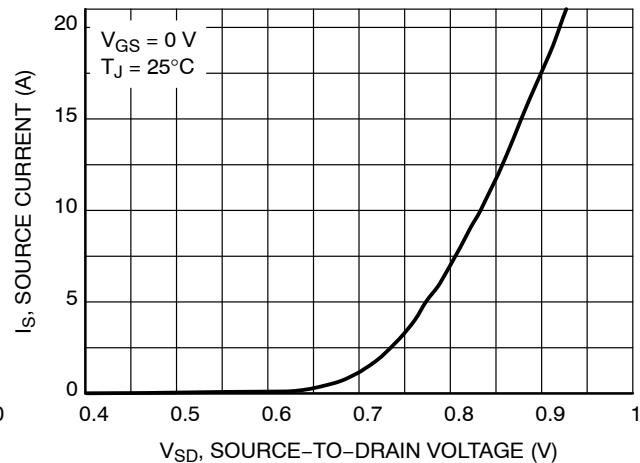


Figure 10. Diode Forward Voltage vs. Current – Channel 1

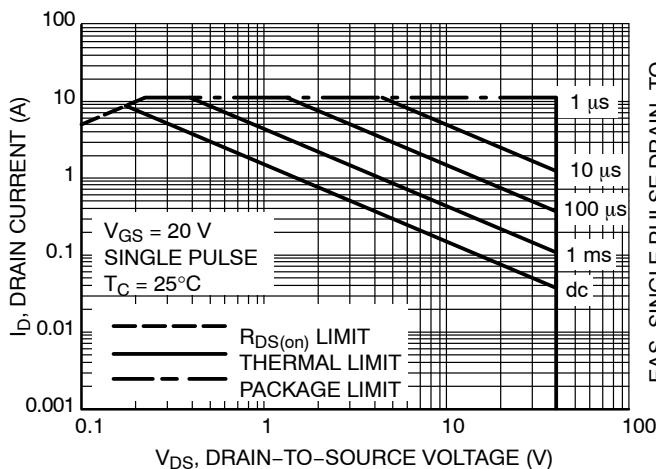


Figure 11. Maximum Rated Forward Biased Safe Operating Area – Channel 1

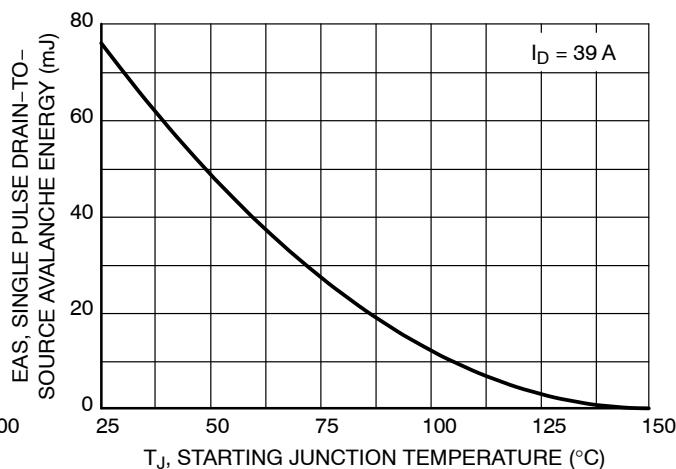


Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature – Channel 1

TYPICAL PERFORMANCE CURVES

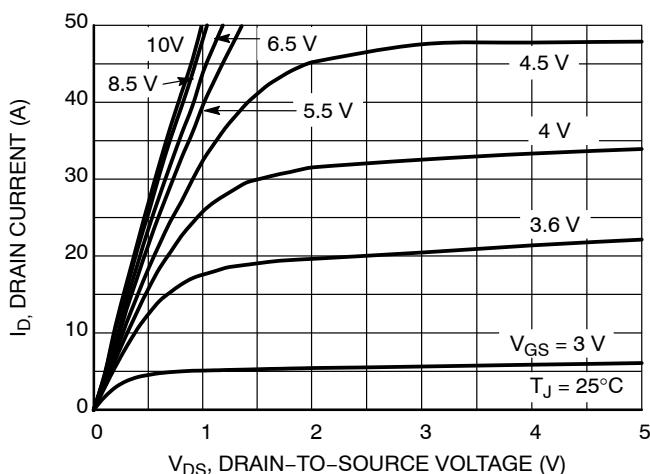


Figure 1. On-Region Characteristics – Channel 2

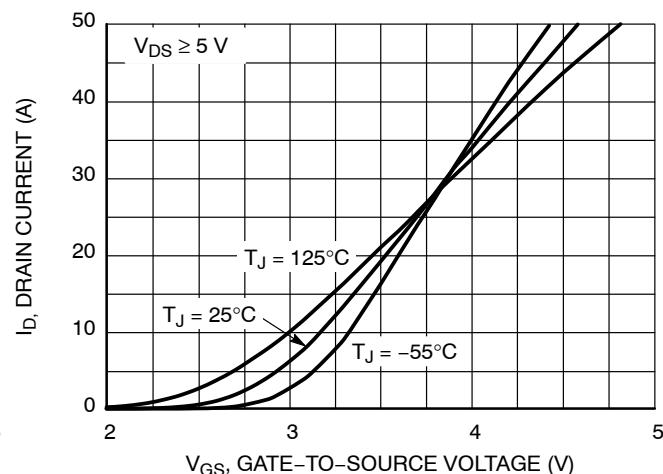


Figure 2. Transfer Characteristics – Channel 2

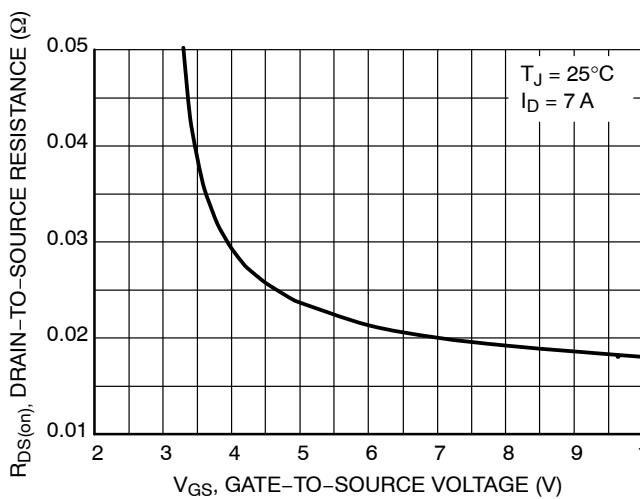


Figure 3. On-Resistance vs. Gate-to-Source Voltage – Channel 2

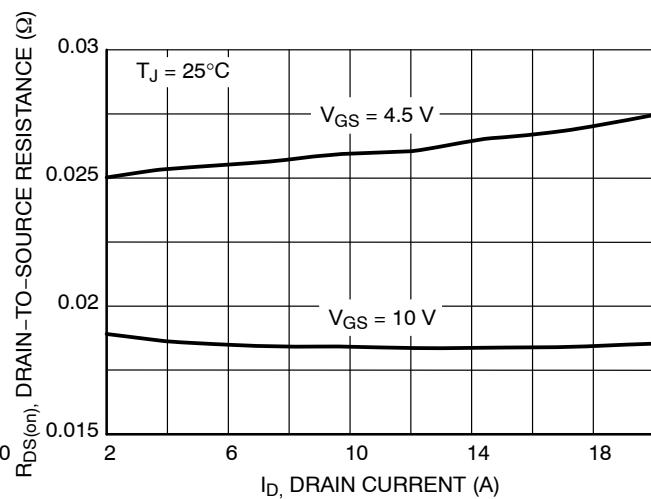


Figure 4. On-Resistance vs. Drain Current and Gate Voltage – Channel 2

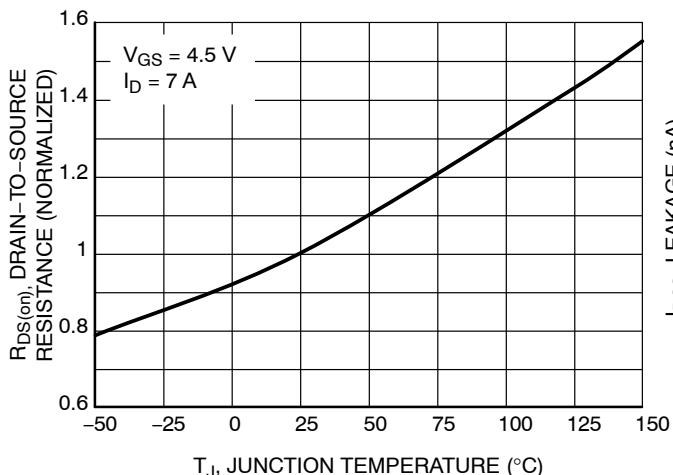


Figure 5. On-Resistance Variation with Temperature – Channel 2

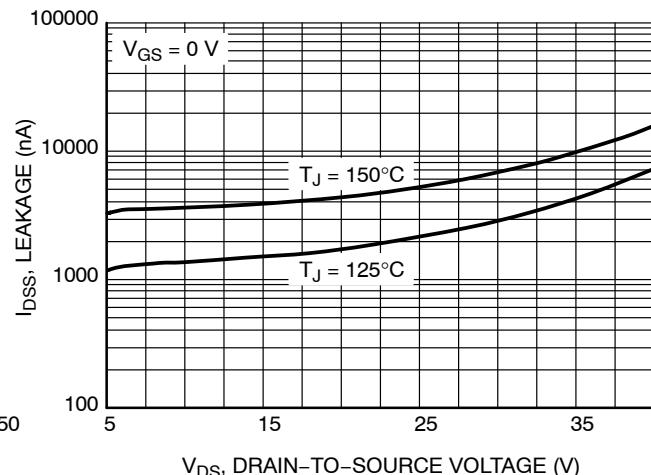
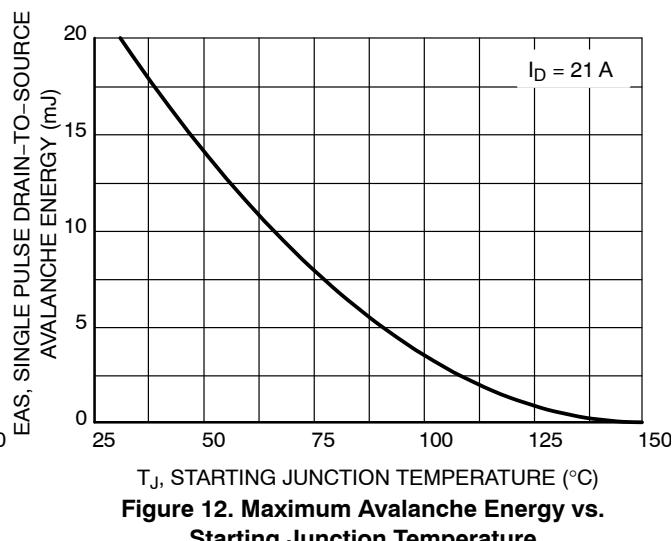
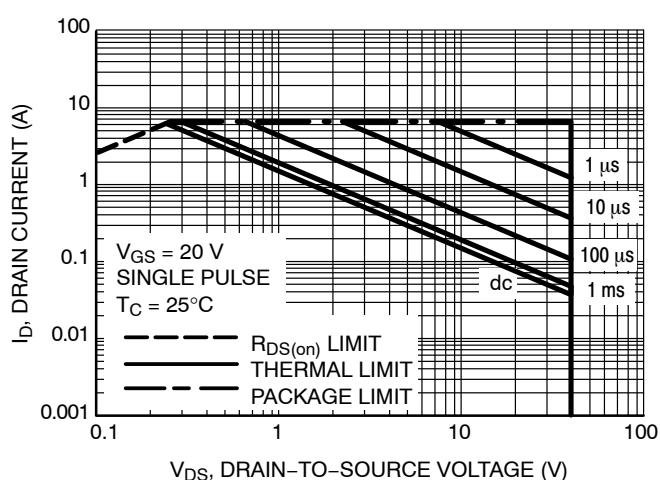
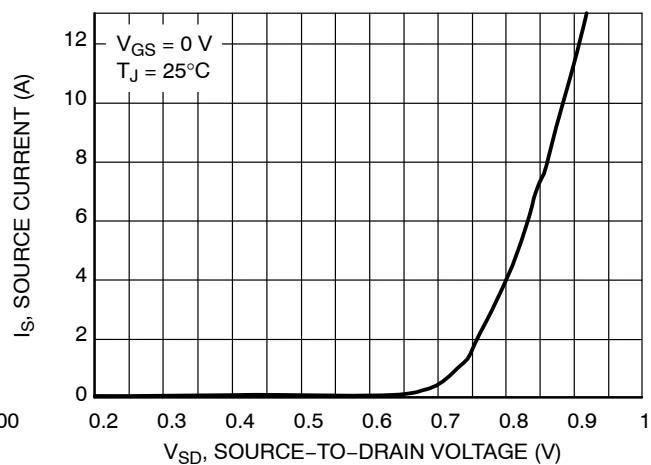
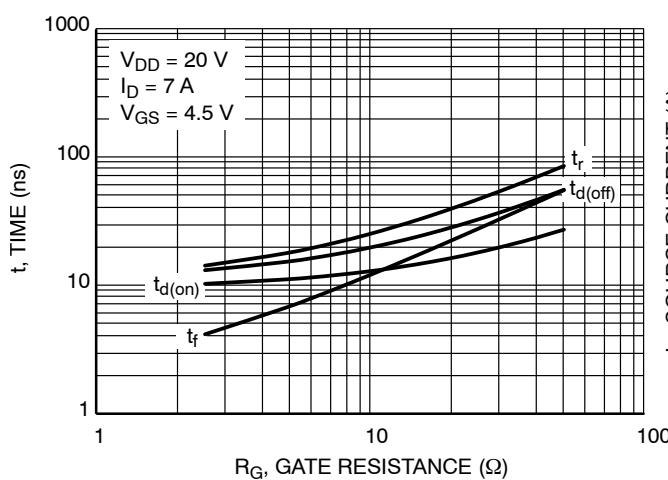
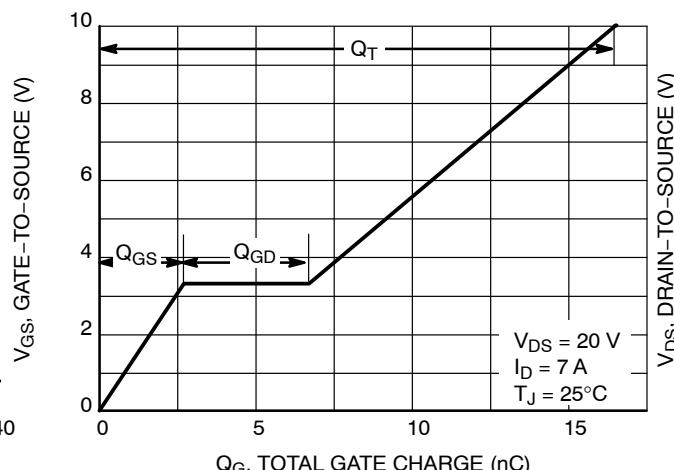
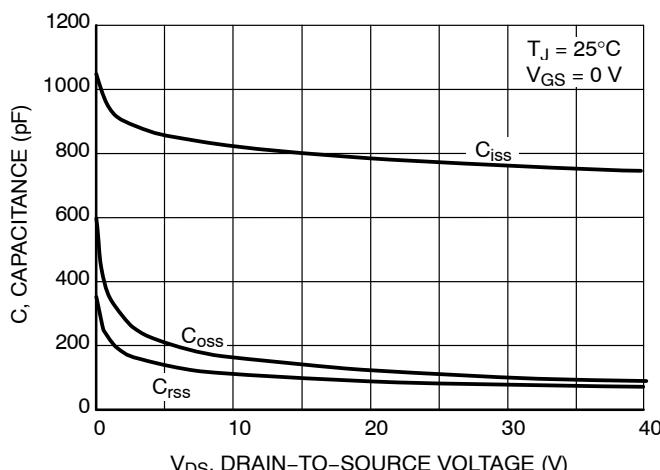


Figure 6. Drain-to-Source Leakage Current vs. Voltage – Channel 2

TYPICAL PERFORMANCE CURVES



NTMD5836NL

TYPICAL PERFORMANCE CURVES

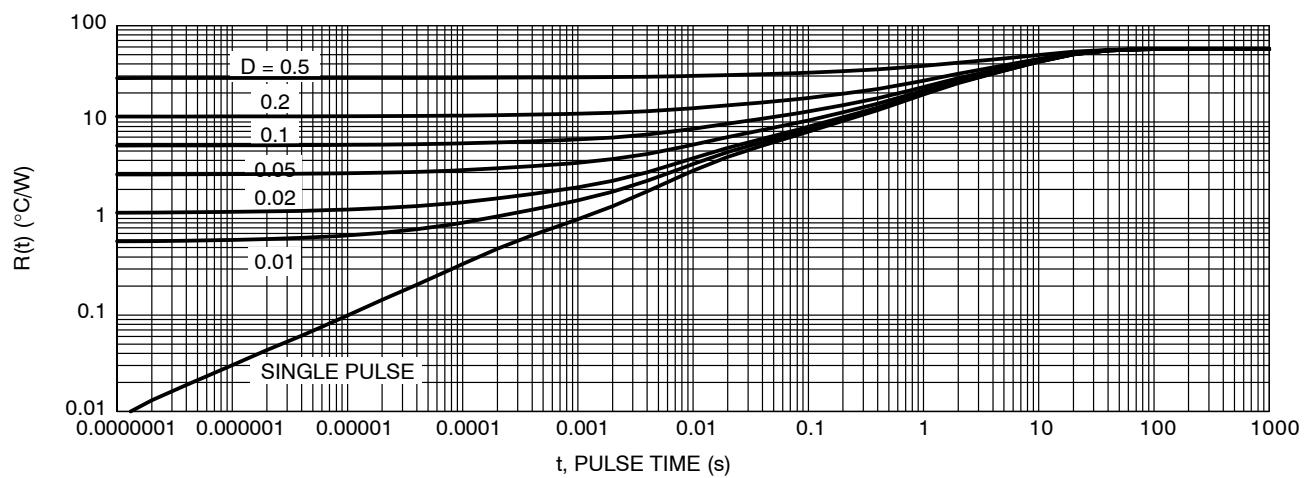


Figure 13. Thermal Response

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

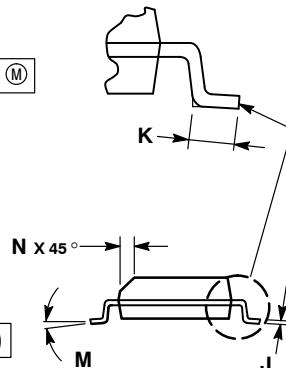
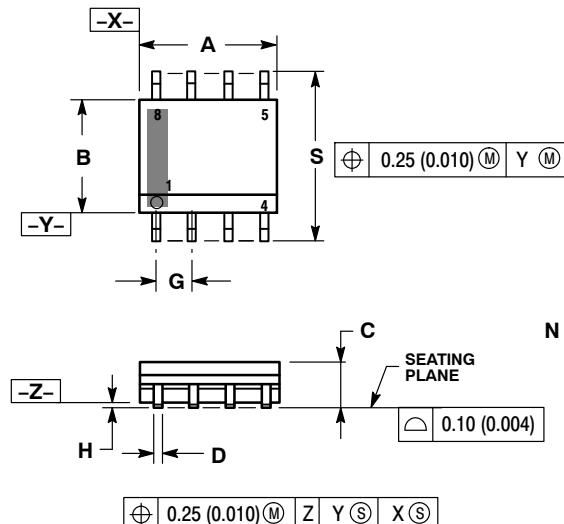
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SCALE 1:1

SOIC-8 NB
CASE 751-07
ISSUE AK

DATE 16 FEB 2011

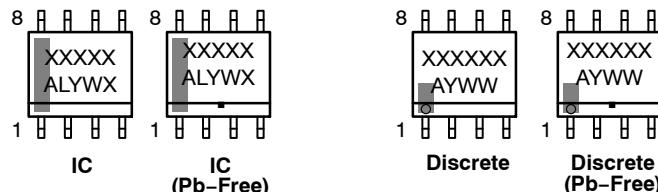


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

**GENERIC
MARKING DIAGRAM***



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

SCALE 6:1 (mm/inches)

STYLES ON PAGE 2

DOCUMENT NUMBER:	98ASB42564B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SOIC-8 NB	PAGE 1 OF 2

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SOIC-8 NB
CASE 751-07
ISSUE AK

DATE 16 FEB 2011

STYLE 1: PIN 1. Emitter 2. Collector 3. Collector 4. Emitter 5. Emitter 6. Base 7. Base 8. Emitter	STYLE 2: PIN 1. Collector, Die #1 2. Collector, #1 3. Collector, #2 4. Collector, #2 5. Base, #2 6. Emitter, #2 7. Base, #1 8. Emitter, #1	STYLE 3: PIN 1. Drain, Die #1 2. Drain, #1 3. Drain, #2 4. Drain, #2 5. Gate, #2 6. Source, #2 7. Gate, #1 8. Source, #1	STYLE 4: PIN 1. Anode 2. Anode 3. Anode 4. Anode 5. Anode 6. Anode 7. Anode 8. Common Cathode
STYLE 5: PIN 1. Drain 2. Drain 3. Drain 4. Drain 5. Gate 6. Gate 7. Source 8. Source	STYLE 6: PIN 1. Source 2. Drain 3. Drain 4. Source 5. Source 6. Gate 7. Gate 8. Source	STYLE 7: PIN 1. Input 2. External Bypass 3. Third Stage Source 4. Ground 5. Drain 6. Gate 3 7. Second Stage Vd 8. First Stage Vd	STYLE 8: PIN 1. Collector, Die #1 2. Base, #1 3. Base, #2 4. Collector, #2 5. Collector, #2 6. Emitter, #2 7. Emitter, #1 8. Collector, #1
STYLE 9: PIN 1. Emitter, Common 2. Collector, Die #1 3. Collector, Die #2 4. Emitter, Common 5. Emitter, Common 6. Base, Die #2 7. Base, Die #1 8. Emitter, Common	STYLE 10: PIN 1. Ground 2. Bias 1 3. Output 4. Ground 5. Ground 6. Bias 2 7. Input 8. Ground	STYLE 11: PIN 1. Source 1 2. Gate 1 3. Source 2 4. Gate 2 5. Drain 2 6. Drain 2 7. Drain 1 8. Drain 1	STYLE 12: PIN 1. Source 2. Source 3. Source 4. Gate 5. Drain 6. Drain 7. Drain 8. Drain
STYLE 13: PIN 1. N.C. 2. Source 3. Source 4. Gate 5. Drain 6. Drain 7. Drain 8. Drain	STYLE 14: PIN 1. N-Source 2. N-Gate 3. P-Source 4. P-Gate 5. P-Drain 6. P-Drain 7. N-Drain 8. N-Drain	STYLE 15: PIN 1. Anode 1 2. Anode 1 3. Anode 1 4. Anode 1 5. Cathode, Common 6. Cathode, Common 7. Cathode, Common 8. Cathode, Common	STYLE 16: PIN 1. Emitter, Die #1 2. Base, Die #1 3. Emitter, Die #2 4. Base, Die #2 5. Collector, Die #2 6. Collector, Die #2 7. Collector, Die #1 8. Collector, Die #1
STYLE 17: PIN 1. VCC 2. V2OUT 3. V1OUT 4. TXE 5. RXE 6. VEE 7. GND 8. ACC	STYLE 18: PIN 1. Anode 2. Anode 3. Source 4. Gate 5. Drain 6. Drain 7. Cathode 8. Cathode	STYLE 19: PIN 1. Source 1 2. Gate 1 3. Source 2 4. Gate 2 5. Drain 2 6. Mirror 2 7. Drain 1 8. Mirror 1	STYLE 20: PIN 1. Source (N) 2. Gate (N) 3. Source (P) 4. Gate (P) 5. Drain 6. Drain 7. Drain 8. Drain
STYLE 21: PIN 1. Cathode 1 2. Cathode 2 3. Cathode 3 4. Cathode 4 5. Cathode 5 6. Common Anode 7. Common Anode 8. Cathode 6	STYLE 22: PIN 1. I/O Line 1 2. Common Cathode/VCC 3. Common Cathode/VCC 4. I/O Line 3 5. Common Anode/GND 6. I/O Line 4 7. I/O Line 5 8. Common Anode/GND	STYLE 23: PIN 1. Line 1 IN 2. Common Anode/GND 3. Common Anode/GND 4. Line 2 IN 5. Line 2 OUT 6. Common Anode/GND 7. Common Anode/GND 8. Line 1 OUT	STYLE 24: PIN 1. Base 2. Emitter 3. Collector/Anode 4. Collector/Anode 5. Cathode 6. Cathode 7. Collector/Anode 8. Collector/Anode
STYLE 25: PIN 1. VIN 2. N/C 3. REXT 4. GND 5. IOUT 6. IOUT 7. IOUT 8. IOUT	STYLE 26: PIN 1. GND 2. dv/dt 3. Enable 4. ILIMIT 5. Source 6. Source 7. Source 8. VCC	STYLE 27: PIN 1. ILIMIT 2. OVLO 3. UVLO 4. INPUT+ 5. SOURCE 6. SOURCE 7. SOURCE 8. DRAIN	STYLE 28: PIN 1. SW_TO_GND 2. DASIC_OFF 3. DASIC_SW_DET 4. GND 5. V_MON 6. VBUCK 7. VBUCK 8. VIN
STYLE 29: PIN 1. Base, Die #1 2. Emitter, #1 3. Base, #2 4. Emitter, #2 5. Collector, #2 6. Collector, #2 7. Collector, #1 8. Collector, #1	STYLE 30: PIN 1. Drain 1 2. Drain 1 3. Gate 2 4. Source 2 5. Source 1/Drain 2 6. Source 1/Drain 2 7. Source 1/Drain 2 8. Gate 1		

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