# CC2591 2.4-GHz RF Front End

## 1 Device Overview

### 1.1 Features

- Seamless Interface to 2.4-GHz Low-Power RF Devices from Texas Instruments
- Output Power up to 22 dBm
- Few External Components
  - Integrated Switches
  - Integrated Matching Network
  - Integrated Balun
  - Integrated Inductors
  - Integrated PA
  - Integrated LNA
- Digital Control of LNA Gain by HGM Pin
- 100-nA in Power Down (EN = PAEN = 0)
- Low Transmit Current Consumption (100 mA at 3 V for 20-dBm Out, PAE = 33%)
- Low-Receive Current Consumption
  - 3.4 mA for High-Gain Mode
  - 1.7 mA for Low-Gain Mode
- 4.8-dB LNA Noise Figure, Including T/R Switch and External Antenna Match
- RoHS Compliant 4×4-mm QFN-16 Package
- 2-V to 3.6-V Operation

### 1.2 Applications

- All 2.4-GHz ISM Band Systems
- Wireless Sensor Networks
- Wireless Industrial Systems
- IEEE 802.15.4 and ZigBee® Systems
- Wireless Consumer Systems
- Wireless Audio Systems

### 1.3 Description

CC2591 is a cost-effective and high-performance RF front end for low-power and low-voltage 2.4-GHz wireless applications. The device is a range extender for all existing and future 2.4-GHz low-power RF transceivers, transmitters, and System-on-Chip products from TI. CC2591 increases the link budget by providing a power amplifier for increased output power, and an LNA with low noise figure for improved receiver sensitivity. The device provides a small size, high output power RF design with its 4-mm × 4-mm QFN-16 package. The device contains PA, LNA, switches, RF-matching, and balun for simple design of high-performance wireless applications.

**Device Information(1)**

| PART NUMBER | PACKAGE | BODY SIZE |
|---|---|---|
| CC2591RGV | RGV (16) | 4.00 mm × 4.00 mm |

(1) For more information, see Section 7, *Mechanical Packaging and Orderable Information*.

## 1.4 Functional Block Diagram

Figure 1-1 shows the functional block diagram of the device.

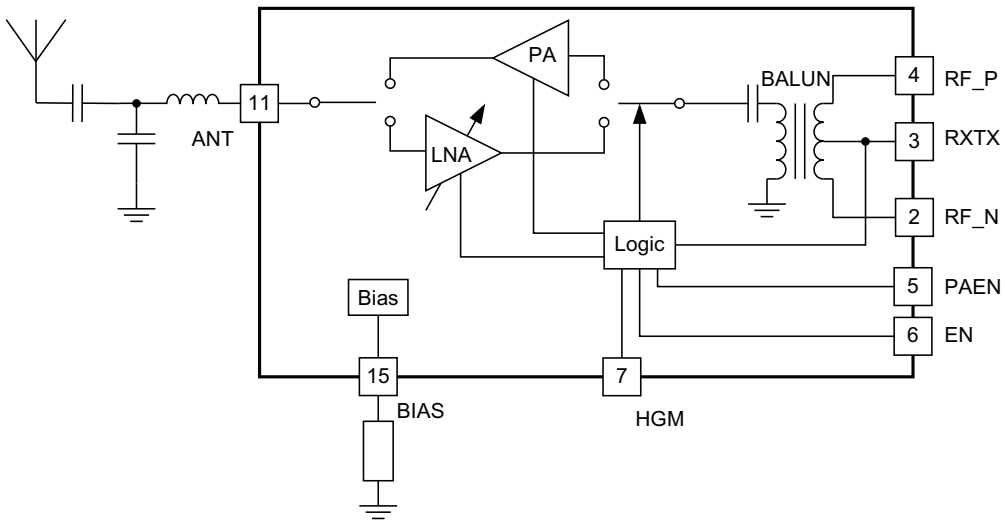



**Figure 1-1. Functional Block Diagram**

# Table of Contents



## 2 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision A (June 2008) to Revision B | Page |
|---|---|
| • Changed format of data sheet to the latest TI standards | 1 |

## 3 Terminal Configuration and Functions

The CC2591 pinout and description are shown in Figure 3-1 and Table 3-1, respectively.

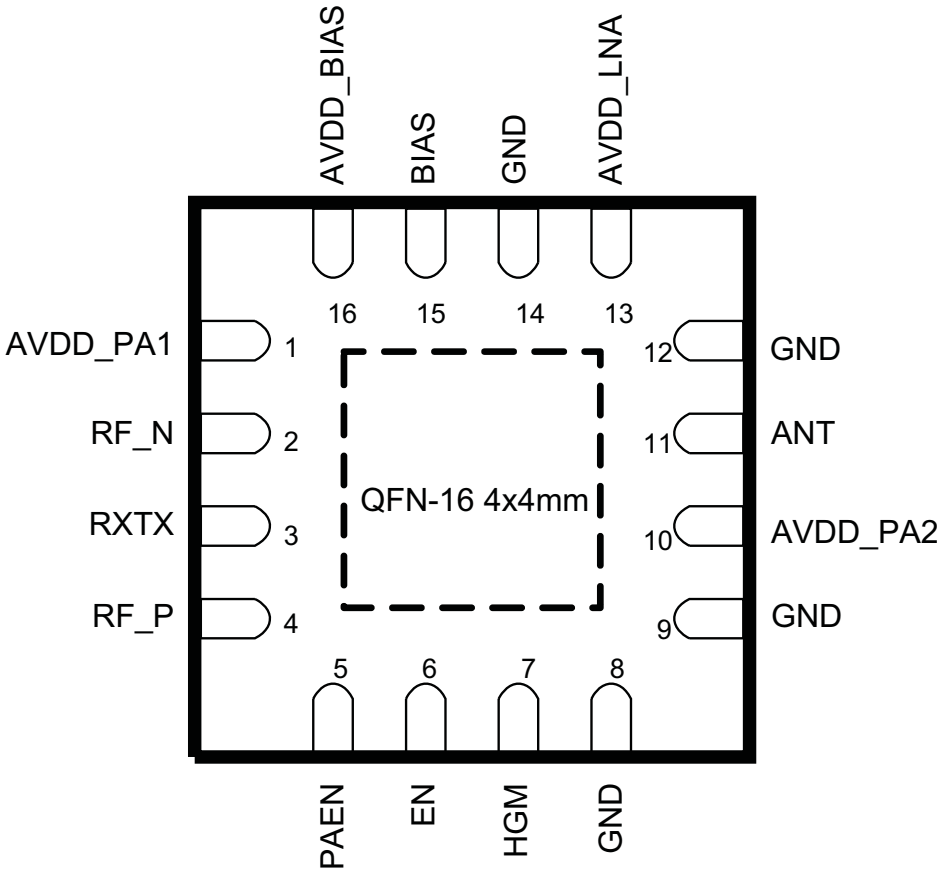



**Figure 3-1. PIN AND I/O CONFIGURATION (TOP VIEW)**

**NOTE**

The exposed die attach pad **must** be connected to a solid ground plane as this is the primary ground connection for the chip. Inductance in vias to the pad should be minimized. It is highly recommended to follow the reference layout. Changes will alter the performance.

For best performance, minimize the length of the ground vias, by using a 4-layer PCB with ground plane as layer 2 when CC2591 is mounted onto layer 1.

## 3.1 Pin Attributes

**Table 3-1. Pin Attributes**

| TERMINAL | | TYPE | DESCRIPTION |
|---|---|---|---|
| NO. | NAME | | |
| — | GND | Ground | The exposed die attach pad must be connected to a solid ground plane. See CC2591EM reference design for recommended layout. |
| 1 | AVDD_PA1 | Power | 2.0 V – 3.6 V Power. PCB trace to this pin serves as inductive load to PA . See CC2591EM reference design for recommended layout. |
| 2 | RF_N | RF | RF interface towards CC24xx or CC25xx device. |
| 3 | RXTX | Analog/Control | RXTX switching voltage when connected to CC24xx devices. See Table 5-2 and Table 5-3 for details. |
| 4 | RF_P | RF | RF interface towards CC24xx or CC25xx device |
| 5 | PAEN | Digital Input | Digital control pin. See Table 5-2 and Table 5-3 for details. |
| 6 | EN | Digital Input | Digital control pin. See Table 5-2 and Table 5-3 for details. |
| 7 | HGM | Digital Input | Digital control pin.<br>HGM=1 → Device in High Gain Mode<br>HGM=0 → Device in Low Gain Mode (RX only) |
| 8, 9, 12, 14 | GND | Ground | Secondary ground connections. Should be shorted to the die attach pad on the top PCB layer. |
| 10 | AVDD_PA2 | Power | 2.0 V – 3.6 V Power. PCB trace to this pin serves as inductive load to PA. See CC2591EM reference design for recommended layout. |
| 11 | ANT | RF | Antenna interface. |
| 13 | AVDD_LNA | Power | 2 V – 3.6 V Power. PCB trace to this pin serves as inductive load to LNA. See CC2591EM reference design for recommended layout. |
| 15 | BIAS | Analog | Biasing input. Resistor between this node and ground sets bias current to PAs. |
| 16 | AVDD_BIAS | Power | 2 V – 3.6 V Power. |

# 4 Specifications

## 4.1 Absolute Maximum Ratings(1)(2)

Under no circumstances must the absolute maximum ratings be violated. Stress exceeding one or more of the limiting values may cause permanent damage to the device.

| PARAMETER | | VALUE | UNIT |
|---|---|---|---|
| Supply voltage | All supply pins must have the same voltage | –0.3 to 3.6 | V |
| Voltage on any digital pin | | –0.3 to $V_{DD}$ + 0.3, max 3.6 | |
| Input RF level | | 10 | dBm |

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to $V_{SS}$, unless otherwise noted.

## 4.2 Handling Ratings

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $T_{stg}$ | Storage temperature range | | –50 | 150 | °C |
| $V_{ESD}$ | Electrostatic discharge (ESD) performance: | Human Body Model (HBM), per ANSI/ESDA/JEDEC JS001(1) | –600 | 600 | V |
| | | Charged Device Model (CDM), per JESD22-C101(2) | –500 | 500 | V |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 4.3 Recommended Operating Conditions

The operating conditions for CC2591 are listed below.

| PARAMETER | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Ambient temperature range | | –40 | 85 | °C |
| Operating supply voltage | | 2 | 3.6 | V |
| Operating frequency range | | 2400 | 2483.5 | MHz |

## 4.4 Electrical Characteristics

$T_C$ = 25°C, $V_{DD}$ = 3 V , $f_{RF}$= 2440 MHz (unless otherwise noted). Measured on CC2591EM reference design including external matching components.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Receive current, High-Gain Mode | HGM = 1 | | 3.4 | 4 | mA |
| Receive current, Low-Gain Mode | HGM = 0 | | 1.7 | 2 | |
| Transmit current | $P_{IN}$ = 0.5 dBm | | 112 | | |
| Transmit current | No input signal | | 40 | 50 | |
| Power-down current | EN = PAEN = 0 | | 0.1 | 0.3 | µA |
| High-input level (control pins) | EN, PAEN, HGM, RXTX | 1.3 | | $V_{DD}$ | V |
| Low-input level (control pins) | EN, PAEN, HGM, RXTX | | | 0.3 | |
| Power down - Receive mode switching time | | | 12 | | µs |
| Power down - Transmit mode switching time | | | 1 | | µs |
| **RF Receive** | | | | | |
| Gain, High-Gain Mode | HGM = 1 | | 11 | | dB |
| Gain, Low-Gain Mode | HGM = 0 | | 1 | | dB |
| Gain variation, 2400 – 2483.5 MHz, High-Gain Mode | HGM = 1 | | 1.3 | | dB |
| Gain variation, 2.0 V – 3.6 V, High-Gain Mode | HGM = 1 | | 1.5 | | dB |

## Electrical Characteristics *(continued)*

$T_C$ = 25°C, $V_{DD}$ = 3 V , $f_{RF}$= 2440 MHz (unless otherwise noted). Measured on CC2591EM reference design including external matching components.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Gain variation, -40°C – 85°C, High-Gain Mode | HGM = 1 | | 3 | | dB |
| Noise figure, High-Gain Mode | HGM = 1, including internal T/R switch and external antenna match | | 4.8 | | dB |
| Input 1-dB compression, High-Gain Mode | HGM = 1 | | –17 | | dBm |
| Input IP3, High-Gain Mode | HGM = 1 | | –2 | | dBm |
| Input reflection coefficient, S11 | HGM = 1, measured at antenna port | | –11 | | dB |
| **RF Transmit** | | | | | |
| Gain | | | 22 | | dB |
| Output power, $P_{OUT}$ | $P_{IN}$ = 0.5 dBm | | 20.6 | | dBm |
| Maximum output power | $P_{IN}$ = 5 dBm | | 22 | | dBm |
| Power Added Efficiency, PAE | $P_{IN}$ = 0.5 dBm | | 34% | | |
| Output 1-dB compression | | | 19 | | dBm |
| Output IP3 | | | 32 | | dBm |
| Output power variation over frequency | 2400 – 2483.5 MHz, $P_{IN}$ = 0.5 dBm | | 0.5 | | dB |
| Output power variation over power supply | 2 V – 3.6 V , $P_{IN}$ = 0.5 dBm | | 3.5 | | dB |
| Output power variation over temperature | -40°C – 85°C, $P_{IN}$ = 0.5 dBm | | 1.5 | | dB |
| Second harmonic power | $P_{IN}$ = 0.5 dBm. The second harmonic can be reduced to below regulatory limits by using an external LC filter and antenna. | | –15 | | dBm |
| Third harmonic power | $P_{IN}$ = 0.5 dBm. The third harmonic can be reduced to below regulatory limits by using an external LC filter and antenna. | | –30 | | dBm |

## 4.5 Thermal Resistance Characteristics for RGV Package

| NAME | DESCRIPTION | °C/W(1) (2) | AIR FLOW (m/s)(3) |
|---|---|---|---|
| $R\Theta_{JC\text{-}top}$ | Junction-to-case (top) | 52.8 | 0.00 |
| $R\Theta_{JB}$ | Junction-to-board | 20.4 | 0.00 |
| $R\Theta_{JA}$ | Junction-to-free air | 41.9 | 0.00 |
| $Psi_{JT}$ | Junction-to-package top | 1.4 | 0.00 |
| $Psi_{JB}$ | Junction-to-board | 20.5 | 0.00 |
| $R\Theta_{JC\text{-}bottom}$ | Junction-to-case (bottom) | 8.3 | 0.00 |

(1) °C/W = degrees Celsius per watt.
(2) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC [$R\Theta_{JC}$] value, which is based on a JEDEC-defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:
- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

(3) m/s = meters per second.

## 4.6 Typical Characteristics

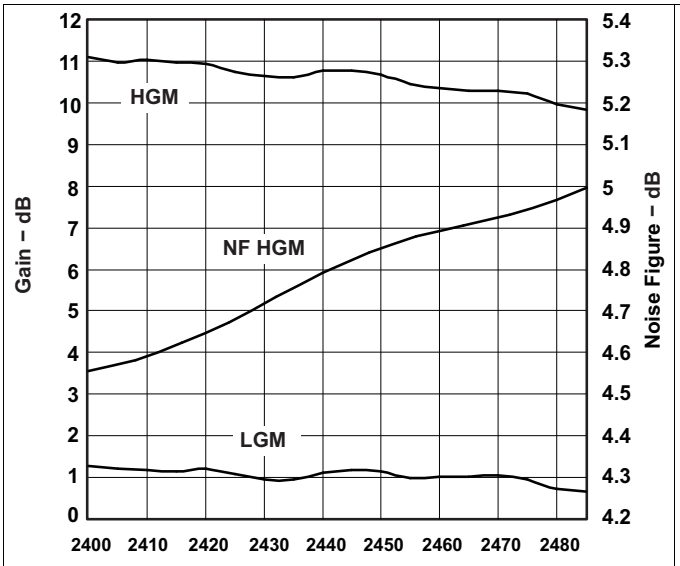



**Figure 4-1. LNA Gain and Noise Figure vs Frequency**

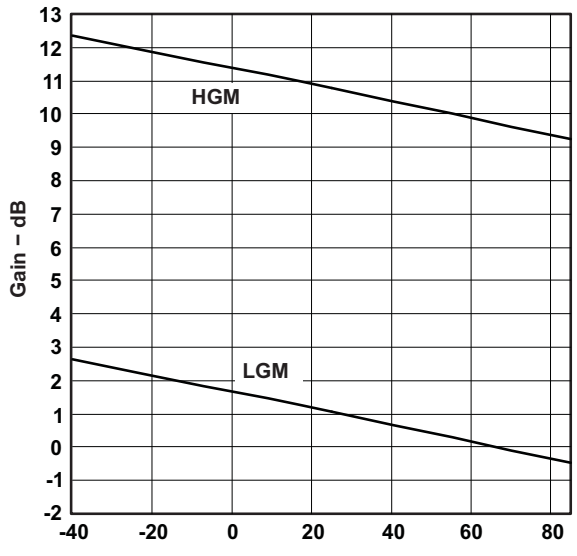



**Figure 4-2. LNA Gain vs Temperature**

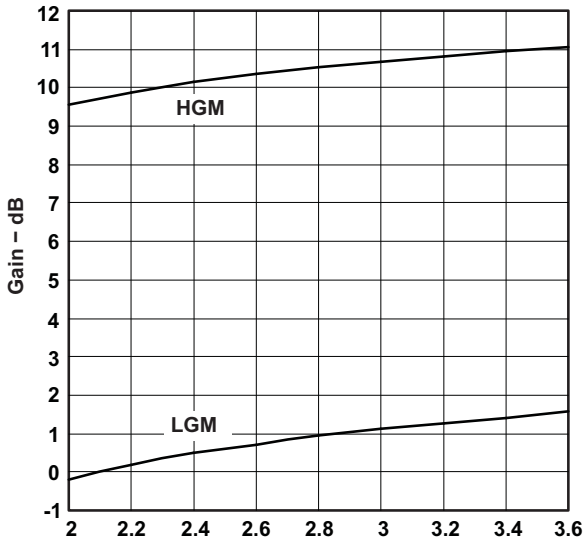



**Figure 4-3. LNA Gain vs Power Supply**

# 5 Applications, Implementation, and Layout

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 5.1 CC2591EM Evaluation Module

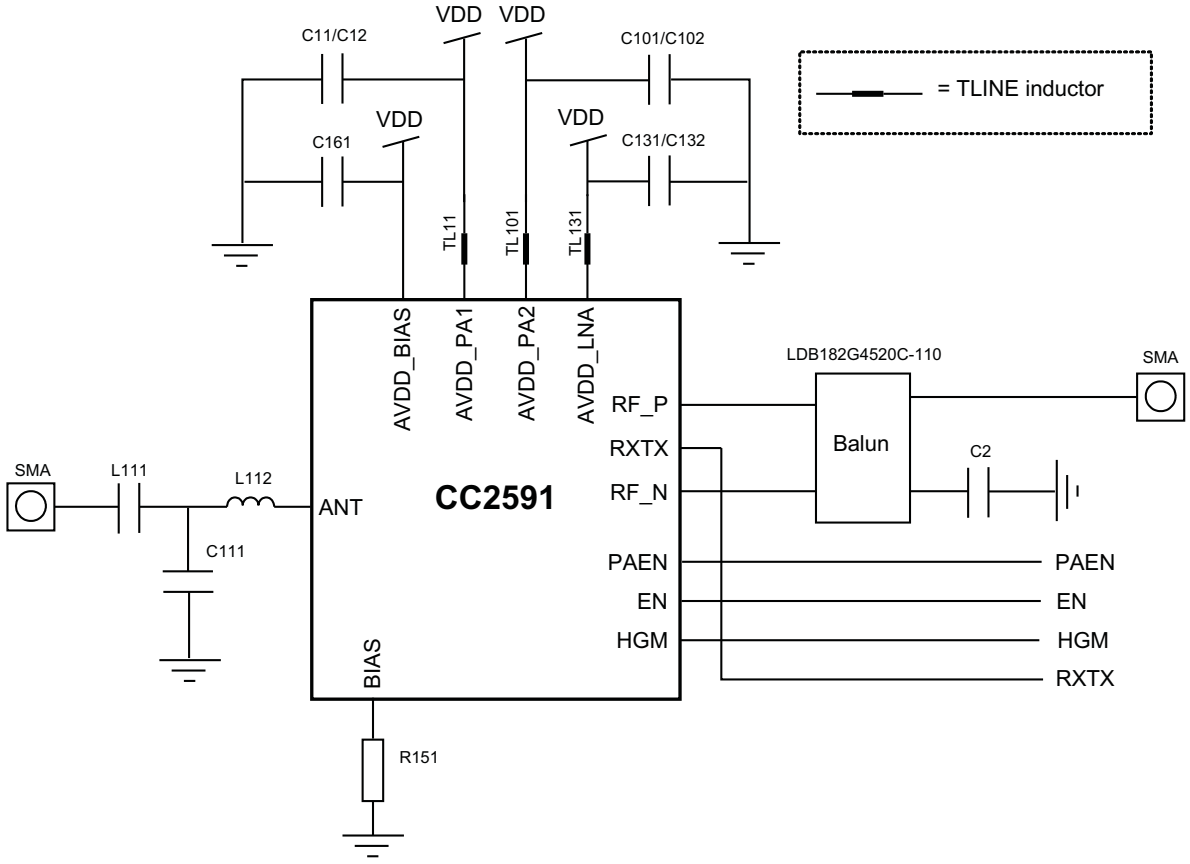



**Figure 5-1. CC2591EM Evaluation Module**

**Table 5-1. List of Materials (See CC2591EM Reference Design)**

| DEVICE | FUNCTION | VALUE |
|---|---|---|
| L112 | Part of antenna match. | 1.5 nH: LQW15AN1N5B00 from Murata |
| L111 | DC block. | 1 nF: GRM1555C1H102JA01 from Murata |
| C111 | Part of antenna match. | 1 pF: GRM1555C1H1R0BZ01 from Murata |
| C161 | Decoupling capacitor. | 1 nF: GRM1555C1H102JA01 from Murata |
| C11/C12 | Decoupling. Will affect PA resonance. | 10 pF \|\| 1 nF. The smallest cap closest. See CC2591EM reference design (SWRU190) for placement.<br>10 pF: GRM1555C1H100JZ01 from Murata<br>1 nF: GRM1555C1H102JA01 from Murata |
| C101/C102 | Decoupling. Will affect PA resonance. | 18 pF \|\| 1 nF. The smallest cap closest. See CC2591EM reference design (SWRU190) for placement.<br>18 pF: GRM1555C1H180JZ01 from Murata<br>1 nF: GRM1555C1H102JA01 from Murata |
| C131/C132 | Decoupling. Will affect PA resonance. | 10 pF \|\| 1 nF. The smallest cap closest. See CC2591EM reference design (SWRU190) for placement.<br>10 pF: GRM1555C1H100JZ01 from Murata<br>1 nF: GRM1555C1H102JA01 from Murata |
| C2 | Decoupling of external balun | 1 nF: GRM1555C1H102JA01 from Murata |
| TL11 | Transmission line. Will affect PA resonance. | See CC2591EM reference design. |
| TL101 | Transmission line. Will affect PA resonance. | See CC2591EM reference design. |
| TL131 | Transmission line. Will affect LNA resonance. | See CC2591EM reference design. |
| R151 | Bias resistor | 4.3 kΩ: RK73H1ETTP4301F from Koa |

## 5.2 Controlling the Output Power from CC2591

The output power of CC2591 is controlled by controlling the input power. The CC2591 PA is designed to work in compression (class AB), and the best efficiency is reached when a strong input signal is applied.

### *5.2.1 Input Levels on Control Pins*

The four digital control pins (PAEN, EN, HGM, RXTX) have built-in level-shifting functionality, meaning that if the CC2591 is operating from a 3.6-V supply voltage, the control pins will still sense 1.6-V - 1.8-V signals as logical ‘1’.

An example of the above would be that RXTX is connected directly to the RXTX pin on CC24xx, but the global supply voltage is 3.6 V. The RXTX pin on CC24xx will switch between 0 V (RX) and 1.8 V(TX), which is still a high enough voltage to control the mode of CC2591.

The input voltages should however not have logical ‘1’ level that is higher than the supply.

### *5.2.2 Connecting CC2591 to a CC24xx Device*

**Table 5-2. Control Logic for Connecting CC2591 to a CC24xx Device**

| PAEN = EN | RXTX | HGM | MODE OF OPERATION |
|---|---|---|---|
| 0 | X | X | Power Down |
| 1 | 0 | 0 | RX Low Gain Mode |
| 1 | 0 | 1 | RX High Gain Mode |
| 1 | 1 | X | TX |

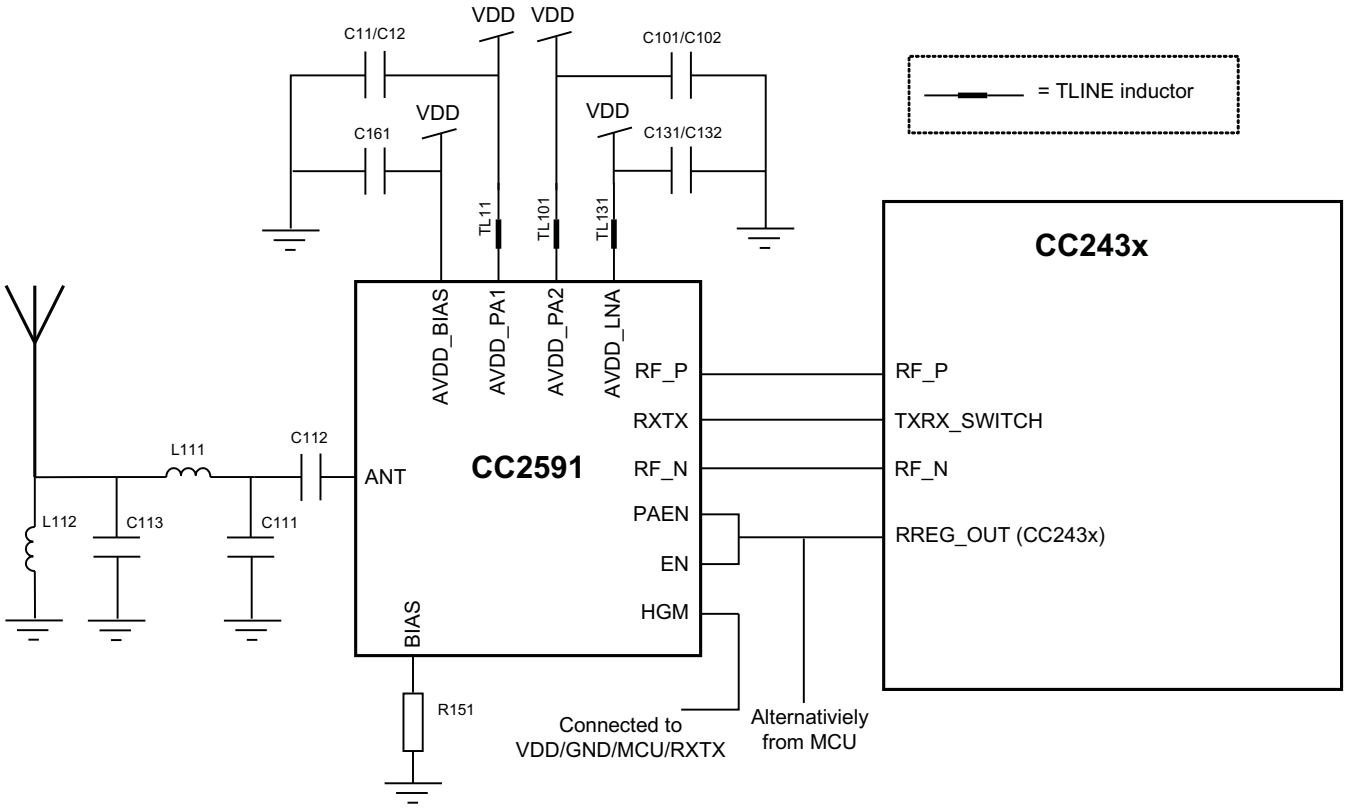



**Figure 5-2. CC2591 + CC24xx Application Circuit**

### 5.2.3 Connecting CC2591 to the CC2500, CC2510, or CC2511 Device

**Table 5-3. Control Logic for Connecting CC2591 to a CC2500/10/11 Devices**

| PAEN | EN | RXTX | HGM | MODE OF OPERATION |
|---|---|---|---|---|
| 0 | 0 | NC | X | Power Down |
| 0 | 1 | NC | 0 | RX LGM |
| 0 | 1 | NC | 1 | RX HGM |
| 1 | 0 | NC | X | TX |
| 1 | 1 | NC | X | Not allowed |

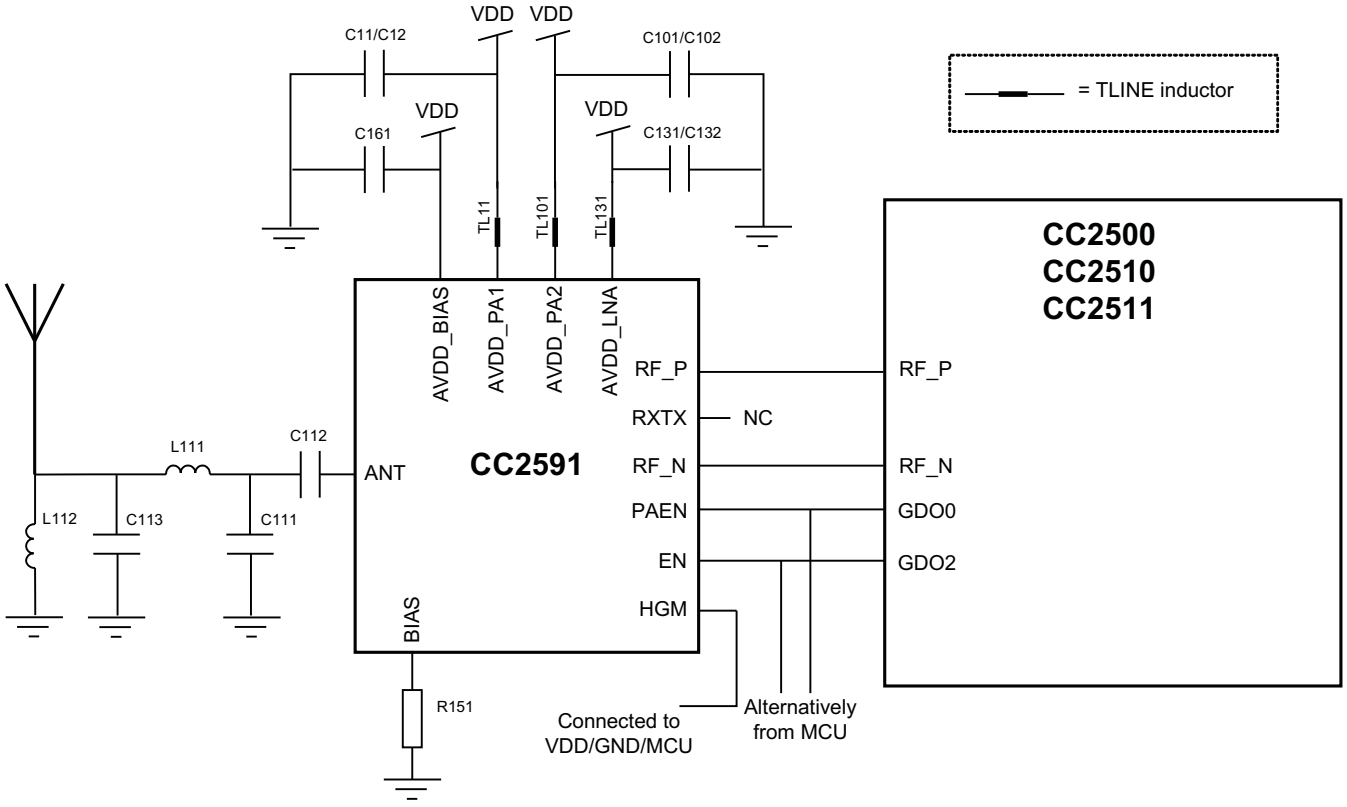



**Figure 5-3. CC2591 + CC2500/10/11 Device Application Circuit**

### 5.2.4 Connecting CC2591 to a CC2520 Device

**Table 5-4. Control Logic for Connecting CC2591 to a CC2520 Device**

| PAEN | EN | RXTX | HGM | MODE OF OPERATION |
|---|---|---|---|---|
| 0 | 0 | NC | X | Power Down |
| 0 | 1 | NC | 0 | RX LGM |
| 0 | 1 | NC | 1 | RX HGM |
| 1 | 0 | NC | X | TX |
| 1 | 1 | NC | X | Not allowed |

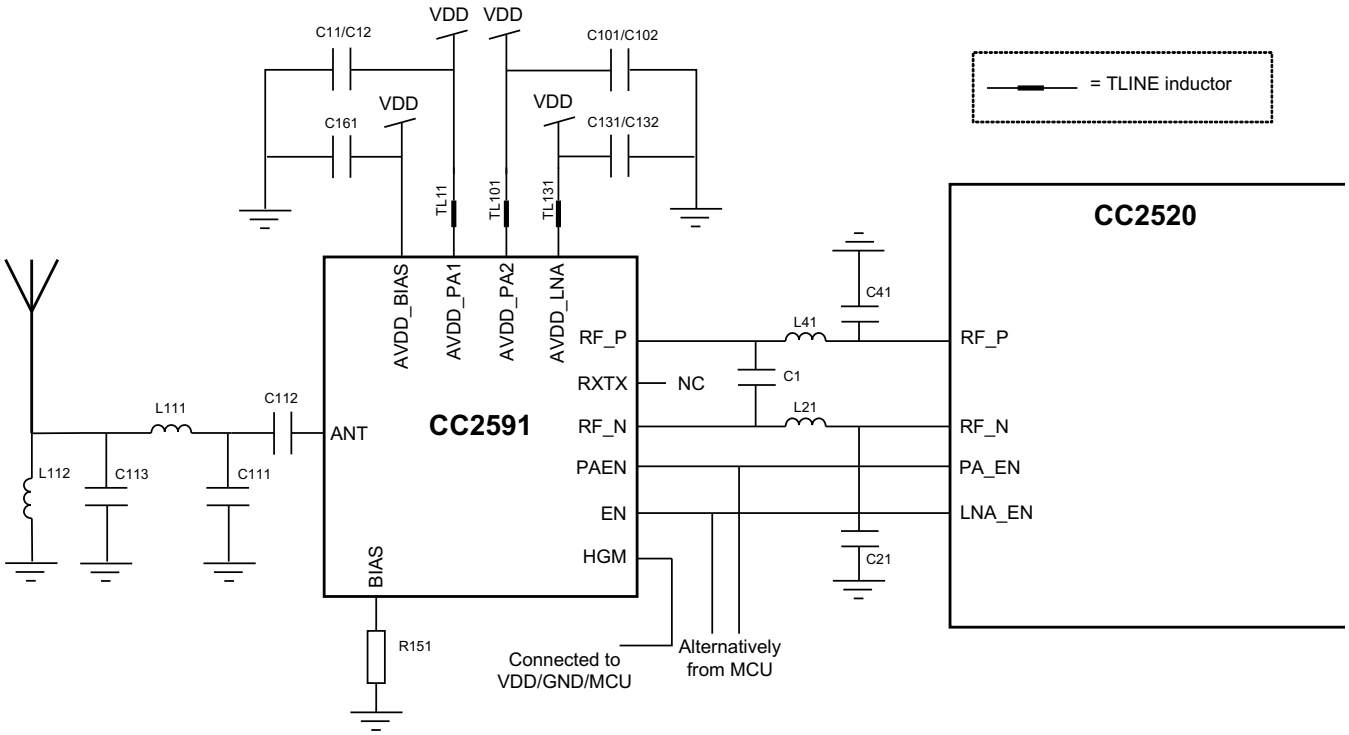



**Figure 5-4. CC2591 + CC2520 Application Circuit**

# 6 Device and Documentation Support

## 6.1 Device Support

### 6.1.1 Development Support

TI offers an extensive line of development tools, including tools to evaluate the performance of the processors, generate code, develop algorithm implementations, and fully integrate and debug software and hardware modules. The tool's support documentation is electronically available within the Code Composer Studio™ Integrated Development Environment (IDE).

The following products support development of the CC2591 device applications:

**Software Development Tools:** Code Composer Studio™ Integrated Development Environment (IDE): including Editor C/C++/Assembly Code Generation, and Debug plus additional development tools Scalable, Real-Time Foundation Software (DSP/BIOS™), which provides the basic run-time target software needed to support any CC2591 device application.

**Hardware Development Tools:** Extended Development System (XDS™) Emulator

For a complete listing of development-support tools for the CC2591 platform, visit the Texas Instruments website at www.ti.com. For information on pricing and availability, contact the nearest TI field sales office or authorized distributor.

### 6.1.2 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all microprocessors (MPUs) and support tools. Each device has one of three prefixes: X, P, or null (no prefix) (for example, CC2591). These prefixes represent evolutionary stages of product development from engineering prototypes (TMDX) through fully qualified production devices and tools (TMDS).

Device development evolutionary flow:

**X** Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.

**P** Prototype device that is not necessarily the final silicon die and may not necessarily meet final electrical specifications.

**null** Production version of the silicon die that is fully qualified.

Support tool development evolutionary flow:

X and P devices are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

Production devices have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (X or P) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, RGV) and the temperature range (for example, blank is the default commercial temperature range). provides a legend for reading the complete device name for any CC2591 device.

For orderable part numbers of CC2591 devices in the RGV package types, see the Package Option Addendum of this document, the TI website (www.ti.com), or contact your TI sales representative.

## 6.2 Documentation Support

The following documents describe the CC2591 processor. Copies of these documents are available on the Internet at www.ti.com.

**SWRA351** Antenna Quick Guide

**SWRA120** Design Note Overview

**SWRA350** YAGI 2.4 GHz PCB Antenna

**SWRA161** Antenna Selection Guide

**SWRA328** CC-Antenna-DK Documentation and Antenna Measurements Summary

**SWRA229** Using CC2591 RF Front End with CC2520

**SWRA308** Using CC2591 Front End with CC2530 and CC2531

**SWRA290** TIMAC and Z-Stack Modifications for using CC2591 RF Front End with CC2

**SWRA236** Design Steps and Results for Changing PCB Layer Thickness

**SWRA230** TI-MAC modifications for using CC2591 PA/LNA with MSP430F2618+CC2520

**SWRA208** TI-MAC and Z-Stack modifications for using CC2591 RF Front End w/CC2430

**SWRA212** Using CC2591 RF Front End with CC2430

**SWRC171** CC2530-CC2591EM Reference Design

**SPRU137** CC2520 Software Examples User's Guide

**SPRU178** CC2430 Software Examples User's Guide

### *6.2.1 Community Resources*

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**TI Embedded Processors Wiki** ***Texas Instruments Embedded Processors Wiki.*** Established to help developers get started with Embedded Processors from Texas Instruments and to foster innovation and growth of general knowledge about the hardware and software surrounding these devices.

## 6.3 Trademarks

E2E is a trademark of Texas Instruments.
ZigBee is a registered trademark of ZigBee Alliance.

## 6.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 6.5 Export Control Notice

Recipient agrees to not knowingly export or re-export, directly or indirectly, any product or technical data (as defined by the U.S., EU, and other Export Administration Regulations) including software, or any controlled product restricted by other applicable national regulations, received from disclosing party under nondisclosure obligations (if any), or any direct product of such technology, to any destination to which such export or re-export is restricted or prohibited by U.S. or other applicable laws, without obtaining prior authorization from U.S. Department of Commerce and other competent Government authorities to the extent required by those laws.

## 6.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 7 Mechanical Packaging and Orderable Information

## 7.1 Packaging Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| CC2591RGVR | NRND | VQFN | RGV | 16 | 2500 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | CC2591 | |
| CC2591RGVT | NRND | VQFN | RGV | 16 | 250 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | CC2591 | |
| CC2591RGVTG4 | NRND | VQFN | RGV | 16 | 250 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | CC2591 | |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

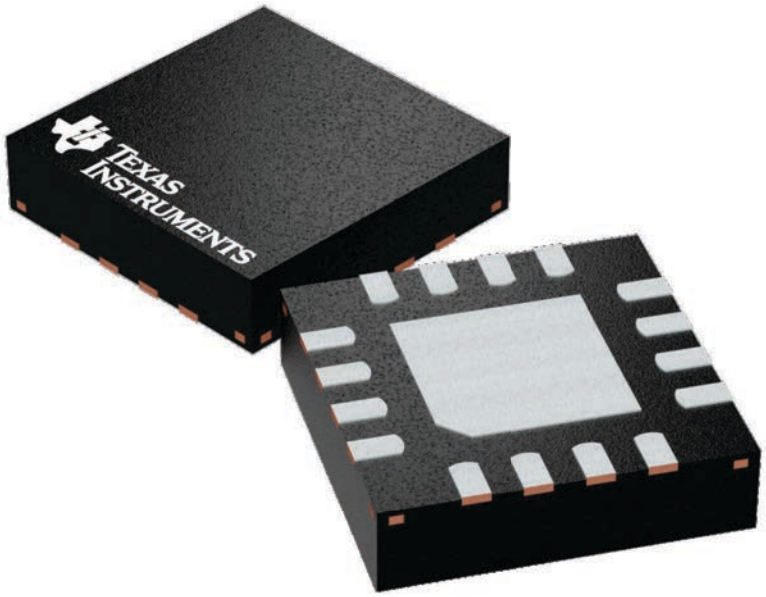
# GENERIC PACKAGE VIEW

## RGV 16

## VQFN - 1 mm max height

**4 x 4, 0.65 mm pitch**

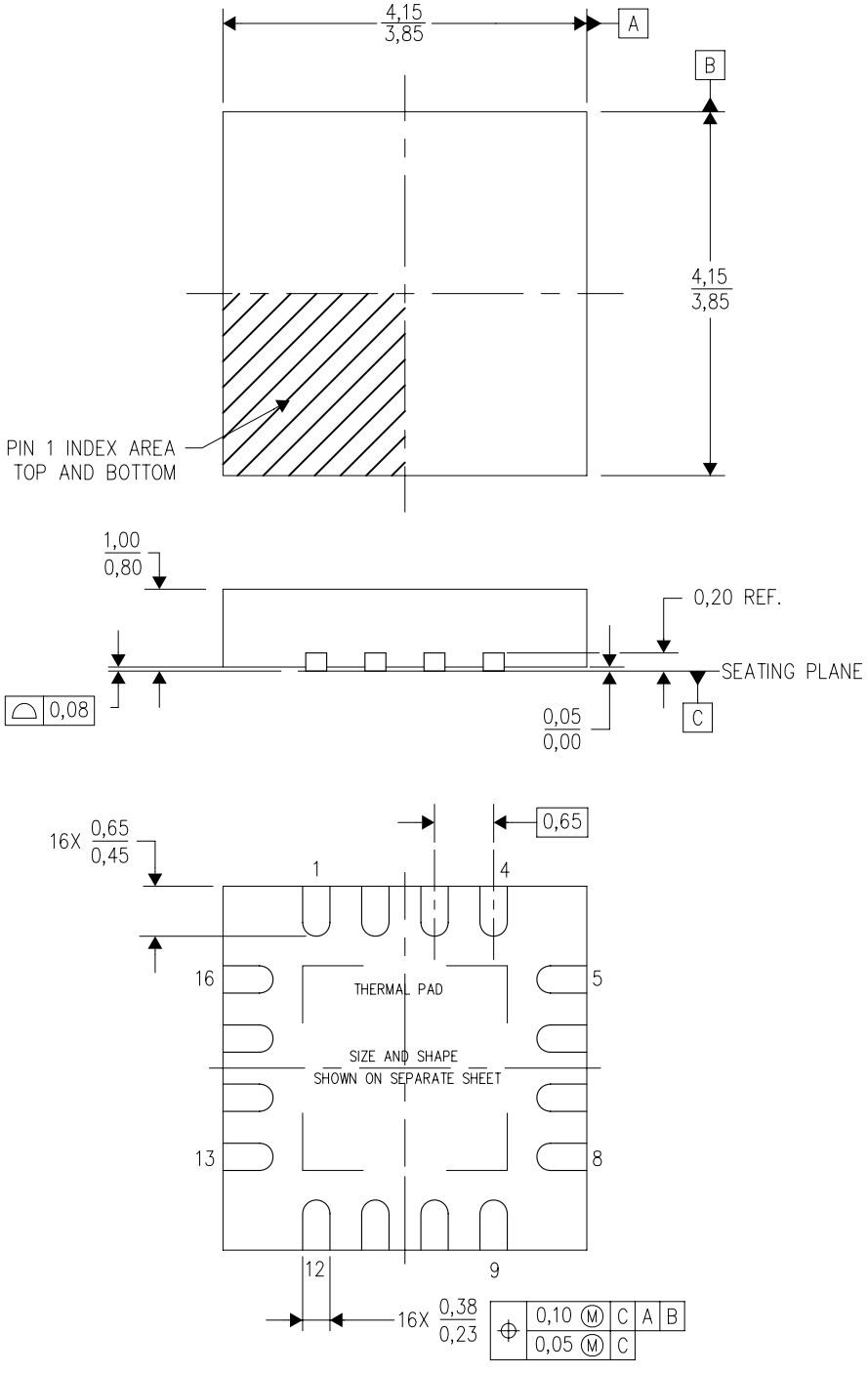
PLASTIC QUAD FLATPACK - NO LEAD




Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4224748/A

RGV (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD




NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

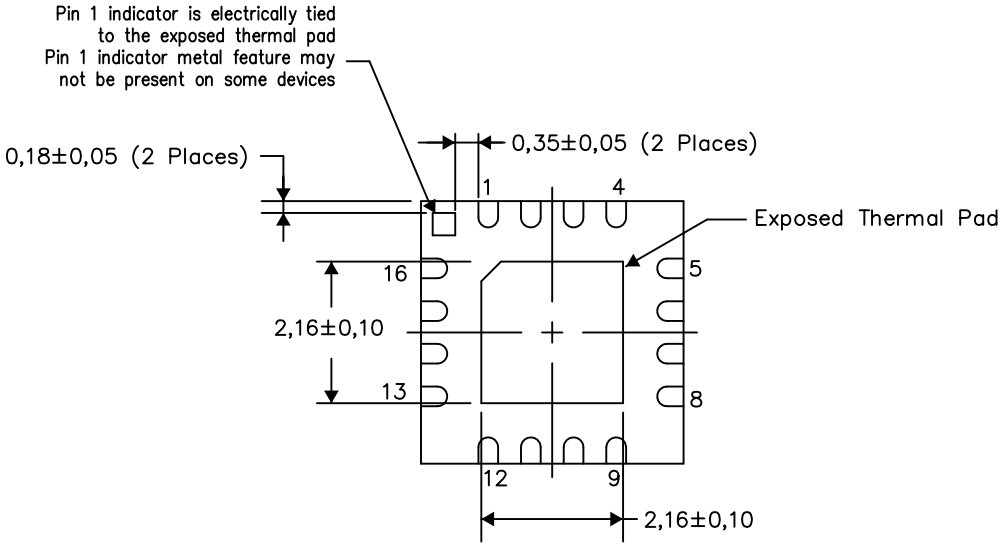
RGV (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



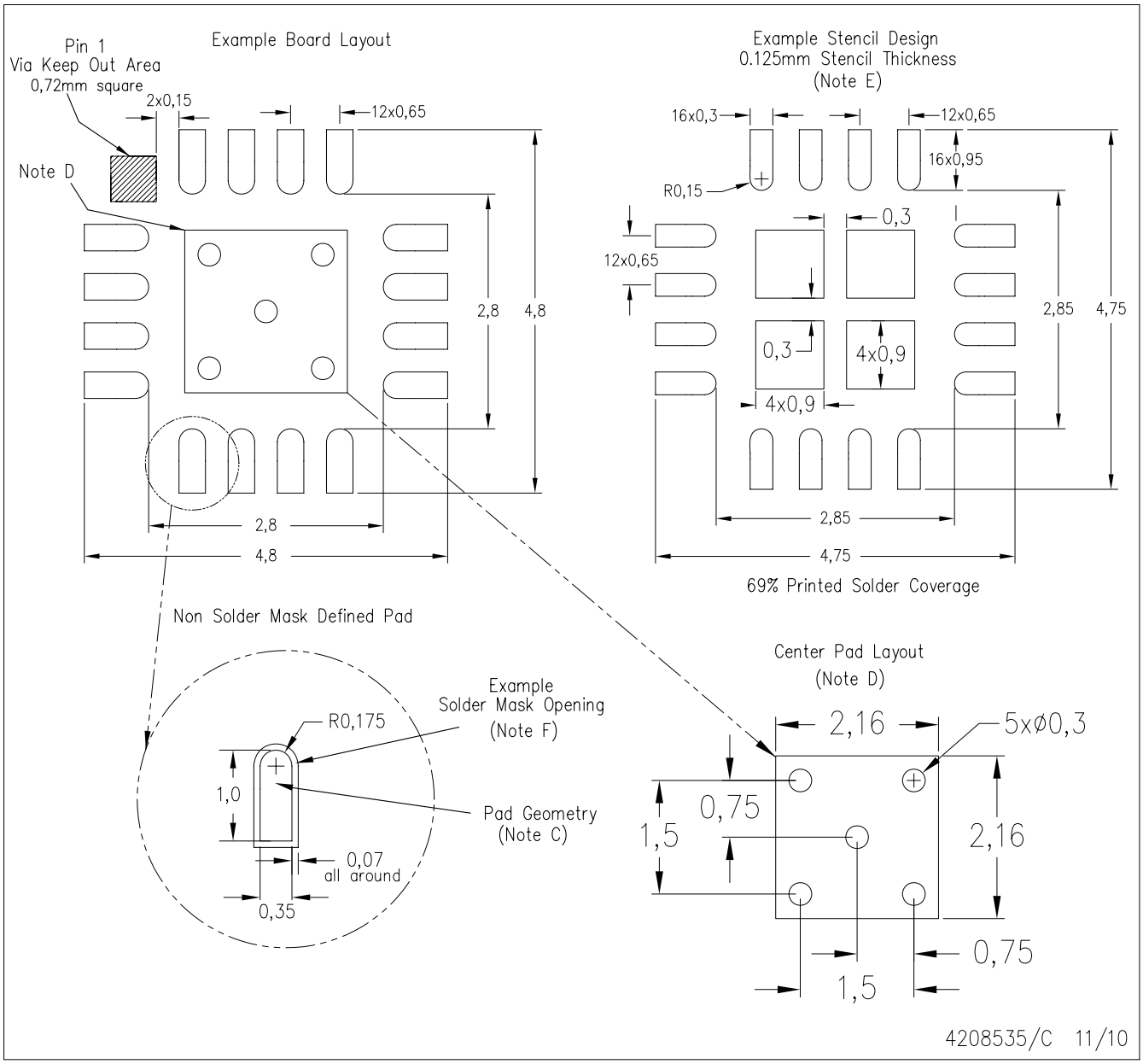

Bottom View

Exposed Thermal Pad Dimensions

4206351–2/L 05/13

NOTE: All linear dimensions are in millimeters

RGV (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



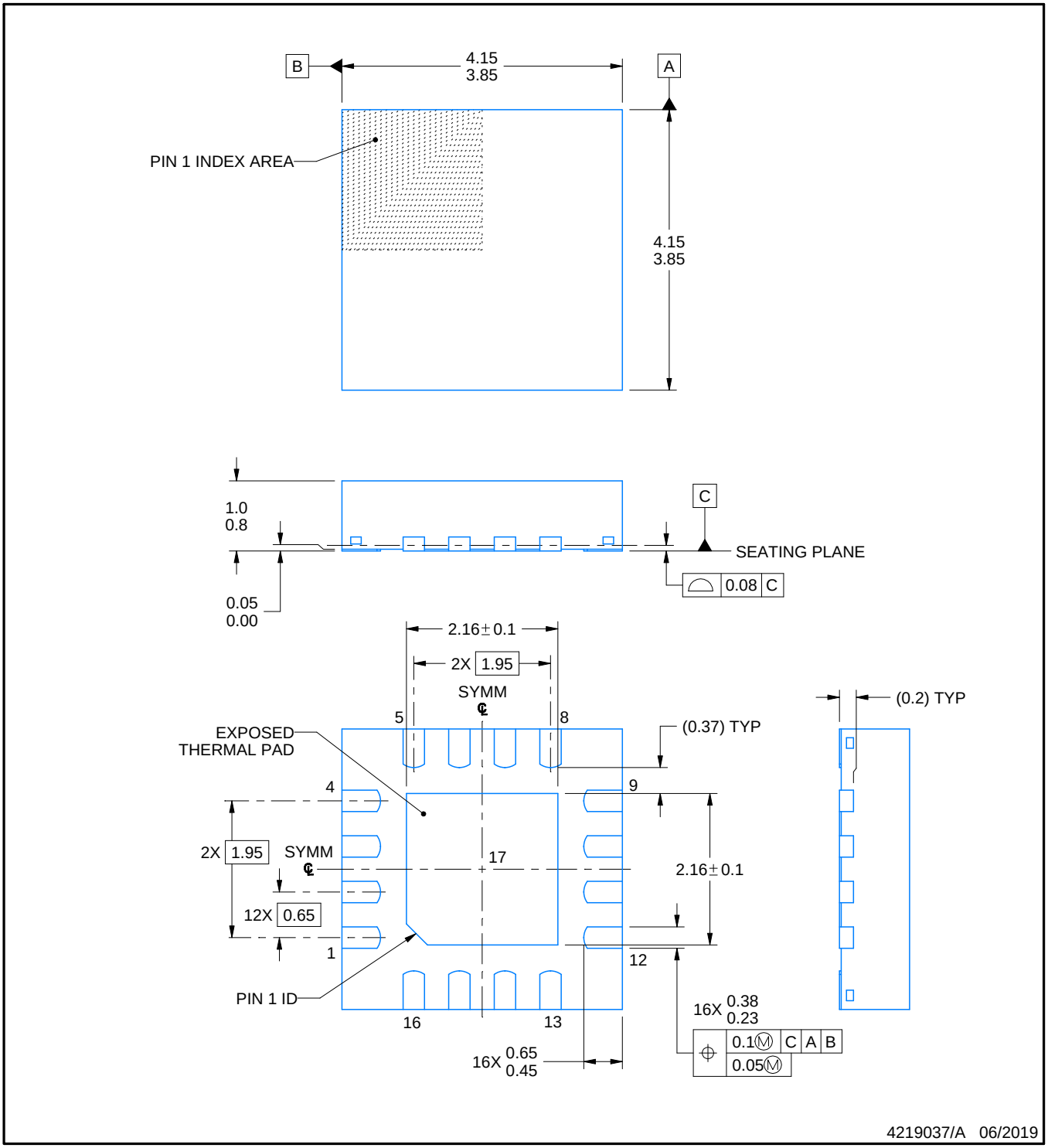

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

# RGV0016A

# PACKAGE OUTLINE

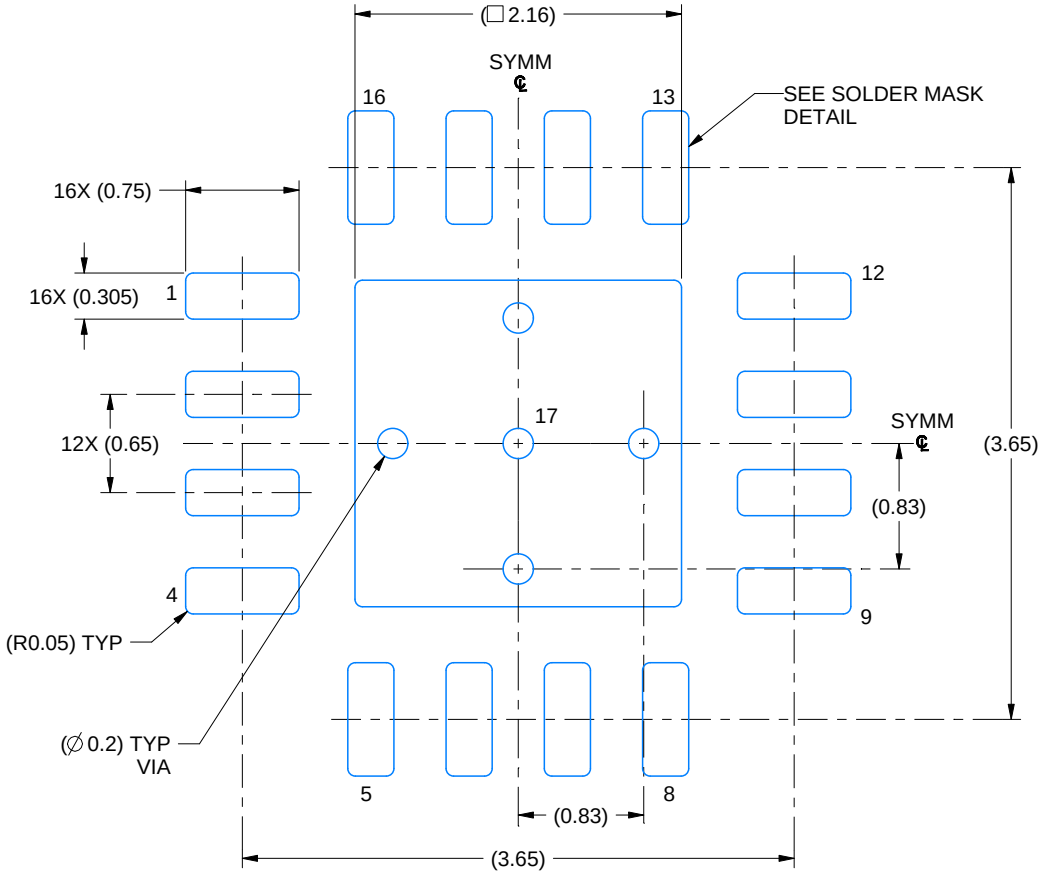
## VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

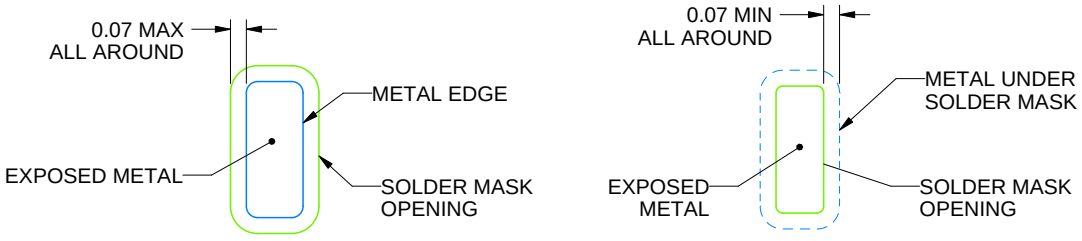



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X




NON SOLDER MASK DEFINED (PREFERRED)

SOLDER MASK DEFINED

SOLDER MASK DETAILS

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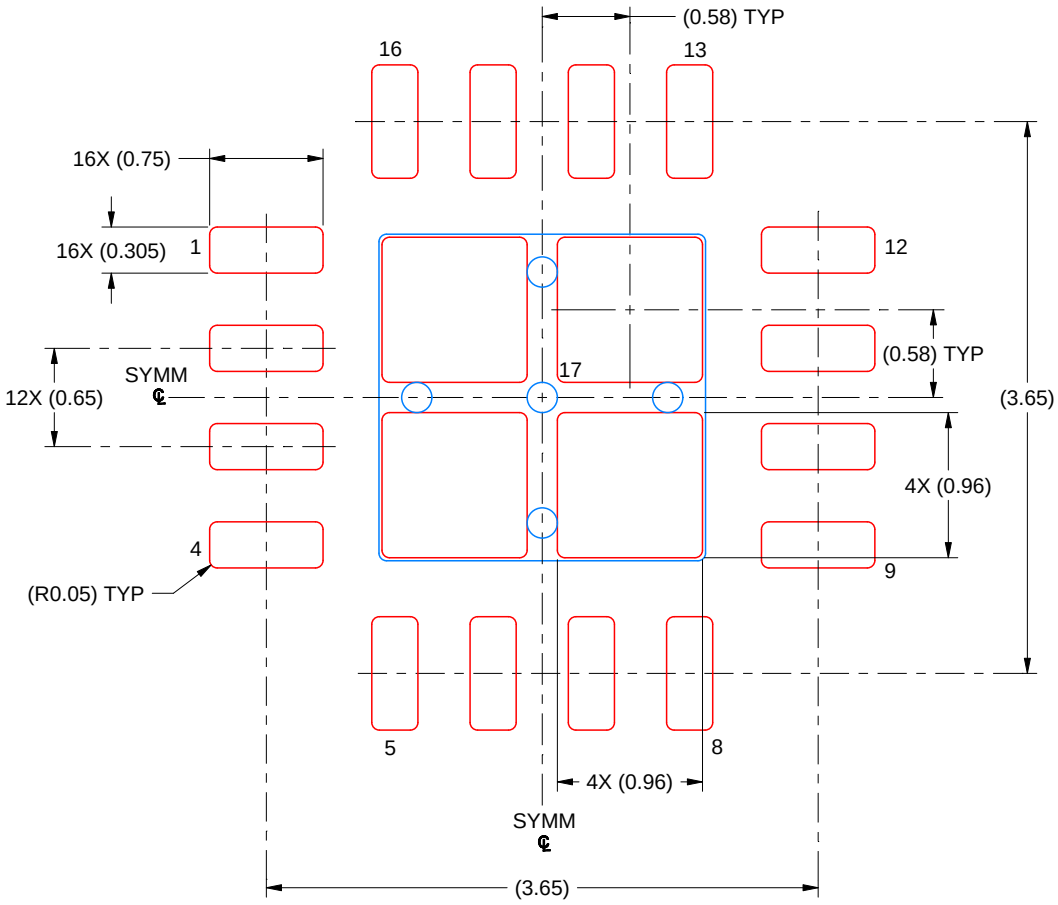
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.




SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 17
79% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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