

NSS20201MR6T1G

20 V, 3 A, Low $V_{CE(sat)}$ NPN Transistor

ON Semiconductor's e²PowerEdge family of low $V_{CE(sat)}$ transistors are miniature surface mount devices featuring ultra low saturation voltage ($V_{CE(sat)}$) and high current gain capability. These are designed for use in low voltage, high speed switching applications where affordable efficient energy control is important.

Typical application are DC-DC converters and power management in portable and battery powered products such as cellular and cordless phones, PDAs, computers, printers, digital cameras and MP3 players. Other applications are low voltage motor controls in mass storage products such as disc drives and tape drives. In the automotive industry they can be used in air bag deployment and in the instrument cluster. The high current gain allows e²PowerEdge devices to be driven directly from PMU's control outputs, and the Linear Gain (Beta) makes them ideal components in analog amplifiers.

MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$)

Rating	Symbol	Max	Unit
Collector-Emitter Voltage	V_{CEO}	20	V
Collector-Base Voltage	V_{CBO}	40	V
Emitter-Base Voltage	V_{EBO}	5.0	V
Collector Current – Continuous	I_C	2.0	A
Collector Current – Peak	I_{CM}	3.0	A

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Total Device Dissipation $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D (Note 1)	460 3.7	mW mW/ $^\circ\text{C}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$ (Note 1)	272	$^\circ\text{C}/\text{W}$
Total Device Dissipation $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D (Note 2)	780 6.3	mW mW/ $^\circ\text{C}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$ (Note 2)	160	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction-to-Lead #1	$R_{\theta JL}$ (Note 1) $R_{\theta JL}$ (Note 2)	48 40	$^\circ\text{C}/\text{W}$ $^\circ\text{C}/\text{W}$
Total Device Dissipation (Single Pulse < 10 s)	$P_{D\text{single}}$ (Note 2)	1.5	W
Junction and Storage Temperature Range	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

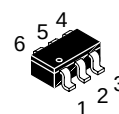
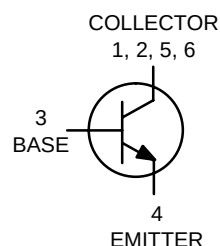
- FR-4 @ 100 mm², 2 oz copper traces.
- FR-4 @ 500 mm², 2 oz copper traces.



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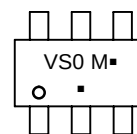
<http://onsemi.com>

**20 VOLTS
3.0 AMPS
NPN LOW $V_{CE(sat)}$ TRANSISTOR
EQUIVALENT $R_{DS(on)}$ 100 m Ω**



CASE 318G
TSOP-6
STYLE 6

DEVICE MARKING



VS0 = Specific Device Code
M = Date Code
■ = Pb-Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NSS20201MR6T1G	TSOP-6 (Pb-Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NSS20201MR6T1G

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector – Emitter Breakdown Voltage ($I_C = 10\text{ mA}$, $I_B = 0$)	$V_{(BR)CEO}$	20	–	–	V
Collector – Base Breakdown Voltage ($I_C = 0.1\text{ mA}$, $I_E = 0$)	$V_{(BR)CBO}$	40	–	–	V
Emitter – Base Breakdown Voltage ($I_E = 0.1\text{ mA}$, $I_C = 0$)	$V_{(BR)EBO}$	5.0	–	–	V
Collector Cutoff Current ($V_{CB} = 40\text{ V}$, $I_E = 0$)	I_{CBO}	–	–	0.1	μA
Collector – Emitter Cutoff Current ($V_{CES} = 20\text{ V}$)	I_{CES}	–	–	0.1	μA
Emitter Cutoff Current ($V_{EB} = 5.0\text{ V}$)	I_{EBO}	–	–	0.1	μA
ON CHARACTERISTICS					
DC Current Gain (Note 3) ($I_C = 1.0\text{ mA}$, $V_{CE} = 5.0\text{ V}$) ($I_C = 0.5\text{ A}$, $V_{CE} = 5.0\text{ V}$) ($I_C = 1.0\text{ A}$, $V_{CE} = 5.0\text{ V}$)	h_{FE}	300 300 200	– – –	– – –	
Collector – Emitter Saturation Voltage (Note 3) ($I_C = 1.0\text{ A}$, $I_B = 100\text{ mA}$) ($I_C = 0.5\text{ A}$, $I_B = 50\text{ mA}$) ($I_C = 0.1\text{ A}$, $I_B = 10\text{ mA}$)	$V_{CE(sat)}$	– – –	– – –	0.150 0.100 0.025	V
Base – Emitter Saturation Voltage (Note 3) ($I_C = 1.0\text{ A}$, $I_B = 0.1\text{ A}$)	$V_{BE(sat)}$	–	–	0.95	V
Base – Emitter Turn-on Voltage (Note 3) ($I_C = 1.0\text{ A}$, $V_{CE} = 2.0\text{ V}$)	$V_{BE(on)}$	–	–	0.90	V
Cutoff Frequency ($I_C = 100\text{ mA}$, $V_{CE} = 5.0\text{ V}$, $f = 100\text{ MHz}$)	f_T	200	–	–	MHz
Output Capacitance ($f = 1.0\text{ MHz}$)	C_{obo}	–	–	15	pF

3. Pulsed Condition: Pulse Width $\leq 300\text{ }\mu\text{sec}$, Duty Cycle $\leq 2\%$.

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

ON Semiconductor®



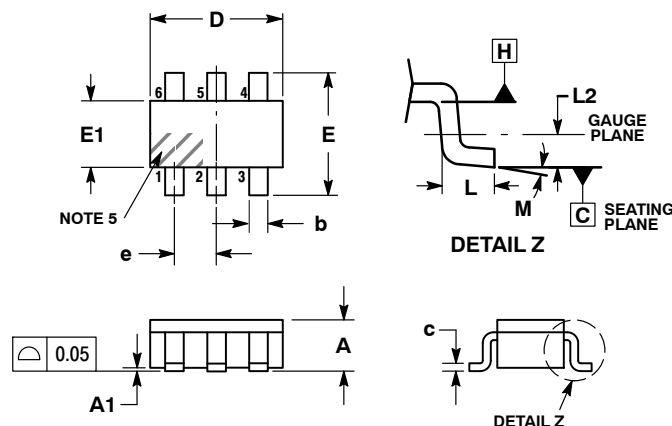
SCALE 2:1

TSOP-6

CASE 318G-02

ISSUE V

DATE 12 JUN 2012



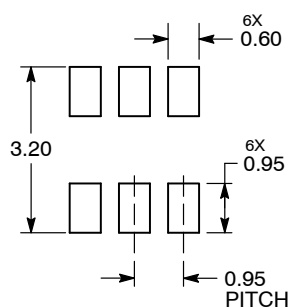
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
5. PIN ONE INDICATOR MUST BE LOCATED IN THE INDICATED ZONE.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.01	0.06	0.10
b	0.25	0.38	0.50
c	0.10	0.18	0.26
D	2.90	3.00	3.10
E	2.50	2.75	3.00
E1	1.30	1.50	1.70
e	0.85	0.95	1.05
L	0.20	0.40	0.60
L2	0.25 BSC		
M	0°	—	10°

STYLE 1: PIN 1. DRAIN 2. DRAIN 3. GATE 4. SOURCE 5. DRAIN 6. DRAIN	STYLE 2: PIN 1. EMITTER 2 2. BASE 1 3. COLLECTOR 1 4. EMITTER 1 5. BASE 2 6. COLLECTOR 2	STYLE 3: PIN 1. ENABLE 2. N/C 3. R BOOST 4. Vz 5. V in 6. V out	STYLE 4: PIN 1. N/C 2. V in 3. NOT USED 4. GROUND 5. ENABLE 6. LOAD	STYLE 5: PIN 1. EMITTER 2 2. BASE 2 3. COLLECTOR 1 4. EMITTER 1 5. BASE 1 6. COLLECTOR 2	STYLE 6: PIN 1. COLLECTOR 2. COLLECTOR 3. BASE 4. EMITTER 5. COLLECTOR 6. COLLECTOR
STYLE 7: PIN 1. COLLECTOR 2. COLLECTOR 3. BASE 4. N/C 5. COLLECTOR 6. EMITTER	STYLE 8: PIN 1. Vbus 2. D(in) 3. D(in)+ 4. D(out)+ 5. D(out) 6. GND	STYLE 9: PIN 1. LOW VOLTAGE GATE 2. DRAIN 3. SOURCE 4. DRAIN 5. DRAIN 6. HIGH VOLTAGE GATE	STYLE 10: PIN 1. D(OUT)+ 2. GND 3. D(OUT)- 4. D(IN)- 5. VBUS 6. D(IN)+	STYLE 11: PIN 1. SOURCE 1 2. DRAIN 2 3. DRAIN 2 4. SOURCE 2 5. GATE 1 6. DRAIN 1/GATE 2	STYLE 12: PIN 1. I/O 2. GROUND 3. I/O 4. I/O 5. VCC 6. I/O
STYLE 13: PIN 1. GATE 1 2. SOURCE 2 3. GATE 2 4. DRAIN 2 5. SOURCE 1 6. DRAIN 1	STYLE 14: PIN 1. ANODE 2. SOURCE 3. GATE 4. CATHODE/DRAIN 5. CATHODE/DRAIN 6. CATHODE/DRAIN	STYLE 15: PIN 1. ANODE 2. SOURCE 3. GATE 4. DRAIN 5. N/C 6. CATHODE	STYLE 16: PIN 1. ANODE/CATHODE 2. BASE 3. EMITTER 4. COLLECTOR 5. ANODE 6. CATHODE	STYLE 17: PIN 1. EMITTER 2. BASE 3. ANODE/CATHODE 4. ANODE 5. CATHODE 6. COLLECTOR	

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
 A = Assembly Location
 Y = Year
 W = Work Week
 ■ = Pb-Free Package

XXX = Specific Device Code
 M = Date Code
 ■ = Pb-Free Package

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

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