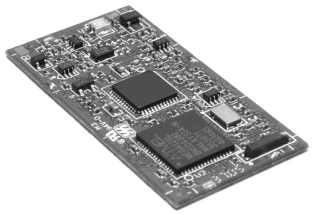
CIRRONET

LPR2400ER

High Power 802.15.4 Module

- ***2.4 GHz Spread Spectrum Transceiver Module***
- ***Supports Multiple Network Topologies***
- ***Small Size, Light Weight, +18 dBm Transmitter Power***
- ***FCC and ETSI Certified for Unlicensed Operation***

The LPR2400ER 2.4 GHz transceiver module is a low cost, high-power solution for peer-to-peer, point-to-point and point-to-multipoint wireless designs. LPR2400ER modules provide the flexibility and versatility to serve applications ranging from cable replacements to sensor networks. Based on the IEEE 802.15.4 wireless standard, the LPR2400ER module is easy to integrate and provides robust wireless communications in applications where full MESH network operation is not required. The LPR2400 also inclues Cirronet's Network Layer (CNL) firmware which features a flexible and simple-to-use Application Programming Interface.



Show with Shield Removed

LPR2400ER Absolute Maximum Ratings

Rating	Value	Units
All Input/Output Pins	-0.3 to +6.0	V
Non-Operating Ambient Temperature Range	-40 to +85	°C

LPR2400ER Electrical Characteristics

Characteristic	Sym	Notes	Minimum	Typical	Maximum	Units
Operating Frequency Range			2405		2480	MHz
Operating Frequency Tolerance			-300		300	kHz
Spread Spectrum Method				Direct Sequence		
Modulation Type				O-QPSK		
Number of RF Channels				16		
RF Data Transmission Rate				250		kb/s
Symbol Rate Tolerance					120	ppm
RF Channel Spacing				5		MHz
Receiver Sensitivity, 10^{-5} BER				-95		dBm
Upper Adjacent Channel Rejection, +5 MHz				46		dB
Lower Adjacent Channel Rejection, -5 MHz				39		dB
Upper Alternate Channel Rejection, +10 MHz				58		dB
Lower Alternate Channel Rejection, -10 MHz				55		dB
Maximum RF Transmit Power			16	17	18	dBm
Transmit Power Adjustment					-25	dB
Optimum Antenna Impedance				50		Ω

LPR2400ER Electrical Characteristics

Characteristic	Sym	Notes	Minimum	Typical	Maximum	Units
ADC Input Range			0		2.5	V
ADC Input Resolution					10	bits
ADC Input Impedance			55			MΩ
PWM Output Resolution					12	bits
UART Baud Rate			1.2		115.2	kb/s
Digital I/O:						
Logic Low Input Level			-0.5		0.64	V
Logic High Input Level			1.98		3.7	V
Logic Input Internal Pull-up Resistor			20			KΩ
Logic Low Output Level, I_{SINK} = 10 mA					0.5	V
Logic High Output Level			2.4			V
Logic Low Output Sink Current	I_{SINK}				20	mA
Logic High Output Source Current	I_{SOURCE}				5	mA
Power Supply Voltage Range	V_{CC}		+3.3		+5.5	Vdc
Power Supply Voltage Ripple					10	mV_{P-P}
Receive Mode Current				50		mA
Transmit Mode Current				150		mA
Sleep Mode Current				25		µA
Operating Temperature Range			-40		85	°C

CAUTION: Electrostatic Sensitive Device. Observe precautions when handling.

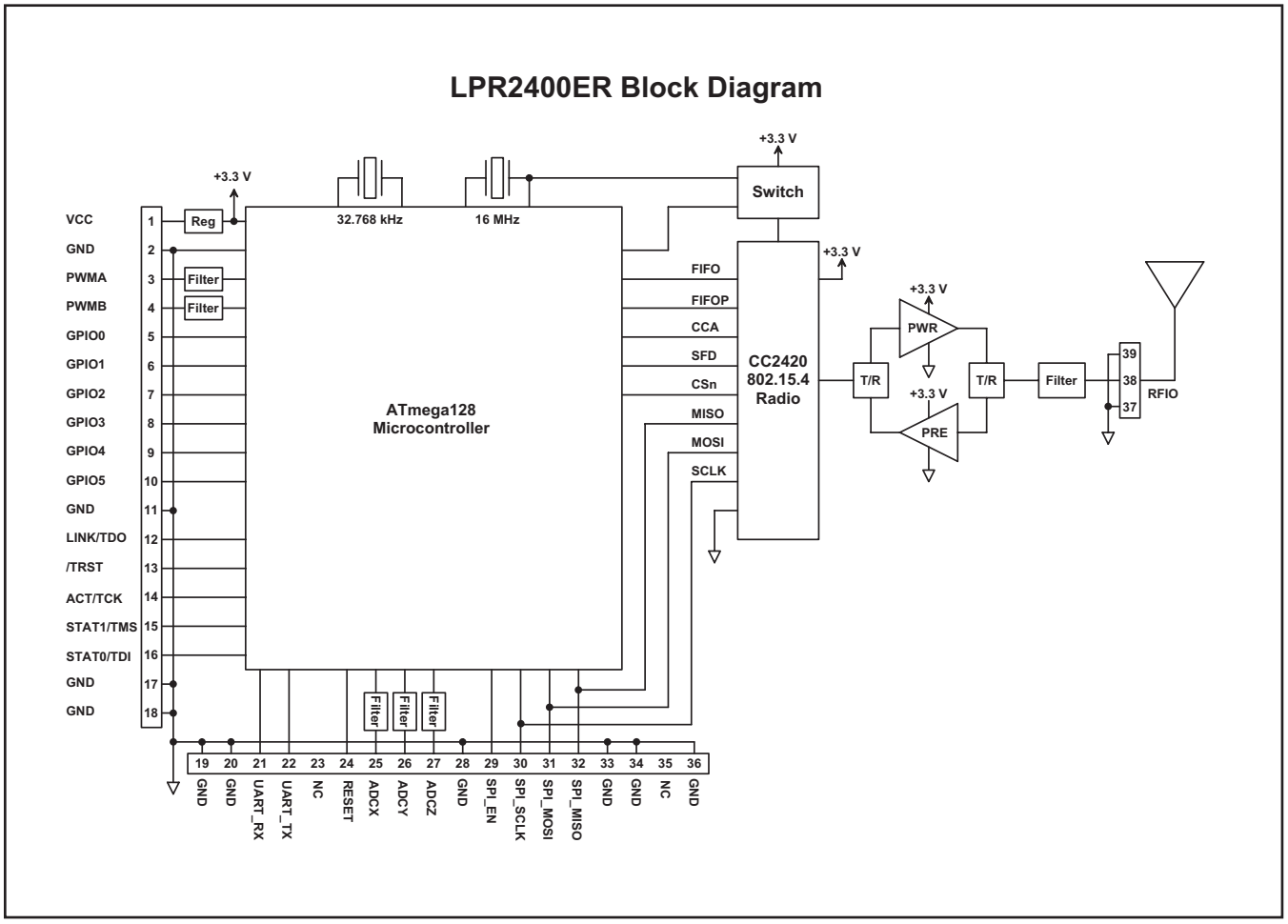


Figure 1

LPR2400ER Hardware

The major hardware components of the LPR2400ER include a CC2420 IEEE 802.15.4 compatible transceiver and an ATmega128 microcontroller. The LPR2400ER operates in the frequency band of 2405 to 2460 MHz at a nominal output power of 63 mW.

The CC2420 transceiver receives a 16 MHz reference clock through an IC switch controlled by the ATmega microcontroller, which allows the transceiver to be idled during sleep periods. SPI signals provide the main interface between the transceiver and microcontroller. The SPI signals are supplemented by *FIFO* and *FIFOP* transceiver buffer status signals, the *CCA* clear channel assessment signal, and the *SFD* start of frame delimiter signal.

In addition to controlling the CC2420, the ATmega128 provides a variety of application hardware interfaces including an SPI interface, UART interface, three 10-bit ADC inputs, two PWM (DAC) outputs, and six general purpose digital I/O ports.

LPR2400ER Firmware

The main firmware components in the LPR2400ER include the 802.15.4 Media Access Control (MAC) layer and the Cirronet Networking Layer (CNL). CNL supports peer-to-peer, point-to-point, and point-to-multipoint communications. CNL networks can deploy up to 60 single-hop routers and can support an unlimited number of remotes. The CNL Application Programming Interface (API) provides an easy-to-use, flexible set of application commands and functions. See the *LPR2400/LPR2400ER Integration Guide* for complete details of the CNL API.

LPR2400ER I/O Pads - Some I/O Pad Functionality Depends on the Firmware Version Installed.

Pad	Name	Description
1	VCC	Power supply input, +3.3 to +5.5 Vdc.
2	GND	Power supply and signal ground. Connect to the host circuit board ground.
3	PWMA	Pulse-width modulated output A. Provides a DAC function when used with an external low-pass filter.
4	PWMB	Pulse-width modulated output B. Provides a DAC function when used with an external low-pass filter.
5	GPIO0	Configurable digital I/O port 0. When configured as an output, the power-on state is also configurable.
6	GPIO1	Configurable digital I/O port 1. When configured as an output, the power-on state is also configurable.
7	GPIO2	Configurable digital I/O port 2. When configured as an output, the power-on state is also configurable.
8	GPIO3	Configurable digital I/O port 3. When configured as an output, the power-on state is also configurable.
9	GPIO4	Configurable digital I/O port 4. When configured as an output, the power-on state is also configurable.
10	GPIO5	Configurable digital I/O port 5. When configured as an output, the power-on state is also configurable.
11	GND	Power supply and signal ground. Connect to the host circuit board ground.
12	LINK/TDO	Output signal indicating module's link status in default mode. Also used by JTAG interface as Test Data Output.
13	/TRST	Used by JTAG interface as active low Reset input. Leave disconnected if JTAG interface will not be used.
14	ACT/TCK	Output signal indicating RF data activity. Also used by JTAG interface as Data Clock Input.
15	STAT1/TMS	Output signal defined by firmware version. Also used to select JTAG mode.
16	STAT0/TDI	Output signal defined by firmware version. Also used by JTAG interface as Test Data Input.
17 - 20	GND	Power supply and signal grounds. Connect to the host circuit board ground.
21	UART_RX	Serial data input to UART.
22	UART_TX	Serial data output from UART.
23	NC	No connection.
24	/RESET	Active low module hardware reset input. This input must be held low when the power supply input is in the range of +1.5 to +2.7 Vdc.
25	ADCX	10-bit ADC input X. Input voltage range is 0 to +2.5 Vdc.
26	ADCY	10-bit ADC input Y. Input voltage range is 0 to +2.5 Vdc.
27	ADCZ	10-bit ADC input Z. Input voltage range is 0 to +2.5 Vdc.
28	GND	Power supply and signal ground. Connect to the host circuit board ground.
29	SPI_EN	Active-low enable output for SPI bus devices.
30	SPI_SCLK	SPI port clock signal.
31	SPI_MOSI	SPI port data output.
32	SPI_MISO	SPI port data input.
33	GND	Power supply and signal ground. Connect to the host circuit board ground.
34	GND	Power supply and signal ground. Connect to the host circuit board ground.
35	NC	No connection.
36	GND	Power supply and signal ground. Connect to the host circuit board ground.
37	GND	RF ground. Connect to the host circuit board ground plane, and to shield when using coaxial cable.
38	RFIO	RF port. Connect the antenna to this port with a 50 Ω stripline or semi-rigid coaxial cable.

Pad	Name	Description
39	GND	RF ground. Connect to the host circuit board ground plane, and to shield when using coaxial cable.

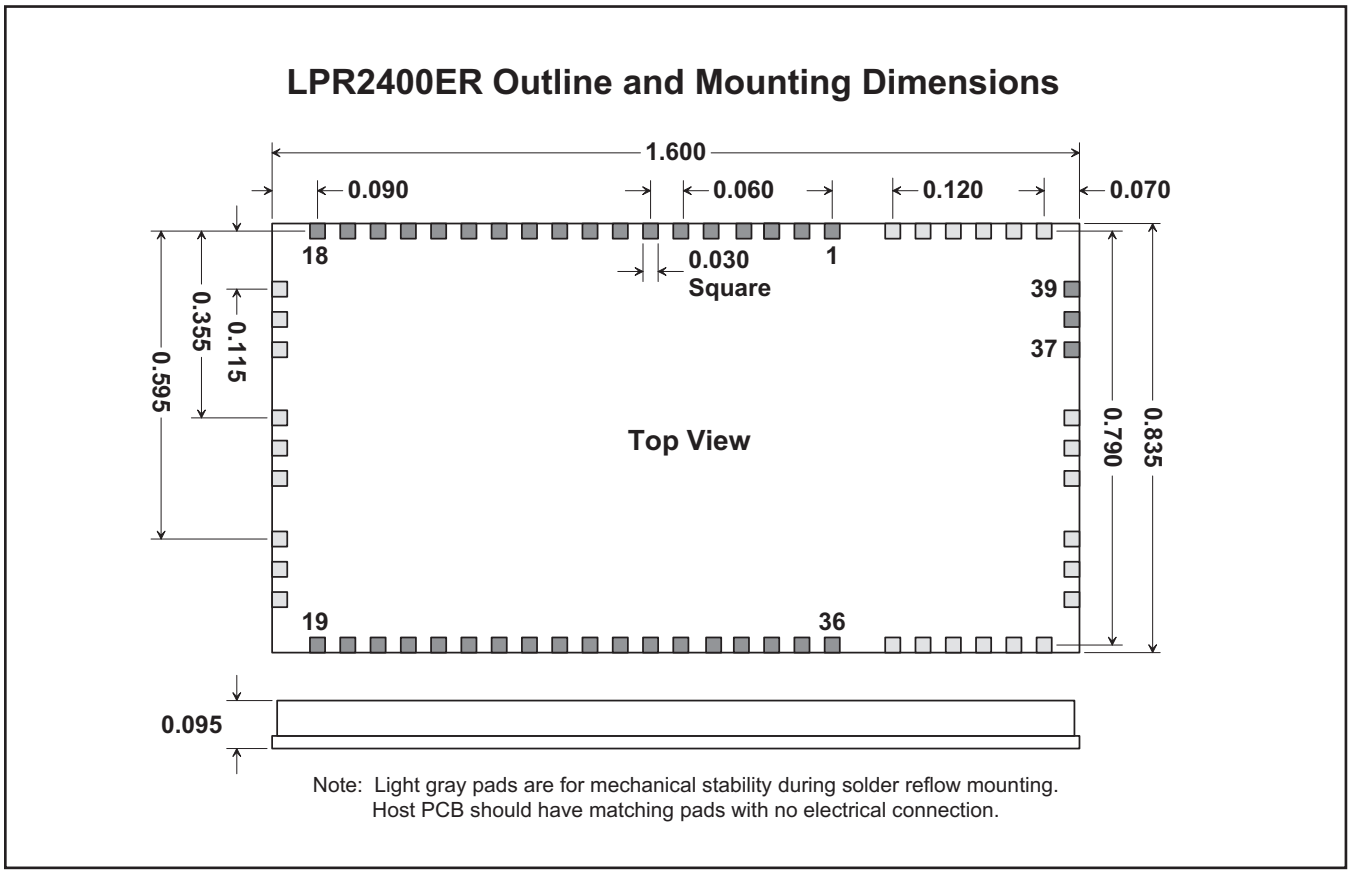


Figure 2

RFIO Stripline

The RFIO pad on the radio module is connected directly to an antenna on the host circuit board, or to an MMCX or similar RF connector. It is important that this connection be implemented as a 50 ohm stripline. Referring to Figure 3, the width of this stripline depends on the thickness of the circuit board between the stripline and the

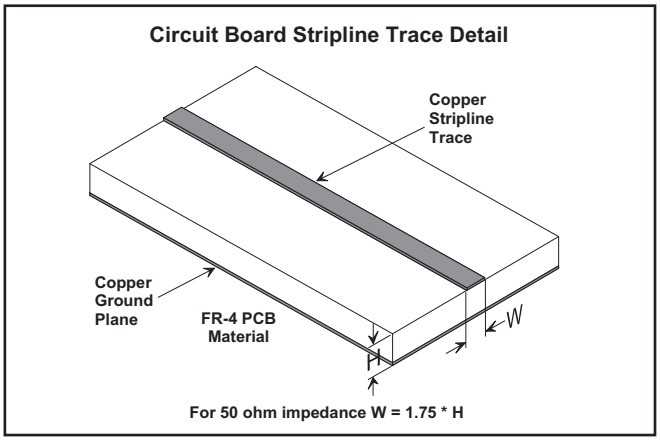
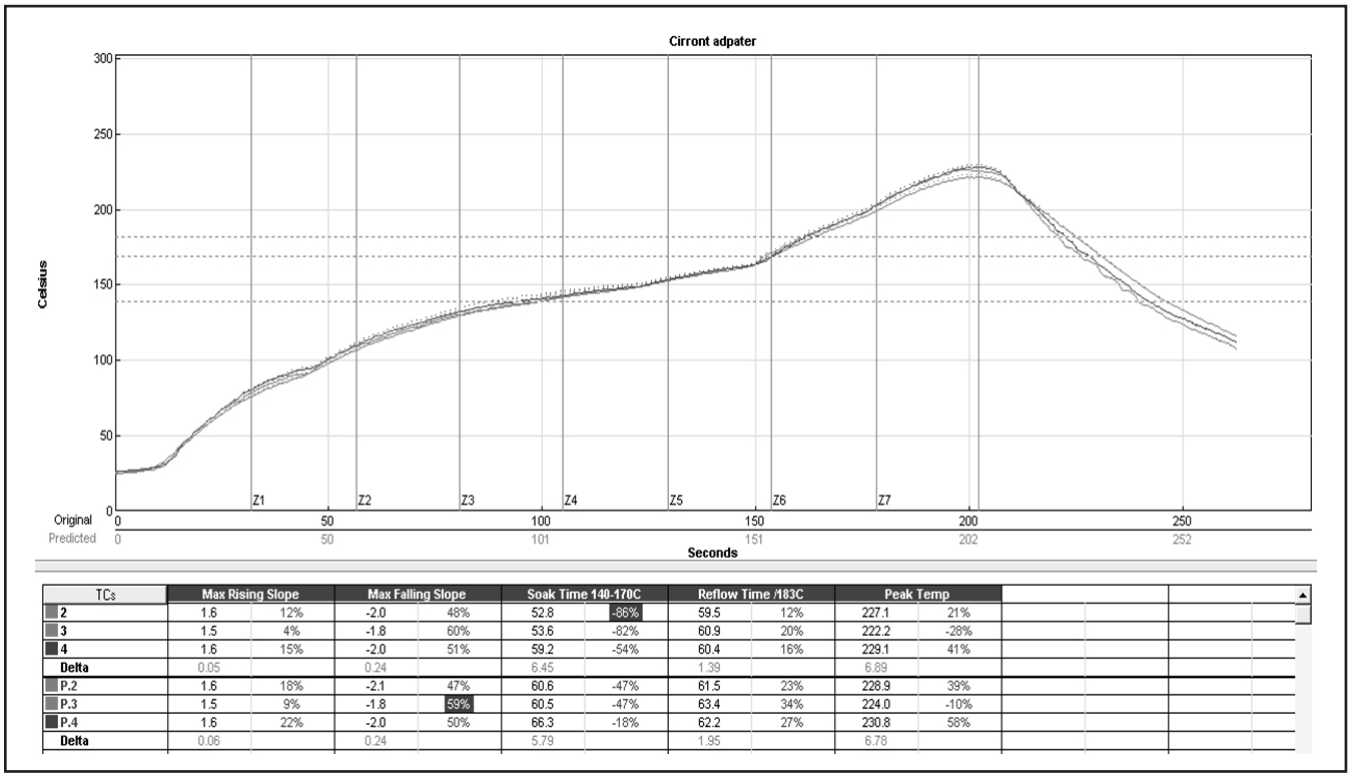


Figure 3

Trace Separation from 50 Ohm Microstrip	Length of Trace Run Parallel to Microstrip
100 mil	125 mil
150 mil	200 mil
200 mil	290 mil
250 mil	450 mil
300 mil	650 mil

Figure 4

groundplane. For FR-4 type circuit board materials (dielectric constant of 4.7), the width of the stripline is equal to 1.75 times the thickness of the circuit board. Note that other circuit board traces should be spaced away from the stripline to prevent signal coupling, as shown in Figure 4. The stipline trace should be kept short to minimize its insertion loss.



TCs	Max Rising Slope		Max Falling Slope		Soak Time 140-170C		Reflow Time /183C		Peak Temp	
2	1.6	12%	-2.0	48%	52.8	-86%	59.5	12%	227.1	21%
3	1.5	4%	-1.8	60%	53.6	-82%	60.9	20%	222.2	-28%
4	1.6	15%	-2.0	51%	59.2	-54%	60.4	16%	229.1	41%
Delta	0.05		0.24		6.45		1.39		6.89	
P.2	1.6	18%	-2.1	47%	60.6	-47%	61.5	23%	228.9	39%
P.3	1.5	9%	-1.8	59%	60.5	-47%	63.4	34%	224.0	-10%
P.4	1.6	22%	-2.0	50%	66.3	-18%	62.2	27%	230.8	58%
Delta	0.06		0.24		5.79		1.95		6.78	

Figure 5

Reflow Profile

An example solder reflow profile for mounting the radio module on its host circuit board is shown in Figure 5.

Note: Specifications subject to change without notice.

file: lpr2400er_g.vp, 2007.02.09 rev

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