

## **DACx760EVM and DACx750EVM**

This user's guide describes the characteristics, operation, and use of the DAC7750 and DAC8750 (DACx750), and the DAC7760, and DAC8760 (DACx760) evaluation boards (EVMs). This user's guide also discusses how to set up and configure the software and hardware, and reviews various aspects of the program operation. Throughout this document, the terms *DAC8760EVM*, *evaluation board*, *evaluation module*, and *EVM* are synonymous with the DACx760EVM and DACx760EVM. This user's guide also includes information regarding operating procedures and input/output connections, an electrical schematic, printed circuit board (PCB) layout drawings, and a parts list for the EVM.

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## 1 Overview

The DAC7760 (12-bit) and DAC8760 (16-bit) are precision digital-to-analog converters (DACs). The output can be configured to produce a current in output ranges of 0 mA to 20 mA, 4 mA to 20 mA, and 4 mA to 24 mA. Both devices can also be configured to have voltage output ranges of 0 V to 5 V, 0 V to 10 V,  $\pm 5$  V, and  $\pm 10$  V. The DAC7750 (12-bit) and DAC8750 (16-bit) feature current outputs only. All of these devices feature configurable slew rates, power-on reset functions, a highway addressable remote transducer (HART) signal interface, a watchdog timer, error checking, external and internal voltage references, and a common hardware fault output.

### 1.1 EVM Kit Contents

Table 1 details the contents of the EVM kit. Contact the Texas Instruments Product Information Center nearest you if any component is missing. It is highly recommended that you check the TI web site at <http://www.ti.com> to verify that you have the latest versions of the related software.

**Table 1. Contents of DACx760EVM and DACx750EVM Kit**

Item	Quantity
DACx760EVM or DACx750EVM PCB	1
SM-USB-DIG platform PCB	1
USB extender cable	1
SM-USB-DIG connector ribbon cable	1
User's guide CD-ROM	1

### 1.2 Related Documentation from Texas Instruments

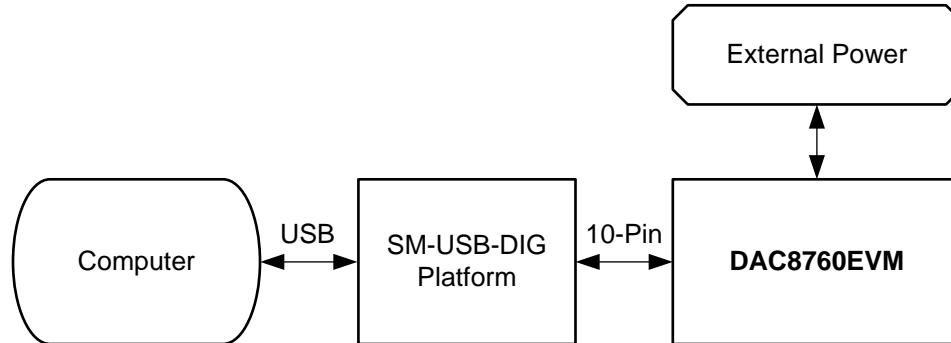
The following documents provide information regarding Texas Instruments integrated circuits used in the assembly of the DACx760EVM and DACx750EVM. This user's guide is available from the TI web site under literature number [SBAU205](#). Any letter appended to the literature number corresponds to the document revision that is current at the time of the writing of this document. Newer revisions may be available from the TI web site at <http://www.ti.com/>, or call the Texas Instruments Literature Response Center at (800) 477-8924 or the Product Information Center at (972) 644-5580. When ordering, identify the document by both title and literature number.

**Table 2. Related Documentation**

Document	Literature Number
DAC7760 and DAC8760 product data sheet	<a href="#">SBAS528</a>
DAC7750 and DAC8750 product data sheet	<a href="#">SBAS538</a>
REF02 product data sheet	<a href="#">SBVS003</a>
SM-USB-DIG Platform User's Guide	<a href="#">SBOU98</a>

## 2 EVM Hardware Setup

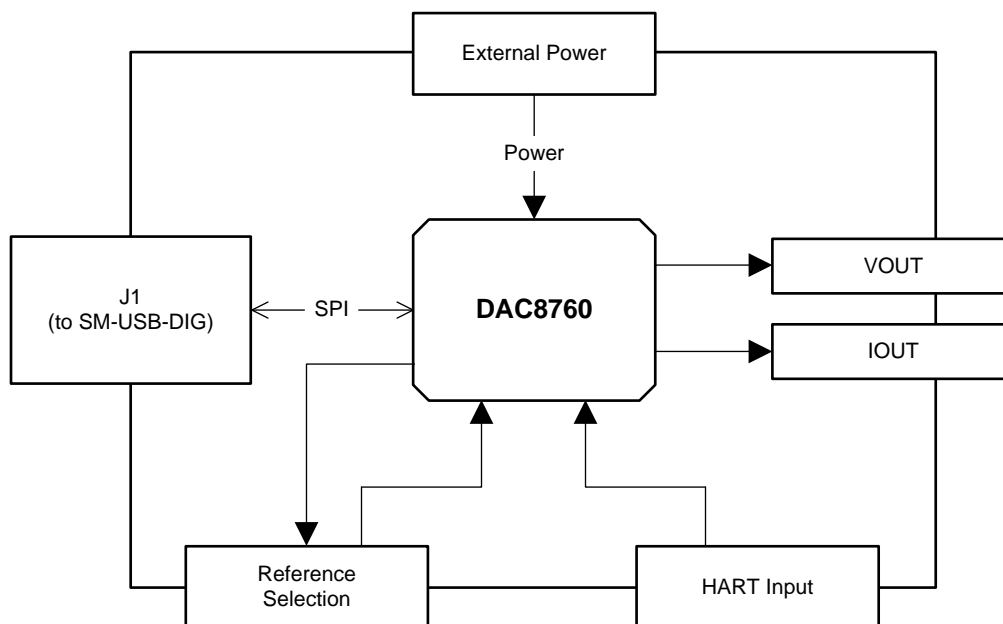
This section discusses the overall system setup for the EVM. A personal computer (PC) runs the software that communicates with the SM-USB-DIG Platform, which provides the power and digital signals used to communicate with the EVM board. Connectors on the EVM board allow the user to connect the required external power supply.



**Figure 1. DAC8760EVM Hardware Setup**

### 2.1 Theory of Operation for EVM Hardware

A block diagram of the EVM hardware setup is shown in [Figure 2](#). This board provides test points for the SPI™ inputs, power, reference, ground connections, ALARM, CLR, BOOST, and the analog outputs of the DAC. Note that DACx750 only features current outputs (IOUT), but also includes a test point for R3-SENSE.



**Figure 2. DAC8760EVM Block Diagram**

## 2.2 Signal Definitions of J1 (10-Pin Male Connector Socket)

Table 3 shows the pinout for the 10-pin connector socket used to communicate between the EVM and the SM-USB-DIG. Note that the I<sup>2</sup>C communications lines (I2C\_SCL and I2C\_SDA1) are not used.

Table 3. SM-USB-DIG Connector

Pin On U1	Signal	Description
1	I2C_SCL	I2C Clock Signal (SCL)
2	CTRL/MEAS4	GPIO – Control Output or Measure Input
3	I2C_SDA1	I2C Data Signal (SDA)
4	CTRL/MEAS5	GPIO – Control Output or Measure Input
5	SPI_DOUT1	SPI Data Output (MOSI)
6	VDUT	Switchable DUT Power Supply: +3.3V, +5V, Hi-Z (Disconnected). Note: When VDUT is Hi-Z all Digital I/O are Hi-Z as well.
7	SPI_CLK	SPI Clock Signal (SCLK)
8	GND	Power Return (GND)
9	SPI_CS1	SPI Chip Select Signal ( $\overline{CS}$ )
10	SPI_DIN1	SPI Data Input (MISO)

## 2.3 Theory of Operation for SM-USB-DIG Platform

Figure 3 shows the block diagram for the SM-USB-DIG Platform. This platform is a general-purpose data-acquisition system that is used on several different Texas Instruments evaluation modules. The details of operation are included in [SBOU098](#), *SM-USB-DIG Platform User's Guide*. The block diagram shown in Figure 3 is given as a brief overview of the platform.

The primary component of the SM-USB-DIG Platform is the TUSB3210, an 8052 microcontroller that has a built-in USB interface. The microcontroller receives information from the host computer that is interpreted into power, I<sup>2</sup>C, SPI, and other digital I/O patterns. During the digital I/O transaction, the microcontroller reads the response of any device connected to the I/O interface. The response from the device is then sent back to the computer where it is interpreted by the host computer.

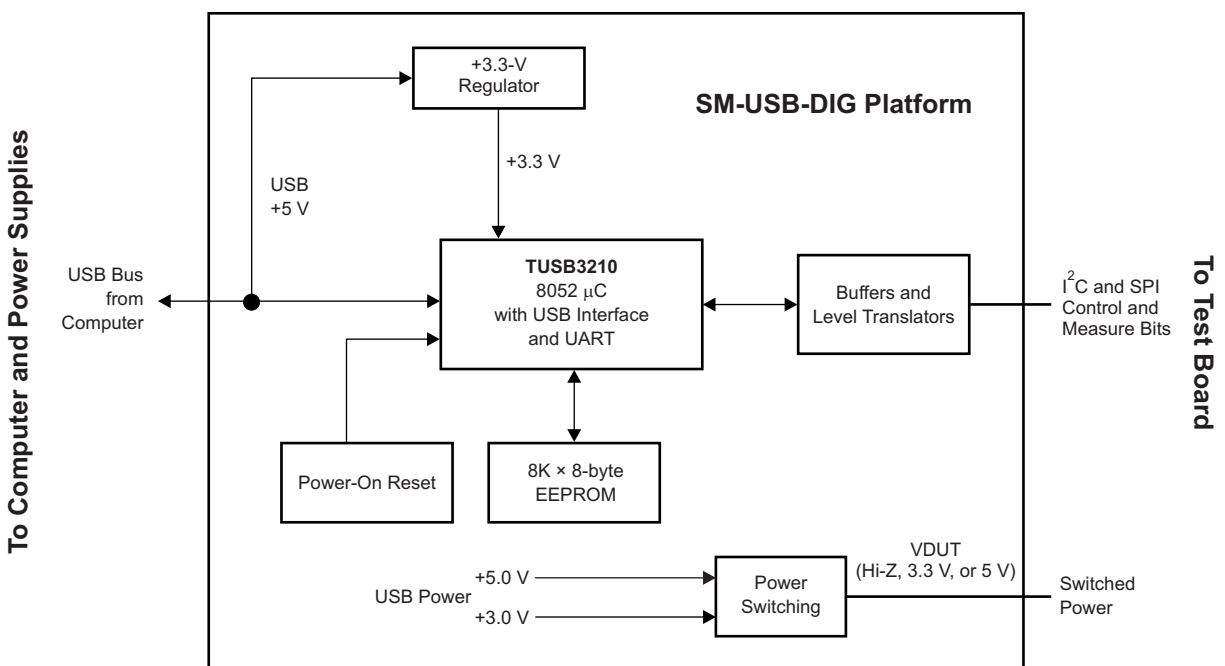


Figure 3. USB-DIG Platform Block Diagram

### 3 EVM Hardware Overview

To use the EVM hardware, set the jumpers, connect the SM-USB-DIG and the EVM together, apply external power, and connect the USB cable from the SM-USB-DIG to the computer. This section presents the details of these procedures.

#### 3.1 Electrostatic Discharge Warning

Many of the components on the EVM are susceptible to damage by electrostatic discharge (ESD). Customers are advised to observe proper ESD handling precautions when unpacking and handling the EVM, including the use of a grounded wrist strap at an approved ESD workstation.

#### 3.2 Jumper Summary

Table 4 summarizes all of the EVM jumper functionality.

**Table 4. EVM Jumper Summary**

Pin On U1	Signal
JP1	When JP1 is installed, AVSS is shorted to ground.
JP2	When JP2 is in the 1-2 (right) position, RSET is used for the HART input path. When JP2 is in the 2-3 (left) position, HART-IN is used for the HART input path.
JP3	When JP3 is uninstalled, the DACx760 or DACx750 provide DVDD.
JP4	When JP4 is in the 1-2 position (bottom), the DACx760 or DACx750 reference voltage is supplied through J3. When JP4 is in the 3-4 position (middle), the onboard reference (REF02) is used to provide the reference voltage. When JP4 is in the 5-6 position (top), the internal reference is used.
JP5	When JP5 is installed, the boost circuit is bypassed.
JP6	When JP6 is installed, shunt resistor R4 is used to measure the DACx760 or DACx750 current output.
JP7	When JP7 in the 1-2 position (right), a <i>clear</i> condition sets the DAC output midscale, or negative full-scale when using bipolar supplies. When JP7 is in the 2-3 position (left), a <i>clear</i> condition sets the output to 0 V.
JP8	When JP8 is installed, +VSENSE is shorted to VOUT on the EVM board. If JP8 is uninstalled, the +VSENSE to Vout connection must be provided off board, near the point of load.
JP9	When JP9 is installed, the SM-USB-DIG provides DVDD.

### 3.3 Connecting the Hardware

To connect the EVM board and the SM-USB-DIG Platform together, firmly slide the male and female ends of the 10-pin connectors together as shown in [Figure 4](#). Make sure that the two connectors are completely pushed together; loose connections may cause intermittent operation.

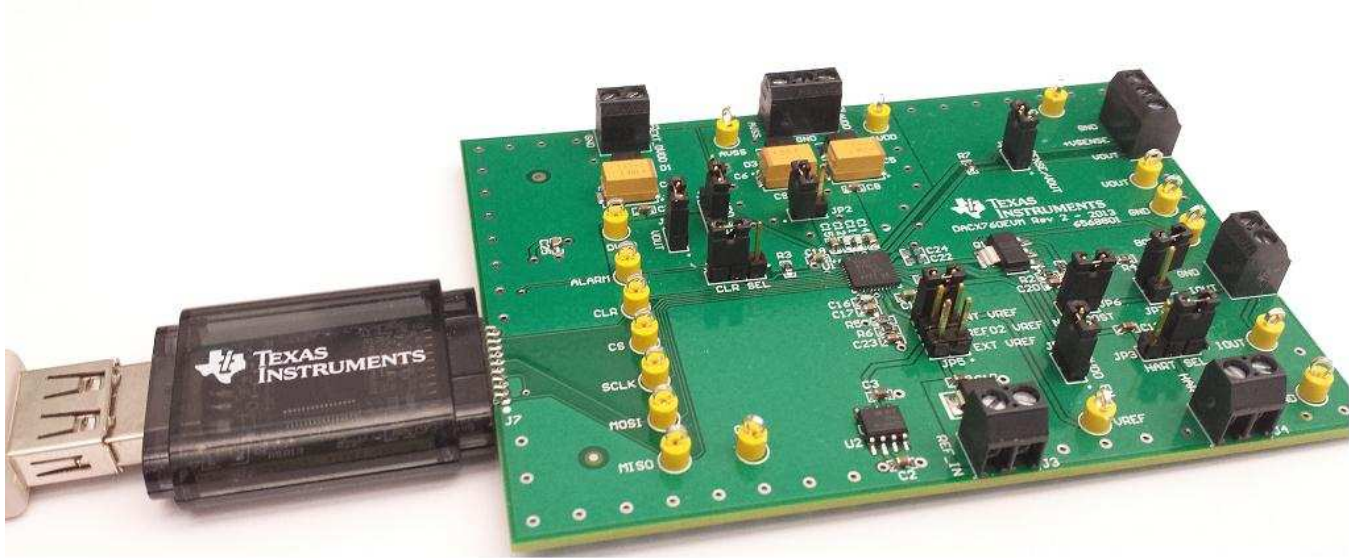


Figure 4. SM-USB-DIG Connection to the DAC8760EVM

### 3.4 Connecting the USB Cable to the SM-USB-DIG Platform

Figure 5 shows the typical response to connecting the SM-USB-DIG Platform board to a USB port for the first time. Typically, the PC responds with a *Found New Hardware, USB Device* pop-up dialog window. The pop-up window then changes to *Found New Hardware, USB Human Interface Device*. This pop-up indicates that the device is ready to be used. The SM-USB-DIG Platform uses the human interface device drivers that are included in the Windows® operating system (OS).

In some cases, the *Add Hardware Wizard* appears. If this prompt occurs, allow the system device manager to install the human interface drivers by clicking *Yes* when requested to install drivers.



Figure 5. Confirmation of SM-USB-DIG Platform Driver Installation

### 3.5 Powering the EVM

This section describes the various power configurations that can be used by the EVM.

#### 3.5.1 AVDD and AVSS Power Configurations

Terminal block J2 allows for external voltage sources to be connected to the AVDD and AVSS supply rails of the DACx760. Note that the DACx750 devices feature only AVDD supplies. The DACx760EVM only requires an AVSS supply if the DACx760 is used in  $\pm 5$  V or  $\pm 10$  V mode. If bipolar output is not required, jumper JP1 can be shunted to connect AVSS to GND, or GND may be connected at J2. AVDD and AVSS are protected to the datasheet absolute maximum potentials by transient-voltage-suppression (TVS) diodes D2, D3, and D5.

#### 3.5.2 DVDD Power Configurations

Terminal block J1 allows for an external voltage source to be connected to the DVDD pin of the DACx760 or DACx750. The EVM receives power from the SM-USB-DIG Platform when JP9 is installed. An external power source can be used when JP9 is removed and JP3 is installed. Note that if an external DVDD is used, it must be set to the same voltage as the SM-USB-DIG Platform for successful SPI communication alongside the SM-USB-DIG. The DVDD input is protected to the datasheet absolute maximum input by D1.

The DACx760 and DACx750 feature internal regulators that can be used to provide DVDD supplies. By removing JP3, the DACx760 or DACx750 provide the DVDD supply. In this configuration, JP9 must be removed and no external supply can be connected.

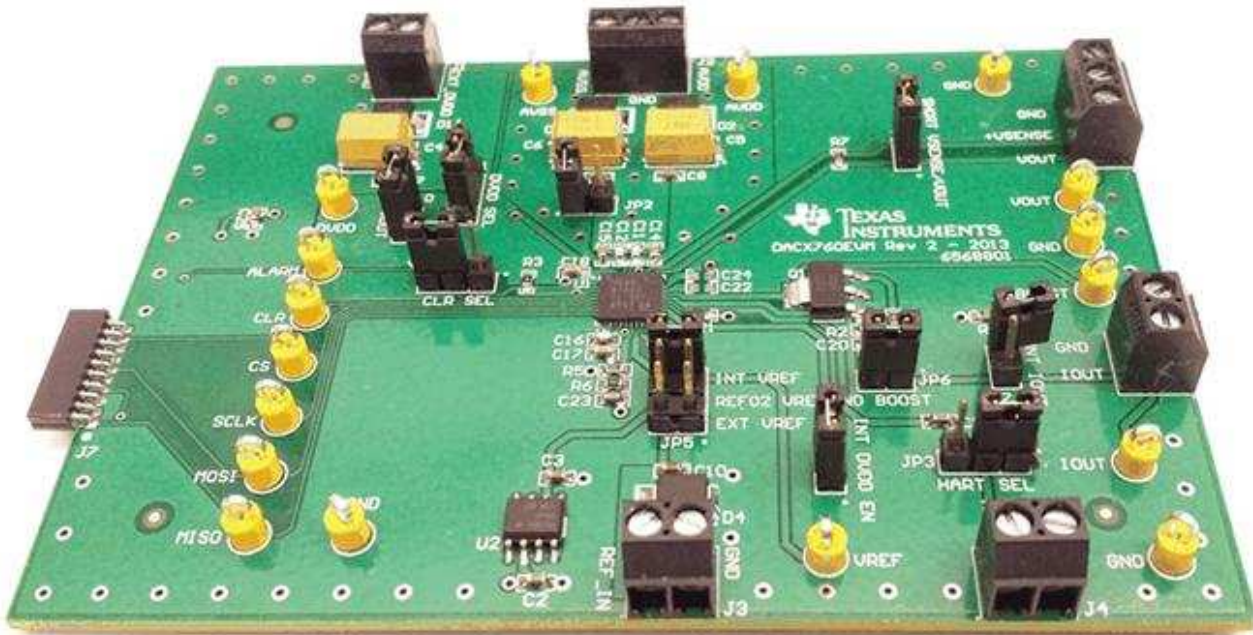


### 3.6 EVM Features

This section describes some of the hardware features present on the EVM board.

#### 3.6.1 Communication Test Points

The EVM board features test points (MISO, MOSI, SCLK, CS, ALARM, and CLEAR) for monitoring the communication between the SM-USB-DIG and the DACx760/DACx750, as shown in [Figure 6](#).



**Figure 6. Hardware Features**

The EVM design also allows external signals to be connected through the communication test points if the EVM is integrated into a custom application or prototype. Note that if the SM-USB-DIG Platform is not used, DVDD must be configured to use the EVM onboard regulators or external supplies, as described in [Section 3.5.2](#)

#### 3.6.2 Power Test Points

Test points AVSS (DACx760 only), AVDD, and DVDD are used to measure the voltage being applied directly to the EVM.

#### 3.6.3 REFOUT and REFIN

The DACx760 and DACx750 have both input and output reference voltage pins. For normal operation, a 5-V reference is required. If a specific application requires a different voltage reference, the EVM allows for a voltage reference component to be installed in the U2 SO-8 footprint (REF02 installed by default), or an external reference can be connected to J3. The external reference input is protected to the datasheet absolute maximum inputs by D4. JP4 connects the different references to the REFIN pin on the DACx760 or DACx750. Position 5-6 (top) connects the REFOUT pin. Position 3-4 (middle) connects to the output of U2. Position 1-2 (bottom) connects to J3.

### 3.6.4 Applying HART Signals

The J4 terminal block allows external HART communication signals to be modulated onto the output current. When the DAC8760EVM is in the 4-mA to 20-mA mode JP2 can be used to route the HART signal to the current output via the HART-IN pin (position 2-3 , left) or via the RSET pin (position 1-2 , right) when external RSET is used. For all other current output ranges, the external RSET path must be used to inject HART on the current output. When using the RSET path to inject HART, the values of R6 and C23 must be selected based on the current output range to avoid attenuating/amplifying the HART signal. Table 5 shows the appropriate values to use for each output range.

**Table 5. R6 and C23 Ideal Values for Each Current Range**

Current Output Range	Appropriate R6 and C23 Values
4 mA to 20 mA	30 k $\Omega$ and 10.6 nF
0 mA to 20 mA	37.5 k $\Omega$ and 8.5 nF
0 mA to 24 mA	45 k $\Omega$ and 7 nF

### 3.6.5 Populating Optional Capacitors

The EVM provides footprints for optional capacitors to be added to the EVM. Unpopulated footprints C21 (DACx760 only), C22, and C24 allow for a 0603-sized surface-mount capacitor to be used. The C21 capacitor is connected the CMP pin on the DACx760. C22 and C24 are connected to CAP1 and CAP2, respectively, for both DACx760 and DACx750 devices.

### 3.6.6 External Boost Transistor

The EVM features an external transistor (Q1) that reduces heating within the DACx760 and DACx750 by redirecting current flow externally. The NPN transistor can be bypassed by shunting jumper JP5.

### 3.6.7 IOOUT and R4

The IOOUT current on the EVM can be measured on the J5 terminal block or on the IOOUT test point. R4 is a 300- $\Omega$  resistor that acts as a load that creates a voltage drop in order to measure IOOUT as a voltage. The load can be disconnected by removing JP6, allowing for a series current meter. In addition, the 300- $\Omega$  resistor can be removed and replaced by an application-specific resistor. The footprint is intended for surface-mount resistors sized 0603. Capacitor C20 is installed by default to ensure stability of the boost circuit. It is important to note that C20 impacts the settling time and slew rate of the current output, even if the BOOST configuration is not used. For accurate evaluation of slew rate and settling time for the current output, remove C20.

### 3.6.8 VOUT and VSENSE (DACx760 Only)

The VOUT pin can be accessed on the J6 terminal block and VOUT test point. The +VSENSE pin is connected to VOUT by JP8. This configuration makes sure that VOUT is accurately measured across J6, or the VOUT test point and GND. When attaching the DACx760EVM VOUT to a specific external load, remove the JP8 shunt and connect +V<sub>SENSE</sub> to the load through J6.

### 3.6.9 CLR-SEL Jumper (DACx760 Only)

The CLR-SEL pin on the DACx760 is set by JP7 on the EVM. When the DACx760 enters a *clear* state, position 2-3 (left) sets V<sub>OUT</sub> to 0 V, and position 1-2 (right) sets VOUT to midscale (or negative full-scale if the DACx760 is in a bipolar voltage mode). Note that the CLR-SEL function can also be controlled through software. To enable this feature, JP7 must be in position 2-3 (left).

## 4 EVM Software Setup

This section discusses how to install the EVM software.

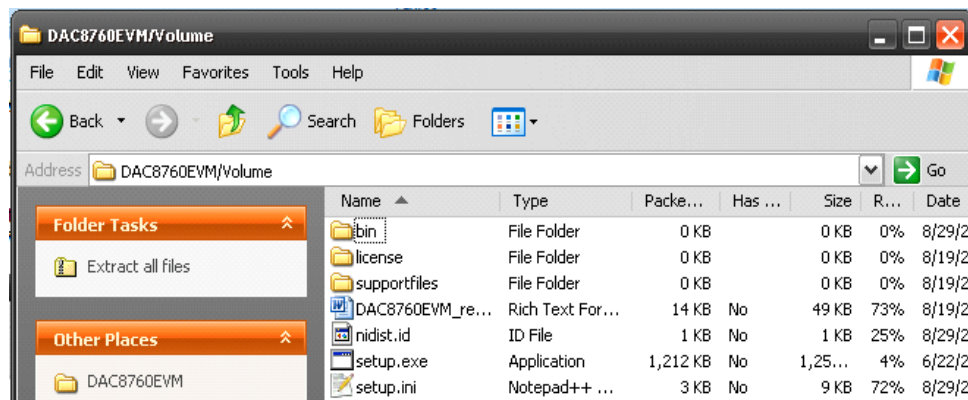
### 4.1 Operating Systems for EVM Software

The EVM software has been tested on the Windows XP® and Windows 7® operating systems with United States and European regional settings. The software should also function on other Windows operating systems.

### 4.2 EVM Software Installation

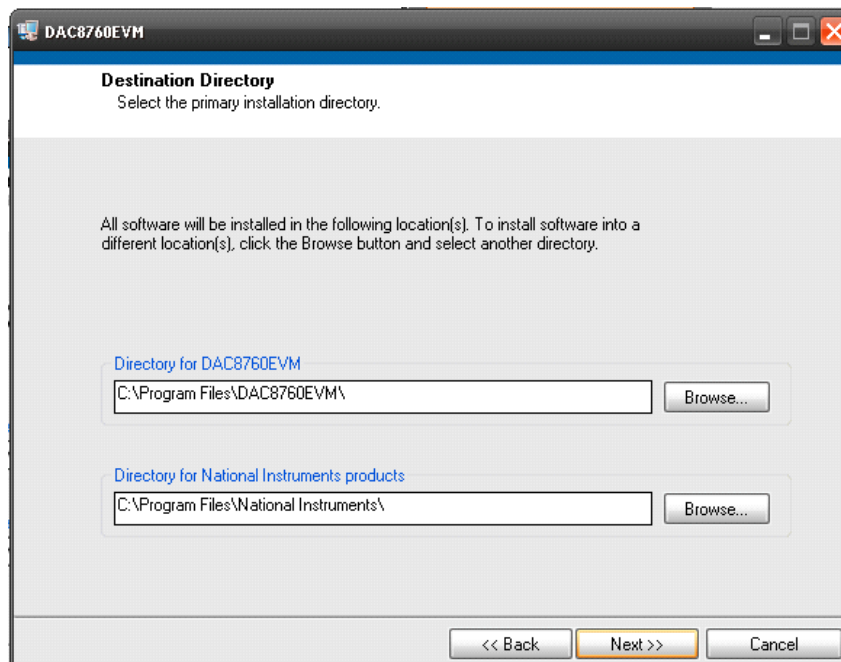
The EVM software is included on the CD that is shipped with the EVM kit. It is also available through the EVM product folder on the [TI website](#). To install the software, insert the included CD into an available CD-ROM drive. Navigate to the drive contents and open the DAC8760EVM software folder. Locate the compressed file named *DACx760EVM.zip* or *DACx750EVM.zip* and open it. Extract the EVM files into a specific folder (for example, C:\DAC8760EVM) on your hard drive.

After the files are extracted, navigate to the folder you created on your hard drive. Locate and execute the *setup.exe* file to start the installation, as shown in [Figure 7](#). The DAC8760 software installer file then opens to begin the installation process.



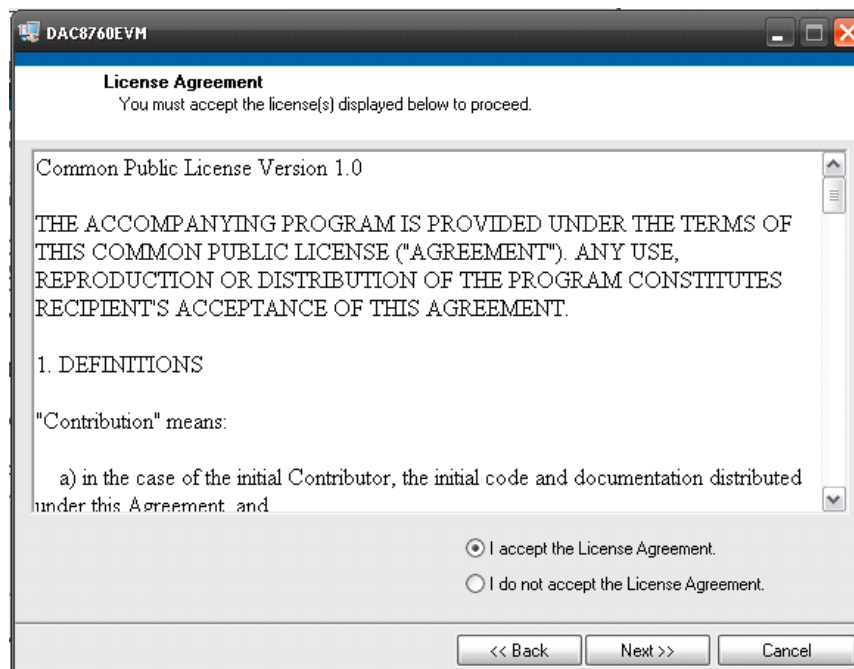
**Figure 7. DAC8760EVM Installer**

After the installation process initializes, the user is given a choice of selecting the installation directory, usually defaulting to *C:\Program Files\DAC8760EVM\* and *C:\Program Files\National Instruments\* as shown in [Figure 8](#).



**Figure 8. DAC8760EVM Install Path**

After selecting the installation directory, two license agreements are presented that must be accepted, as shown in [Figure 9](#).



**Figure 9. DAC8760EVM Software License Agreements**

After accepting the Texas Instruments and National Instruments license agreements, the progress bar opens and shows the installation of the software. Once the installation process is completed, click *Finish*.

## 5 EVM Software Overview

This section describes the use of the EVM software.

### 5.1 Starting the EVM Software

The EVM software can be operated through the Windows start menu. From the start menu, select *All Programs*, and then select *DAC8760EVM*. Figure 10 illustrates how the software should appear at launch if the EVM is functioning properly.

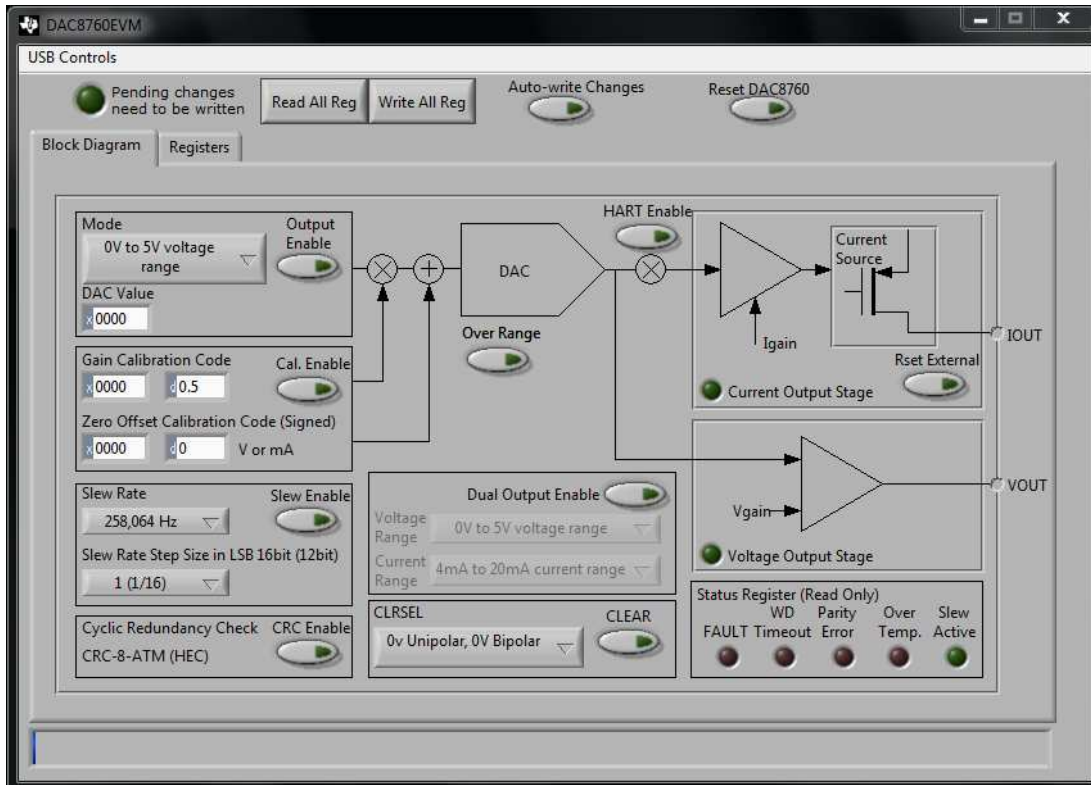


Figure 10. DAC8760EVM Software Interface

Figure 11 shows an error window that appears if the PC cannot communicate with the EVM. In the event you receive this error, first ensure that the USB cable is properly connected on both ends. This error can also occur if you connect the USB cable before the SM-USB-DIG Platform power source. Another possible source for this error is a problem with the USB human interface device driver on your PC. Make sure that the device is recognized when the USB cable is plugged in, indicated by a Windows-generated confirmation sound.

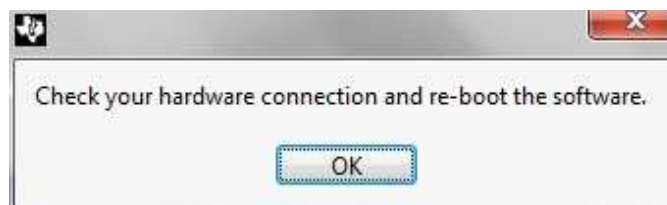


Figure 11. Communication Error with SM-USB-DIG Platform

## 5.2 EVM Software Features

### 5.2.1 Registers Tab

The EVM software features a tab devoted to reading and writing directly to the registers found on the DACx760 and DACx750, as shown in [Figure 12](#). By selecting a register in the register table, the individual bits can be set in the *Register Value* section of the tab. The function of each bit can be found in the DACx760 and DACx750 data sheets, or by clicking the *Help w/ Reg* button. Note that read-only registers cannot have their values changed in this tab.

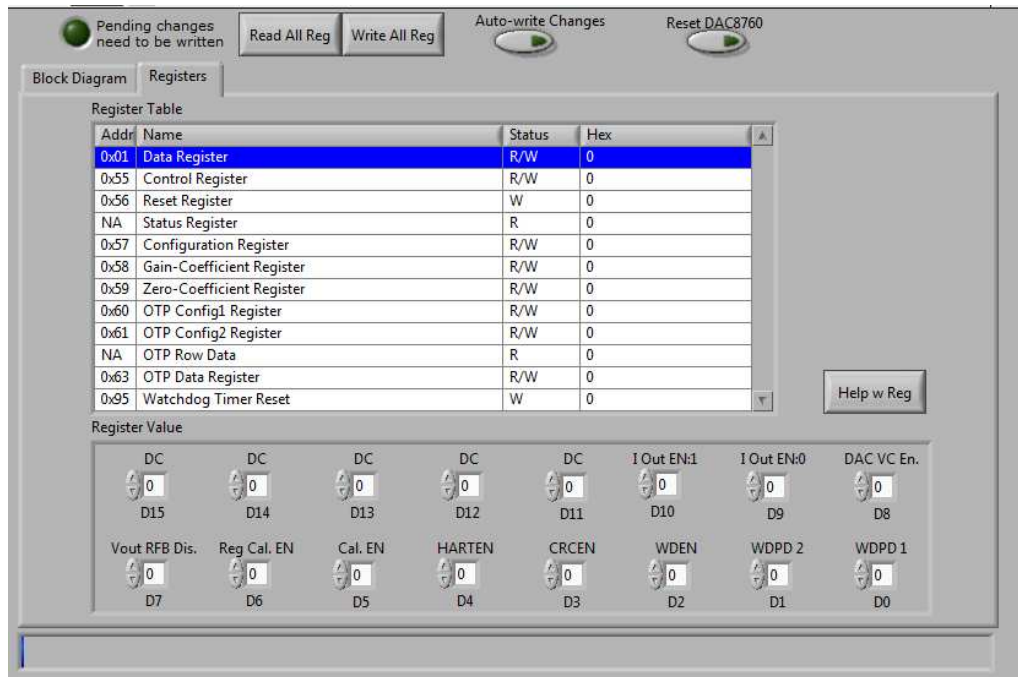


Figure 12. Registers Tab

### 5.2.2 Reading From and Writing to Registers

The EVM software only reads from and writes to the DACx760 and DACx750 registers at the user's command. These actions are accomplished with the *Read All Reg* and *Write All Reg* buttons. When any change is made to the configuration register in the *Registers* tab or the *Block Diagram* tab, the green light is on to show that changes are pending, as shown in [Figure 13](#).

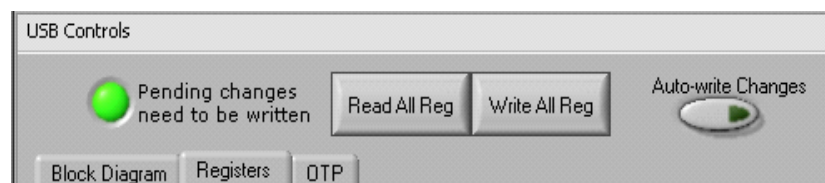


Figure 13. Read, Write, and Auto-Write Buttons

Pressing the *Write All Reg* button writes the pending changes to the DACx760 or DACx750. In addition, by enabling the *Auto-Write* button, changes are written to the configuration register automatically.

The registers in the DACx760 and DACx750 are read when the *Read All Reg* button is pressed. Perform a read after writing to the device configuration register to verify that the DACx760 or DACx750 successfully stored the data.

More information about the individual registers can be found by pressing the *Help w/ Reg* button.

### 5.2.3 Software Reset

Figure 14 shows the *Reset DAC8760* button. This button resets the DAC8760 back to the default power-on state after the change is written to the DAC.

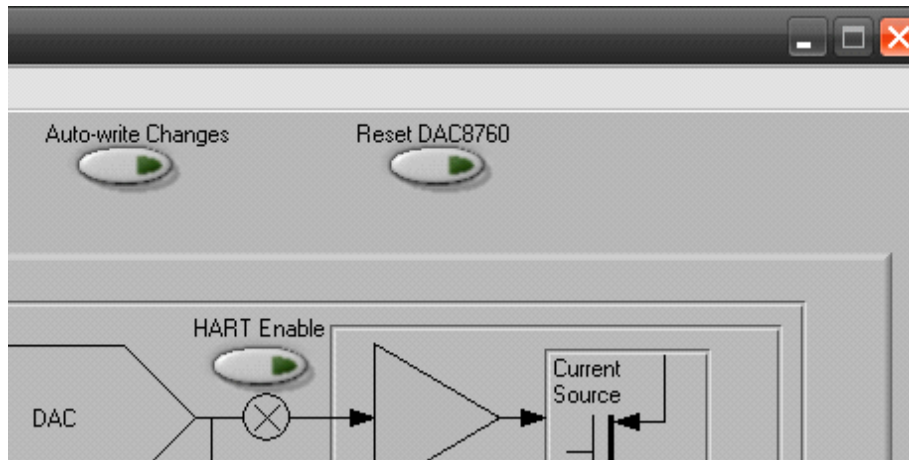


Figure 14. Resetting DAC8760

### 5.2.4 Setting the Output

The *Mode* section of the *Block Diagram* tab allows for the configuration of the output range, output enable, and output value to be set, as shown in Figure 15.

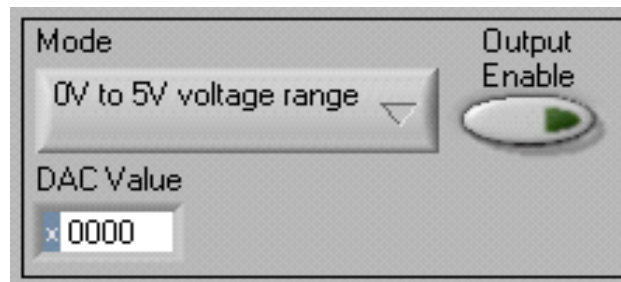


Figure 15. Mode Selection

The *DAC Value* field must be rewritten to the DACx760 or DACx750 when the range is changed because the DAC value is reset. The *Output Enable* toggle button sets the OUTEN bit in the control register to high, which enables either the  $I_{OUT}$  or  $V_{OUT}$  functions.

### 5.2.5 Dual Output Enable (DACx760 devices only)

The DACx760 devices that feature both current and voltage outputs also feature a dual output enable option. This feature is not included on the DACx750 current output only devices. To enable dual outputs toggle the *Dual Output Enable* button shown in Figure 16 and select a voltage and current output range. The *Output Enable* and *DAC Value* shown in Figure 15 are used in dual output mode to enable the pair of outputs and to set the output code.

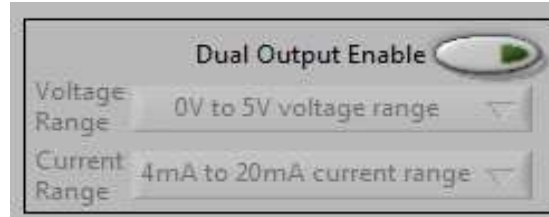


Figure 16. Dual Output Enable

### 5.2.6 Enabling Voltage Overrange (DACx760 devices only)

Figure 17 shows the *Over Range* toggle button. This button enables the DACx760 overrange function, which increases the voltage output range by 10% (not included in DACx750 devices).

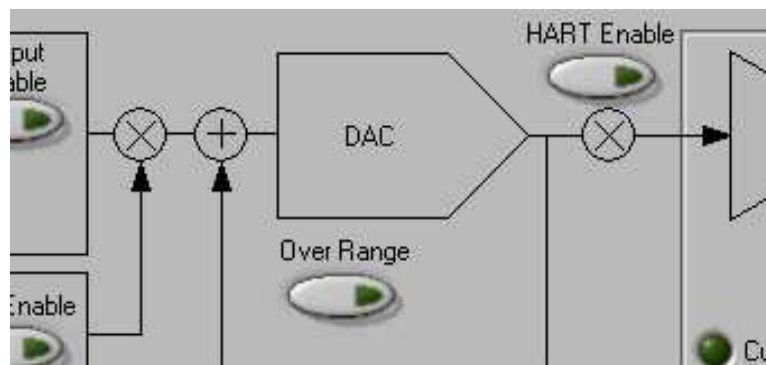


Figure 17. Enabling Over-Range Operation

### 5.2.7 Accessing Calibration Registers

The DACx760 and DACx750 feature programmable gain and offset functions. Set the gain and offset with the *Gain Calibration Code* and *Zero Offset Calibration Code* fields. As shown in Figure 18, the fields on the left allow a 16-bit hex value to be entered directly, and the fields on the right allow decimal values to be used. The *Cal. Enable* toggle button applies the gain and offset to the data register. After reading all registers, the *DAC Value* field shows the changes.

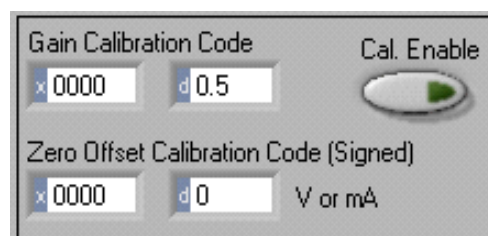


Figure 18. Calibration Registers



### 5.2.8 Slew Rate Configuration

Use the *Slew Rate* section of the *Block Diagram* tab, as shown in Figure 19, to set the various slew-rate controls. The *Slew Rate* drop-down menu sets the slewing frequency. The *Slew Rate Step Size* drop-down menu sets the step size, which is listed in LSB increments with the 12-bit step sizes in parentheses. The *Slew Enable* toggle button enables the programmed slew rates and step size on the DAC.

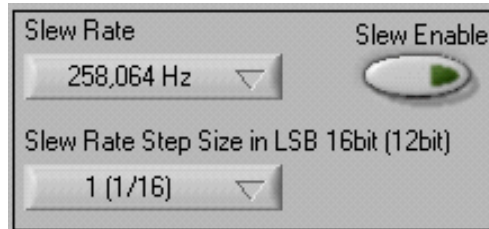


Figure 19. Setting Slew Rates

### 5.2.9 Cyclic Redundancy Check

The *CRC Enable* toggle button enables the DACx760 or DACx750 cyclic redundancy check function. When the button is pressed, the EVM software informs the user that the configuration register will be written to immediately, as shown in Figure 20. It is written immediately to make sure that any other pending changes are written to the DACx760 or DACx750 with the correct CRC value.

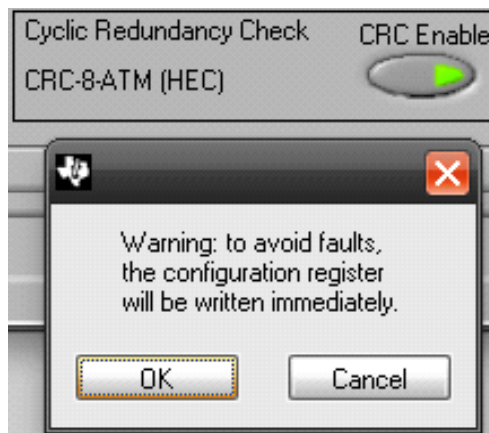


Figure 20. CRC Enable and Dialog

### 5.2.10 Clear Functionality

The *CLRSEL* drop-down menu, as shown in Figure 21, sets the value of VOUT after a power-on and reset occur. The *CLEAR* button sets the CLR pin high, resulting in a *clear* state. Note that the DACx760 and DACx750 set the voltage out to midscale (negative full-scale when in bipolar mode for DACx760 devices) if either the CLR-SEL pin is high or the register is set to midrange.

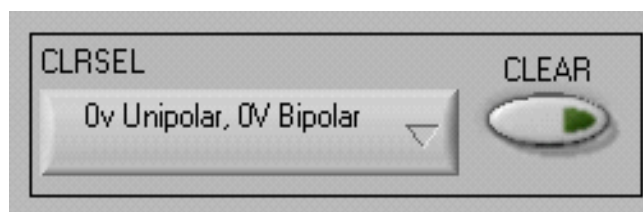


Figure 21. CLRSEL Drop-Down Menu and Clear Button

## 6 Schematics, PCB Assembly Drawings, and Bills of Materials

This section contains the schematics, PCB layouts, and bills of materials for the DACx760EVM and DACx750EVM. Documentation information for the SM-USB-DIG Platform can be found in [SBOU098](#), *SM-USB-DIG Platform User's Guide*, available at the TI web site at <http://www.ti.com>.

### 6.1 DACx760EVM Board Schematic

Figure 22 shows the schematic for the DACx760EVM board.

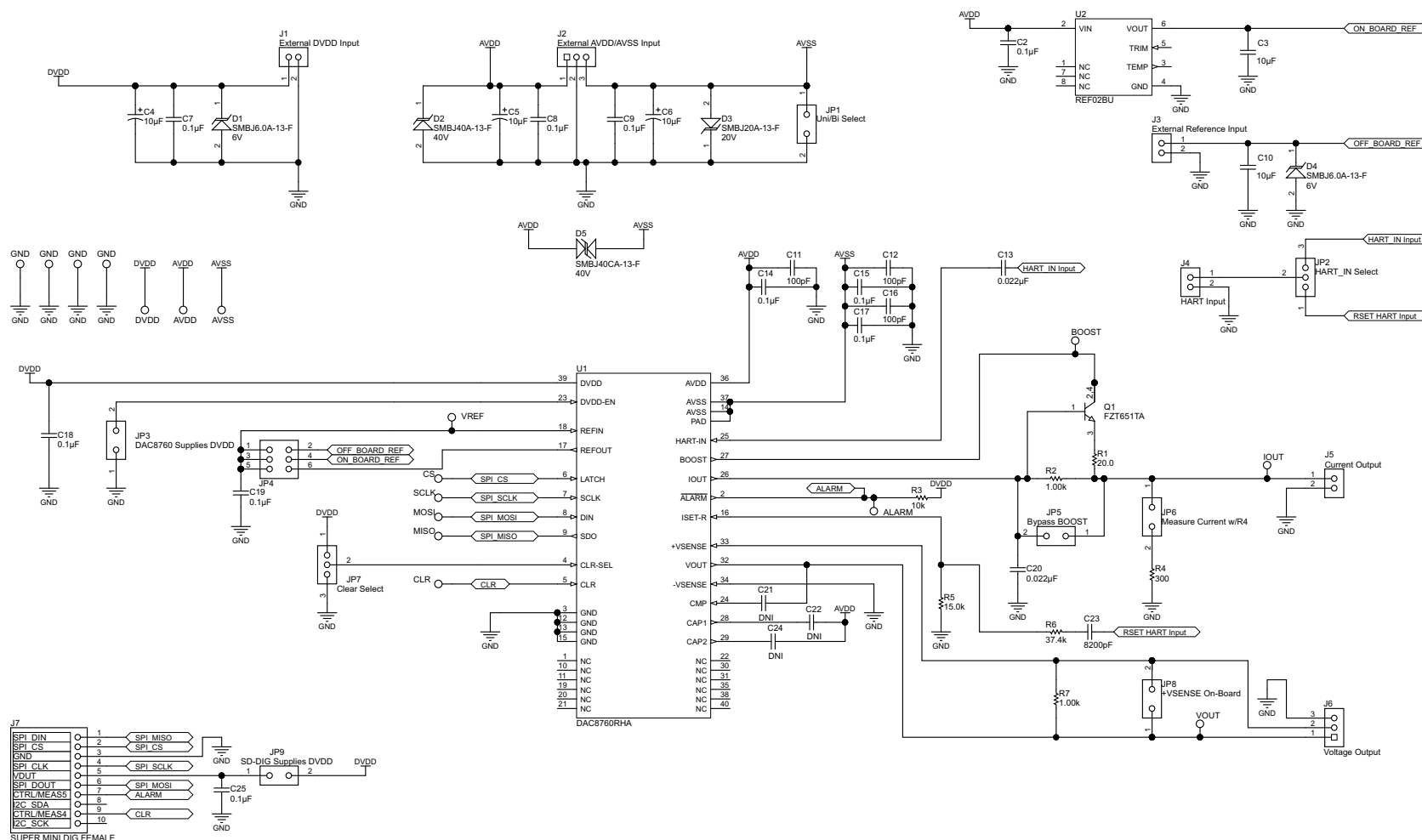


Figure 22. DACx760EVM Schematic

## 6.2 DACx760EVM Assembly Drawing

Figure 23 shows the assembly drawing of the components for the DACx760EVM board.

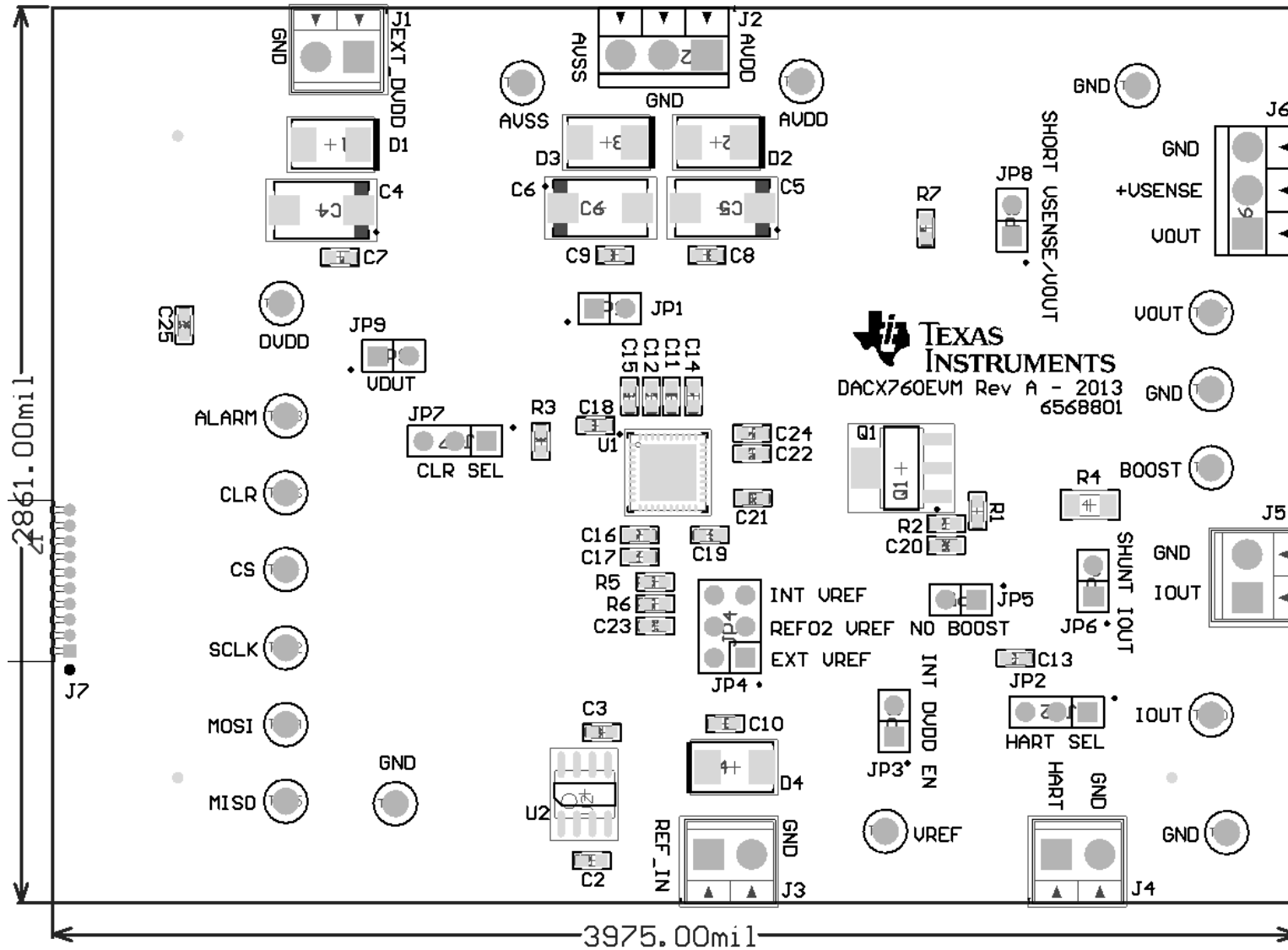


Figure 23. DACx760EVM Assembly Drawing

### 6.3 DACx760EVM Bill of Materials

Table 6 lists the bill of materials for the DACx760EVM.

**Table 6. DACx760EVM Bill of Materials**

Count	Ref.	Value	Description	Manufacturer	Model
10	C2, C7, C8, C9, C14, C15, C17, C18, C19, C25	0.1uF	CAP, CERM, 0.1uF, 50V, +/-10%, X7R, 0603	MuRata Electronics	GRM188R71H104KA93D
2	C3, C10	10uF	CAP, CERM, 10uF, 6.3V, +/-20%, X5R, 0603	TDK Corporation	C1608X5R0J106M
3	C4, C5, C6	10uF	CAP, TA, 10uF, 50V, +/-10%, 0.4 ohm, SMD	AVX Corporation	TPSE106K050R0400
3	C11, C12, C16	100pF	CAP, CERM, 100pF, 50V, +/-5%, C0G/NP0, 0603	MuRata Electronics	GRM1885C1H101JA01D
2	C13, C20	0.022uF	CAP, CERM, 0.022uF, 50V, +/-10%, X7R, 0603	TDK Corporation	C1608X7R1H223K
0	C21, C22, C24	N/A	Not Installed	N/A	N/A
1	C23	8200pF	CAP, CERM, 8200pF, 50V, +/-10%, X7R, 0603	MuRata	GRM188R71H822KA01D
2	D1, D4	N/A	Diode, TVS, Uni, 6V, 600W, SMB	Diodes Inc	SMBJ6.0A-13-F
1	D2	N/A	Diode, TVS, Uni, 40V, 600W, SMB	Diodes Inc	SMBJ40A-13-F
1	D3	N/A	Diode, TVS, Uni, 20V, 200W, SMB	Diodes Inc	SMBJ20A-13-F
1	D5	N/A	Diode, TVS, Bi, 40V, 600W, SMB	Diodes Inc	SMBJ40CA-13-F
4	J1, J3, J4, J5	N/A	Terminal Block, 6A, 3.5mm Pitch, 2-Pos, TH	On-Shore Technology	ED555/2DS
2	J2, J6	N/A	Terminal Block, 6A, 3.5mm Pitch, 3-Pos, TH	On-Shore Technology	ED555/3DS
1	J7	N/A	Receptacle, 50mil 10x1, R/A, TH	Mill-Max Corporation	851-43-010-20-001000
3	JP1, JP3, JP8	N/A	Header, TH, 100mil, 3x1, Gold plated, 230 mil above insulator	Samtec Inc	TSW-103-07-G-S
5	JP2, JP4, JP6, JP7, JP9	N/A	Header, TH, 100mil, 2x1, Gold plated, 230 mil above insulator	Samtec Inc	TSW-102-07-G-S
1	JP5	N/A	Header, TH, 100mil, 3x2, Gold plated, 230 mil above insulator	Samtec Inc	TSW-103-07-G-D
1	Q1	N/A	Transistor, NPN, 60V, 3A, SOT-223	Zetex	FZT651TA
1	R1	20.0Ω	RES, 20.0 ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW060320R0FKEA
2	R2, R7	1.00kΩ	RES, 1.00k ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW06031K00FKEA
1	R3	10.0kΩ	RES, 10k ohm, 5%, 0.1W, 0603	Vishay-Dale	CRCW060310K0JNEA
1	R4	300Ω	RES, 300 ohm, 0.1%, 0.25W, 1206	Susumu Co Ltd	RG3216P-3000-B-T1
1	R5	15.0kΩ	RES, 15.0k ohm, 0.1%, 0.1W, 0603	Susumu Co Ltd	RG1609P-153-B-T5
1	R6	37.4kΩ	RES, 37.4k ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW060337K4FKEA
17	TP1-TP17	N/A	Test Point, Compact, Yellow, TH	Keystone Electronics	5009
1	U1	N/A	Single-Channel, 16-Bit Programmable Current Output and Voltage Output DIGITAL-TO-ANALOG CONVERTER for 4mA to 20mA Current Loop Applications, RHA0040C	Texas Instruments	DAC8760RHA
1	U2	N/A	5V PRECISION VOLTAGE REFERENCE, D0008A	Texas Instruments	REF02BU
10	SH-JP1-SH-JP9	N/A	Shunt, 100mil, Gold plated, Black	3M	969102-0000-DA
4	H1, H2, H3, H4	N/A	Bump, Hemisphere, 0.44 X 0.20, Clear	3M	SJ-5303 (CLEAR)

### 6.4 DACx750EVM Board Schematic

Figure 24 shows the schematic for the DACx750EVM board

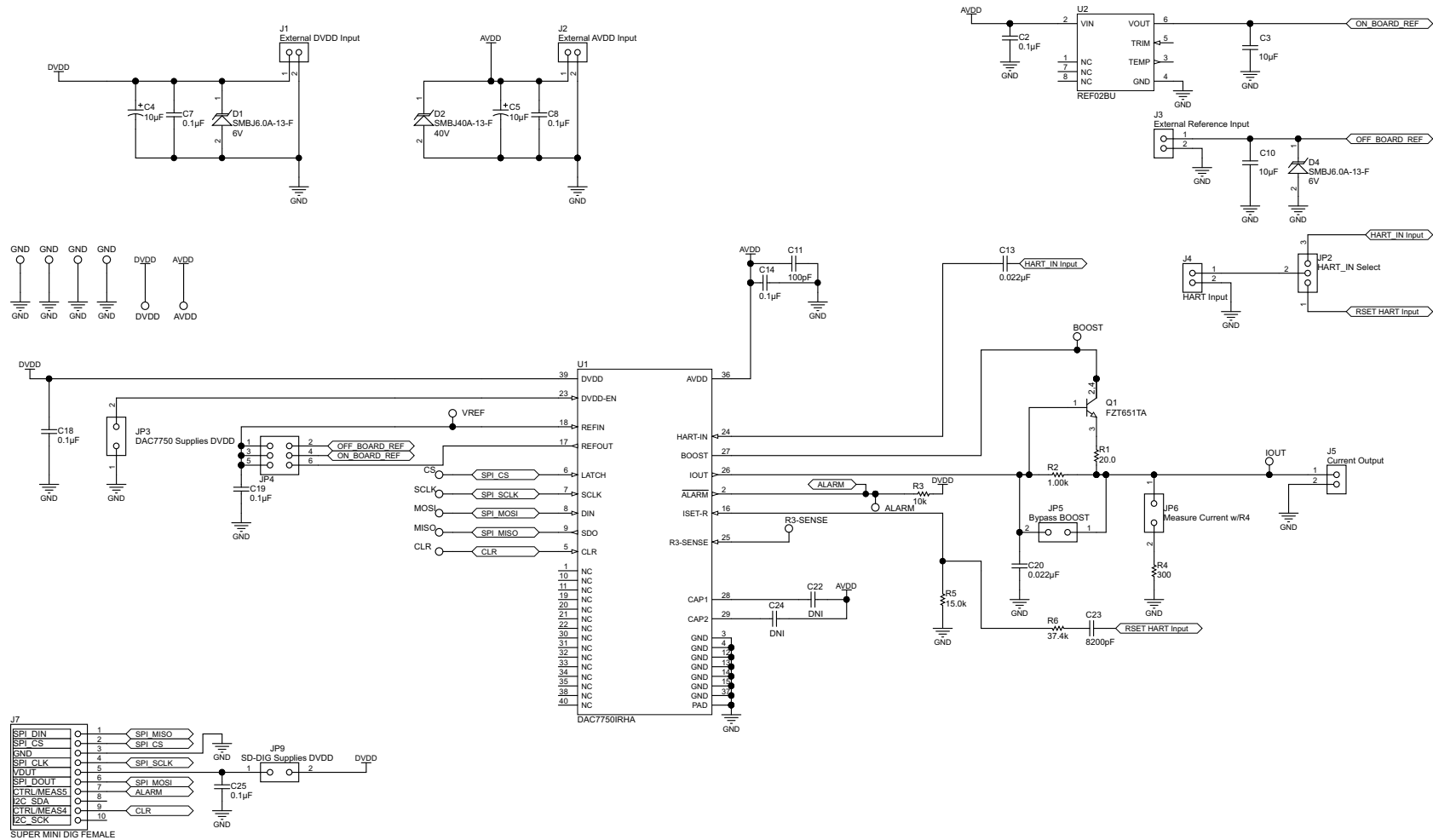


Figure 24. DACx750EVM Schematic

### 6.5 DACx750EVM Assembly Drawing

Figure 25 shows the assembly drawing for the DACx750EVM board

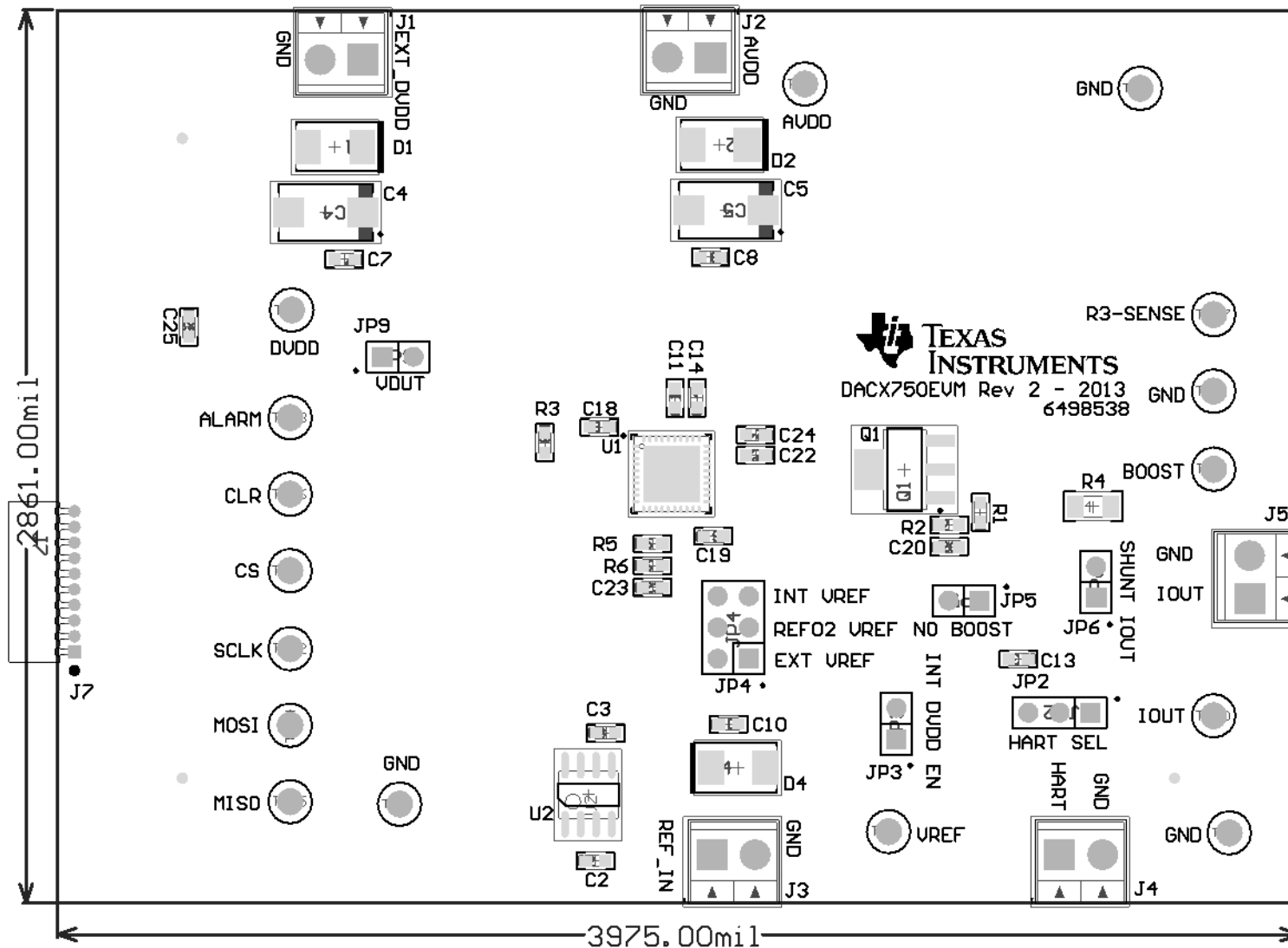


Figure 25. DACx750EVM Assembly Drawing

## 6.6 DACx750EVM Bill of Materials

Table 7 lists the bill of materials for the DACx750EVM.

**Table 7. DACx750EVM Bill of Materials**

Count	Ref.	Value	Description	Manufacturer	Model
7	C2, C7, C8, C14, C18, C19, C25	0.1uF	CAP, CERM, 0.1uF, 50V, +/-10%, X7R, 0603	MuRata Electronics	GRM188R71H104KA93D
2	C3, C10	10uF	CAP, CERM, 10uF, 6.3V, +/-20%, X5R, 0603	TDK Corporation	C1608X5R0J106M
2	C4, C5	10uF	CAP, TA, 10uF, 50V, +/-10%, 0.4 ohm, SMD	AVX Corporation	TPSE106K050R0400
1	C11	100pF	CAP, CERM, 100pF, 50V, +/-5%, C0G/NP0, 0603	MuRata Electronics	GRM1885C1H101JA01D
2	C13, C20	0.022uF	CAP, CERM, 0.022uF, 50V, +/-10%, X7R, 0603	TDK Corporation	C1608X7R1H223K
0	C22, C24	N/A	Not Installed	N/A	N/A
1	C23	8200pF	CAP, CERM, 8200pF, 50V, +/-10%, X7R, 0603	MuRata	GRM188R71H822KA01D
2	D1, D4	N/A	Diode, TVS, Uni, 6V, 600W, SMB	Diodes Inc	SMBJ6.0A-13-F
1	D2	N/A	Diode, TVS, Uni, 40V, 600W, SMB	Diodes Inc	SMBJ40A-13-F
4	J1, J3, J4, J5	N/A	Terminal Block, 6A, 3.5mm Pitch, 2-Pos, TH	On-Shore Technology	ED555/2DS
1	J7	N/A	Receptacle, 50mil 10x1, R/A, TH	Mill-Max Corporation	851-43-010-20-001000
2	JP1, JP3	N/A	Header, TH, 100mil, 3x1, Gold plated, 230 mil above insulator	Samtec Inc	TSW-103-07-G-S
3	JP4, JP6, JP7,	N/A	Header, TH, 100mil, 2x1, Gold plated, 230 mil above insulator	Samtec Inc	TSW-102-07-G-S
1	JP5	N/A	Header, TH, 100mil, 3x2, Gold plated, 230 mil above insulator	Samtec Inc	TSW-103-07-G-D
1	Q1	N/A	Transistor, NPN, 60V, 3A, SOT-223	Zetex	FZT651TA
1	R1	20.0Ω	RES, 20.0 ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW060320R0FKEA
2	R2	1.00kΩ	RES, 1.00k ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW06031K00FKEA
1	R3	10.0kΩ	RES, 10k ohm, 5%, 0.1W, 0603	Vishay-Dale	CRCW060310K0JNEA
1	R4	300Ω	RES, 300 ohm, 0.1%, 0.25W, 1206	Susumu Co Ltd	RG3216P-3000-B-T1
1	R5	15.0kΩ	RES, 15.0k ohm, 0.1%, 0.1W, 0603	Susumu Co Ltd	RG1609P-153-B-T5
1	R6	37.4kΩ	RES, 37.4k ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW060337K4FKEA
16	TP1-TP16	N/A	Test Point, Compact, Yellow, TH	Keystone Electronics	5009
1	U1	N/A	Single-Channel, 16-Bit Programmable Current Output DIGITAL-TO-ANALOG CONVERTER for 4-mA to 20-mA Current Loop Applications, RHA0040C	Texas Instruments	DAC8750RHA
1	U2	N/A	5V PRECISION VOLTAGE REFERENCE, D0008A	Texas Instruments	REF02BU
6	SH-JP1, SH-JP3, SH-JP4, SH-JP5, SH-JP6, SH-JP7	N/A	Shunt, 100mil, Gold plated, Black	3M	969102-0000-DA
4	H1, H2, H3, H4	N/A	Bumpon, Hemisphere, 0.44 X 0.20, Clear	3M	SJ-5303 (CLEAR)

## Revision History

<b>Changes from Original (March 2013) to A Revision</b>	<b>Page</b>
• Added DAC7750 and DAV8750 devices and updated document to show these additional devices .....	1
• Changed <a href="#">Figure 2</a> .....	4
• Changed <a href="#">Section 3</a> ; updated jumpers settings, resistors, and capacitors throughout this section. ....	6
• Added <a href="#">Section 3.2, Jumper Summary</a> .....	6
• Changed <a href="#">Figure 4</a> .....	7
• Changed <a href="#">Figure 6</a> .....	9
• Added <a href="#">Table 5</a> .....	10
• Added <a href="#">Section 5.2.5, Dual Output Enable</a> .....	16

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.



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As noted in the EVM User's Guide and/or EVM itself, this EVM and/or accompanying hardware may or may not be subject to the Federal Communications Commission (FCC) and Industry Canada (IC) rules.

For EVMs **not** subject to the above rules, this evaluation board/kit/module is intended for use for ENGINEERING DEVELOPMENT, DEMONSTRATION OR EVALUATION PURPOSES ONLY and is not considered by TI to be a finished end product fit for general consumer use. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to part 15 of FCC or ICES-003 rules, which are designed to provide reasonable protection against radio frequency interference. Operation of the equipment may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

### **General Statement for EVMs including a radio**

*User Power/Frequency Use Obligations:* This radio is intended for development/professional use only in legally allocated frequency and power limits. Any use of radio frequencies and/or power availability of this EVM and its development application(s) must comply with local laws governing radio spectrum allocation and power limits for this evaluation module. It is the user's sole responsibility to only operate this radio in legally acceptable frequency space and within legally mandated power limitations. Any exceptions to this are strictly prohibited and unauthorized by Texas Instruments unless user has obtained appropriate experimental/development licenses from local regulatory authorities, which is responsibility of user including its acceptable authorization.

### **For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant**

#### **Caution**

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

#### **FCC Interference Statement for Class A EVM devices**

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

### **FCC Interference Statement for Class B EVM devices**

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

### **For EVMs annotated as IC – INDUSTRY CANADA Compliant**

This Class A or B digital apparatus complies with Canadian ICES-003.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

### **Concerning EVMs including radio transmitters**

This device complies with Industry Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

### **Concerning EVMs including detachable antennas**

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication.

This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Cet appareil numérique de la classe A ou B est conforme à la norme NMB-003 du Canada.

Les changements ou les modifications pas expressément approuvés par la partie responsable de la conformité ont pu vider l'autorité de l'utilisateur pour actionner l'équipement.

### **Concernant les EVMs avec appareils radio**

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

### **Concernant les EVMs avec antennes détachables**

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante.

Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

## **【Important Notice for Users of EVMs for RF Products in Japan】**

**This development kit is NOT certified as Confirming to Technical Regulations of Radio Law of Japan**

If you use this product in Japan, you are required by Radio Law of Japan to follow the instructions below with respect to this product:

1. Use this product in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use this product only after you obtained the license of Test Radio Station as provided in Radio Law of Japan with respect to this product, or
3. Use of this product only after you obtained the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to this product. Also, please do not transfer this product, unless you give the same notice above to the transferee. Please note that if you could not follow the instructions above, you will be subject to penalties of Radio Law of Japan.

**Texas Instruments Japan Limited**  
**(address) 24-1, Nishi-Shinjuku 6 chome, Shinjuku-ku, Tokyo, Japan**

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西新宿三井ビル

<http://www.tij.co.jp>

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**For Feasibility Evaluation Only, in Laboratory/Development Environments.** Unless otherwise indicated, this EVM is not a finished electrical equipment and not intended for consumer use. It is intended solely for use for preliminary feasibility evaluation in laboratory/development environments by technically qualified electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems and subsystems. It should not be used as all or part of a finished end product.

Your Sole Responsibility and Risk. You acknowledge, represent and agree that:

1. You have unique knowledge concerning Federal, State and local regulatory requirements (including but not limited to Food and Drug Administration regulations, if applicable) which relate to your products and which relate to your use (and/or that of your employees, affiliates, contractors or designees) of the EVM for evaluation, testing and other purposes.
2. You have full and exclusive responsibility to assure the safety and compliance of your products with all such laws and other applicable regulatory requirements, and also to assure the safety of any activities to be conducted by you and/or your employees, affiliates, contractors or designees, using the EVM. Further, you are responsible to assure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard.
3. Since the EVM is not a completed product, it may not meet all applicable regulatory and safety compliance standards (such as UL, CSA, VDE, CE, RoHS and WEEE) which may normally be associated with similar items. You assume full responsibility to determine and/or assure compliance with any such standards and related certifications as may be applicable. You will employ reasonable safeguards to ensure that your use of the EVM will not result in any property damage, injury or death, even if the EVM should fail to perform as described or expected.
4. You will take care of proper disposal and recycling of the EVM's electronic components and packing materials.

**Certain Instructions.** It is important to operate this EVM within TI's recommended specifications and environmental considerations per the user guidelines. Exceeding the specified EVM ratings (including but not limited to input and output voltage, current, power, and environmental ranges) may cause property damage, personal injury or death. If there are questions concerning these ratings please contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, some circuit components may have case temperatures greater than 60°C as long as the input and output are maintained at a normal ambient operating temperature. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors which can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during normal operation, please be aware that these devices may be very warm to the touch. As with all electronic evaluation tools, only qualified personnel knowledgeable in electronic measurement and diagnostics normally found in development environments should use these EVMs.

**Agreement to Defend, Indemnify and Hold Harmless.** You agree to defend, indemnify and hold TI, its licensors and their representatives harmless from and against any and all claims, damages, losses, expenses, costs and liabilities (collectively, "Claims") arising out of or in connection with any use of the EVM that is not in accordance with the terms of the agreement. This obligation shall apply whether Claims arise under law of tort or contract or any other legal theory, and even if the EVM fails to perform as described or expected.

**Safety-Critical or Life-Critical Applications.** If you intend to evaluate the components for possible use in safety critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, such as devices which are classified as FDA Class III or similar classification, then you must specifically notify TI of such intent and enter into a separate Assurance and Indemnity Agreement.

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