

74LVC1G79-Q100

Single D-type flip-flop; positive-edge trigger

Rev. 3 — 1 February 2022

Product data sheet

1. General description

The 74LVC1G79-Q100 is a single positive-edge triggered D-type flip-flop. Data at the D-input that meets the set-up and hold time requirements on the LOW-to-HIGH clock transition will be stored in the flip-flop and appear at the Q output. Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in mixed 3.3 V and 5 V environments.

Schmitt-trigger action at all inputs makes the circuit tolerant of slower input rise and fall times.

This device is fully specified for partial power down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
 - Specified from -40 °C to +85 °C and -40 °C to +125 °C
- Wide supply voltage range from 1.65 V to 5.5 V
- Overvoltage tolerant inputs to 5.5 V
- High noise immunity
- CMOS low power dissipation
- ±24 mA output drive (V_{CC} = 3.0 V)
- Direct interface with TTL levels
- Latch-up performance exceeds 250 mA
- I_{OFF} circuitry provides partial Power-down mode operation
- Complies with JEDEC standard:
 - JESD8-7 (1.65 V to 1.95 V)
 - JESD8-5 (2.3 V to 2.7 V)
 - JESD8C (2.7 V to 3.6 V)
 - JESD36 (4.5 V to 5.5 V)
- ESD protection:
 - MIL-STD-883, method 3015 exceeds 2000 V
 - HBM JESD22-A114F exceeds 2000 V
 - MM JESD22-A115-A exceeds 200 V

3. Ordering information

Table 1. Ordering information

| Type number | Package | | | Version |
|------------------|-------------------|--------|--|----------|
| | Temperature range | Name | Description | |
| 74LVC1G79GW-Q100 | -40 °C to +125 °C | TSSOP5 | plastic thin shrink small outline package; 5 leads; body width 1.25 mm | SOT353-1 |
| 74LVC1G79GV-Q100 | -40 °C to +125 °C | SC-74A | plastic surface-mounted package; 5 leads | SOT753 |

4. Marking

Table 2. Marking codes

| Type number | Marking ^[1] |
|------------------|------------------------|
| 74LVC1G79GW-Q100 | VP |
| 74LVC1G79GV-Q100 | V79 |

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5. Functional diagram

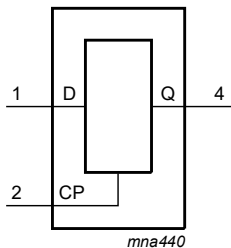


Fig. 1. Logic symbol

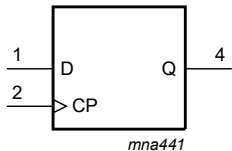


Fig. 2. IEC logic symbol

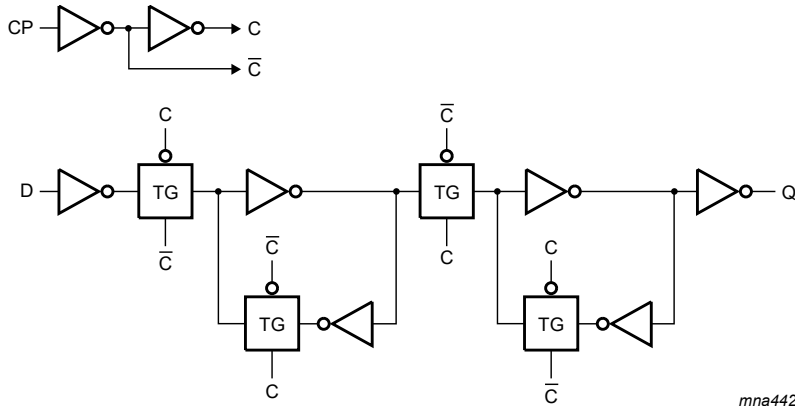
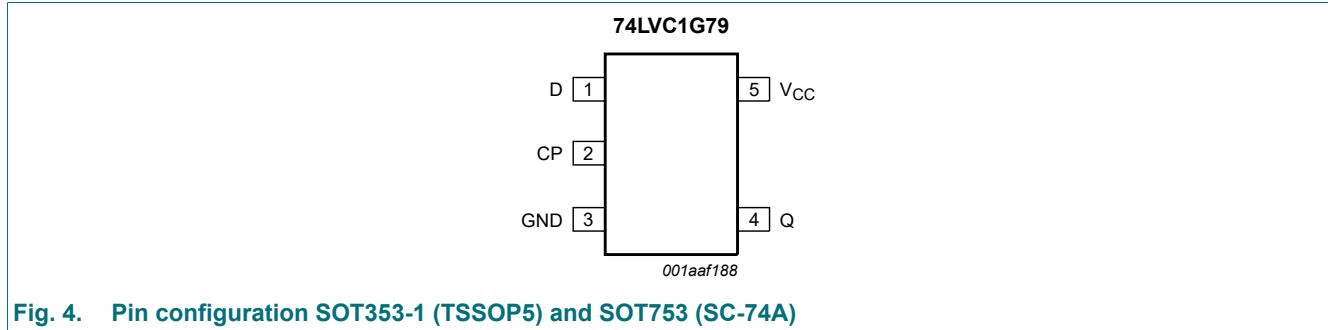


Fig. 3. Logic diagram

6. Pinning information

6.1. Pinning



6.2. Pin description

Table 3. Pin description

| Symbol | Pin | Description |
|-----------------|-----|-------------------|
| D | 1 | data input |
| CP | 2 | clock pulse input |
| GND | 3 | ground (0 V) |
| Q | 4 | data output |
| V _{CC} | 5 | supply voltage |

7. Functional description

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level; ↑ = LOW-to-HIGH CP transition; X = don't care; q = lower case letter indicates the state of referenced input, one set-up time prior to the LOW-to-HIGH CP transition.

| Input | | Output |
|-------|---|--------|
| CP | D | Q |
| ↑ | L | L |
| ↑ | H | H |
| L | X | q |

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------|-------------------------|---------------------------------|------|----------------|------|
| V_{CC} | supply voltage | | -0.5 | +6.5 | V |
| I_{IK} | input clamping current | $V_I < 0$ V | -50 | - | mA |
| V_I | input voltage | | -0.5 | +6.5 | V |
| I_{OK} | output clamping current | $V_O > V_{CC}$ or $V_O < 0$ V | - | ± 50 | mA |
| V_O | output voltage | Active mode | -0.5 | $V_{CC} + 0.5$ | V |
| | | Power-down mode; $V_{CC} = 0$ V | -0.5 | +6.5 | V |
| I_O | output current | $V_O = 0$ V to V_{CC} | - | ± 50 | mA |
| I_{CC} | supply current | | - | 100 | mA |
| I_{GND} | ground current | | -100 | - | mA |
| P_{tot} | total power dissipation | $T_{amb} = -40$ °C to $+125$ °C | - | 250 | mW |
| T_{stg} | storage temperature | | -65 | +150 | °C |

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SOT353-1 (TSSOP5) package: P_{tot} derates linearly with 3.3 mW/K above 74 °C.

For SOT753 (SC-74A) package: P_{tot} derates linearly with 3.8 mW/K above 85 °C.

9. Recommended operating conditions

Table 6. Recommended operating conditions

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------------|-------------------------------------|---------------------------------|------|-----|----------|------|
| V_{CC} | supply voltage | | 1.65 | - | 5.5 | V |
| V_I | input voltage | | 0 | - | 5.5 | V |
| V_O | output voltage | Active mode | 0 | - | V_{CC} | V |
| | | Power-down mode; $V_{CC} = 0$ V | 0 | - | 5.5 | V |
| T_{amb} | ambient temperature | | -40 | - | +125 | °C |
| $\Delta t/\Delta V$ | input transition rise and fall rate | $V_{CC} = 1.65$ V to 2.7 V | - | - | 20 | ns/V |
| | | $V_{CC} = 2.7$ V to 5.5 V | - | - | 10 | ns/V |

10. Static characteristics

Table 7. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Typ[1] | Max | Unit |
|---|---------------------------|--|------------------------|--------|------------------------|------|
| T_{amb} = -40 °C to +85 °C | | | | | | |
| V _{IH} | HIGH-level input voltage | V _{CC} = 1.65 V to 1.95 V | 0.65 × V _{CC} | - | - | V |
| | | V _{CC} = 2.3 V to 2.7 V | 1.7 | - | - | V |
| | | V _{CC} = 2.7 V to 3.6 V | 2.0 | - | - | V |
| | | V _{CC} = 4.5 V to 5.5 V | 0.7 × V _{CC} | - | - | V |
| V _{IL} | LOW-level input voltage | V _{CC} = 1.65 V to 1.95 V | - | - | 0.35 × V _{CC} | V |
| | | V _{CC} = 2.3 V to 2.7 V | - | - | 0.7 | V |
| | | V _{CC} = 2.7 V to 3.6 V | - | - | 0.8 | V |
| | | V _{CC} = 4.5 V to 5.5 V | - | - | 0.3 × V _{CC} | V |
| V _{OH} | HIGH-level output voltage | V _I = V _{IH} or V _{IL} | | | | |
| | | I _O = -100 μA; V _{CC} = 1.65 V to 5.5 V | V _{CC} - 0.1 | - | - | V |
| | | I _O = -4 mA; V _{CC} = 1.65 V | 1.2 | - | - | V |
| | | I _O = -8 mA; V _{CC} = 2.3 V | 1.9 | - | - | V |
| | | I _O = -12 mA; V _{CC} = 2.7 V | 2.2 | - | - | V |
| | | I _O = -24 mA; V _{CC} = 3.0 V | 2.3 | - | - | V |
| V _{OL} | LOW-level output voltage | V _I = V _{IH} or V _{IL} | | | | |
| | | I _O = 100 μA; V _{CC} = 1.65 V to 5.5 V | - | - | 0.1 | V |
| | | I _O = 4 mA; V _{CC} = 1.65 V | - | - | 0.45 | V |
| | | I _O = 8 mA; V _{CC} = 2.3 V | - | - | 0.3 | V |
| | | I _O = 12 mA; V _{CC} = 2.7 V | - | - | 0.4 | V |
| | | I _O = 24 mA; V _{CC} = 3.0 V | - | - | 0.55 | V |
| I _O = 32 mA; V _{CC} = 4.5 V | - | - | 0.55 | V | | |
| I _I | input leakage current | V _I = 5.5 V or GND; V _{CC} = 0 V to 5.5 V | - | ±0.1 | ±1 | μA |
| I _{OFF} | power-off leakage current | V _{CC} = 0 V; V _I or V _O = 5.5 V | - | ±0.1 | ±2 | μA |
| I _{CC} | supply current | V _I = 5.5 V or GND; V _{CC} = 1.65 V to 5.5 V; I _O = 0 A | - | 0.1 | 4 | μA |
| ΔI _{CC} | additional supply current | per pin; V _{CC} = 2.3 V to 5.5 V; V _I = V _{CC} - 0.6 V; I _O = 0 A | - | 5 | 500 | μA |
| C _I | input capacitance | V _{CC} = 3.3 V; V _I = GND to V _{CC} | - | 5 | - | pF |

| Symbol | Parameter | Conditions | Min | Typ[1] | Max | Unit |
|--|---------------------------|--|------------------------|--------|------------------------|------|
| T_{amb} = -40 °C to +125 °C | | | | | | |
| V _{IH} | HIGH-level input voltage | V _{CC} = 1.65 V to 1.95 V | 0.65 × V _{CC} | - | - | V |
| | | V _{CC} = 2.3 V to 2.7 V | 1.7 | - | - | V |
| | | V _{CC} = 2.7 V to 3.6 V | 2.0 | - | - | V |
| | | V _{CC} = 4.5 V to 5.5 V | 0.7 × V _{CC} | - | - | V |
| V _{IL} | LOW-level input voltage | V _{CC} = 1.65 V to 1.95 V | - | - | 0.35 × V _{CC} | V |
| | | V _{CC} = 2.3 V to 2.7 V | - | - | 0.7 | V |
| | | V _{CC} = 2.7 V to 3.6 V | - | - | 0.8 | V |
| | | V _{CC} = 4.5 V to 5.5 V | - | - | 0.3 × V _{CC} | V |
| V _{OH} | HIGH-level output voltage | V _I = V _{IH} or V _{IL} | | | | |
| | | I _O = -100 μA; V _{CC} = 1.65 V to 5.5 V | V _{CC} - 0.1 | - | - | V |
| | | I _O = -4 mA; V _{CC} = 1.65 V | 0.95 | - | - | V |
| | | I _O = -8 mA; V _{CC} = 2.3 V | 1.7 | - | - | V |
| | | I _O = -12 mA; V _{CC} = 2.7 V | 1.9 | - | - | V |
| | | I _O = -24 mA; V _{CC} = 3.0 V | 2.0 | - | - | V |
| V _{OL} | LOW-level output voltage | V _I = V _{IH} or V _{IL} | | | | |
| | | I _O = 100 μA; V _{CC} = 1.65 V to 5.5 V | - | - | 0.1 | V |
| | | I _O = 4 mA; V _{CC} = 1.65 V | - | - | 0.70 | V |
| | | I _O = 8 mA; V _{CC} = 2.3 V | - | - | 0.45 | V |
| | | I _O = 12 mA; V _{CC} = 2.7 V | - | - | 0.60 | V |
| | | I _O = 24 mA; V _{CC} = 3.0 V | - | - | 0.80 | V |
| I _I | input leakage current | V _I = 5.5 V or GND; V _{CC} = 0 V to 5.5 V | - | - | ±1 | μA |
| | | V _{CC} = 0 V; V _I or V _O = 5.5 V | - | - | ±2 | μA |
| I _{OFF} | power-off leakage current | V _{CC} = 0 V; V _I or V _O = 5.5 V | - | - | ±2 | μA |
| I _{CC} | supply current | V _I = 5.5 V or GND; V _{CC} = 1.65 V to 5.5 V; I _O = 0 A | - | - | 4 | μA |
| ΔI _{CC} | additional supply current | per pin; V _{CC} = 2.3 V to 5.5 V; V _I = V _{CC} - 0.6 V; I _O = 0 A | - | - | 500 | μA |

[1] All typical values are measured at V_{CC} = 3.3 V and T_{amb} = 25 °C.

11. Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see Fig. 7.

| Symbol | Parameter | Conditions | -40 °C to +85 °C | | | -40 °C to +125 °C | | Unit |
|------------------|-------------------------------|---|------------------|--------|-----|-------------------|------|------|
| | | | Min | Typ[1] | Max | Min | Max | |
| t _{pd} | propagation delay | CP to Q; see Fig. 5 [2] | | | | | | |
| | | V _{CC} = 1.65 V to 1.95 V | 1.0 | 3.6 | 9.9 | 1.0 | 12.5 | ns |
| | | V _{CC} = 2.3 V to 2.7 V | 0.5 | 2.3 | 7.0 | 0.5 | 9.0 | ns |
| | | V _{CC} = 2.7 V | 0.5 | 2.6 | 6.0 | 0.5 | 8.0 | ns |
| | | V _{CC} = 3.0 V to 3.6 V | 0.5 | 2.2 | 5.0 | 0.5 | 6.5 | ns |
| | | V _{CC} = 4.5 V to 5.5 V | 0.5 | 1.7 | 3.8 | 0.5 | 5.0 | ns |
| t _{su} | set-up time | D to CP; see Fig. 6 | | | | | | |
| | | V _{CC} = 1.65 V to 1.95 V | 2.5 | 1.4 | - | 2.5 | - | ns |
| | | V _{CC} = 2.3 V to 2.7 V | 1.7 | 0.9 | - | 1.7 | - | ns |
| | | V _{CC} = 2.7 V | 1.7 | 0.9 | - | 1.7 | - | ns |
| | | V _{CC} = 3.0 V to 3.6 V | 1.3 | 0.6 | - | 1.2 | - | ns |
| | | V _{CC} = 4.5 V to 5.5 V | 1.2 | 0.6 | - | 1.2 | - | ns |
| t _h | hold time | D to CP; see Fig. 6 | | | | | | |
| | | V _{CC} = 1.65 V to 1.95 V | 0 | -0.7 | - | 0 | - | ns |
| | | V _{CC} = 2.3 V to 2.7 V | 0 | -0.4 | - | 0 | - | ns |
| | | V _{CC} = 2.7 V | +0.5 | -0.3 | - | 0.5 | - | ns |
| | | V _{CC} = 3.0 V to 3.6 V | +0.5 | -0.3 | - | 0.5 | - | ns |
| | | V _{CC} = 4.5 V to 5.5 V | +0.5 | -0.2 | - | 0.5 | - | ns |
| t _w | pulse width | CP HIGH or LOW; see Fig. 6 | | | | | | |
| | | V _{CC} = 1.65 V to 1.95 V | 3.0 | 1.1 | - | 3.0 | - | ns |
| | | V _{CC} = 2.3 V to 2.7 V | 2.5 | 0.7 | - | 2.5 | - | ns |
| | | V _{CC} = 2.7 V | 2.5 | 0.6 | - | 2.5 | - | ns |
| | | V _{CC} = 3.0 V to 3.6 V | 2.5 | 0.6 | - | 2.5 | - | ns |
| | | V _{CC} = 4.5 V to 5.5 V | 2.0 | 0.5 | - | 2.0 | - | ns |
| f _{max} | maximum frequency | CP; see Fig. 6 | | | | | | |
| | | V _{CC} = 1.65 V to 1.95 V | 160 | 250 | - | 160 | - | MHz |
| | | V _{CC} = 2.3 V to 2.7 V | 160 | 300 | - | 160 | - | MHz |
| | | V _{CC} = 2.7 V | 160 | 350 | - | 160 | - | MHz |
| | | V _{CC} = 3.0 V to 3.6 V | 160 | 450 | - | 160 | - | MHz |
| | | V _{CC} = 4.5 V to 5.5 V | 200 | 500 | - | 200 | - | MHz |
| C _{PD} | power dissipation capacitance | V _I = GND to V _{CC} ; V _{CC} = 3.3 V [3] | - | 17 | - | - | - | pF |

[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.8 V, 2.5 V, 2.7 V, 3.3 V and 5.0 V respectively.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz; f_o = output frequency in MHz; C_L = output load capacitance in pF;

V_{CC} = supply voltage in V; N = number of inputs switching; $\sum(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

11.1. Waveforms and test circuit

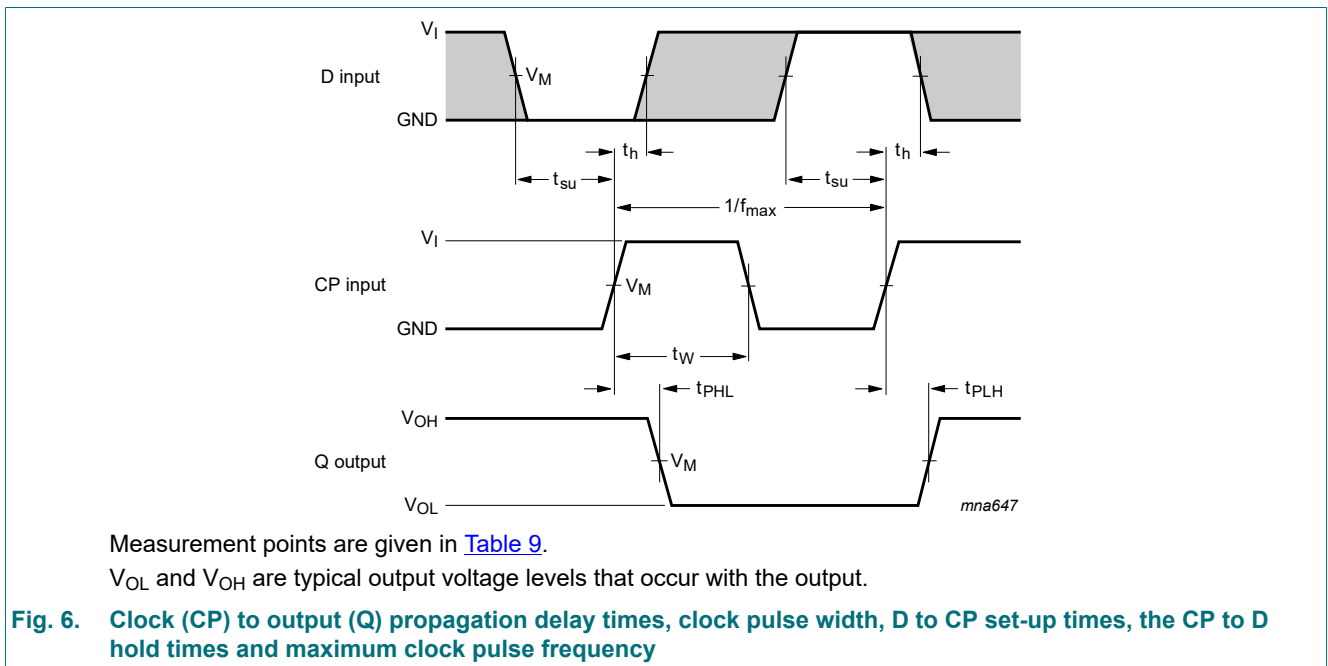
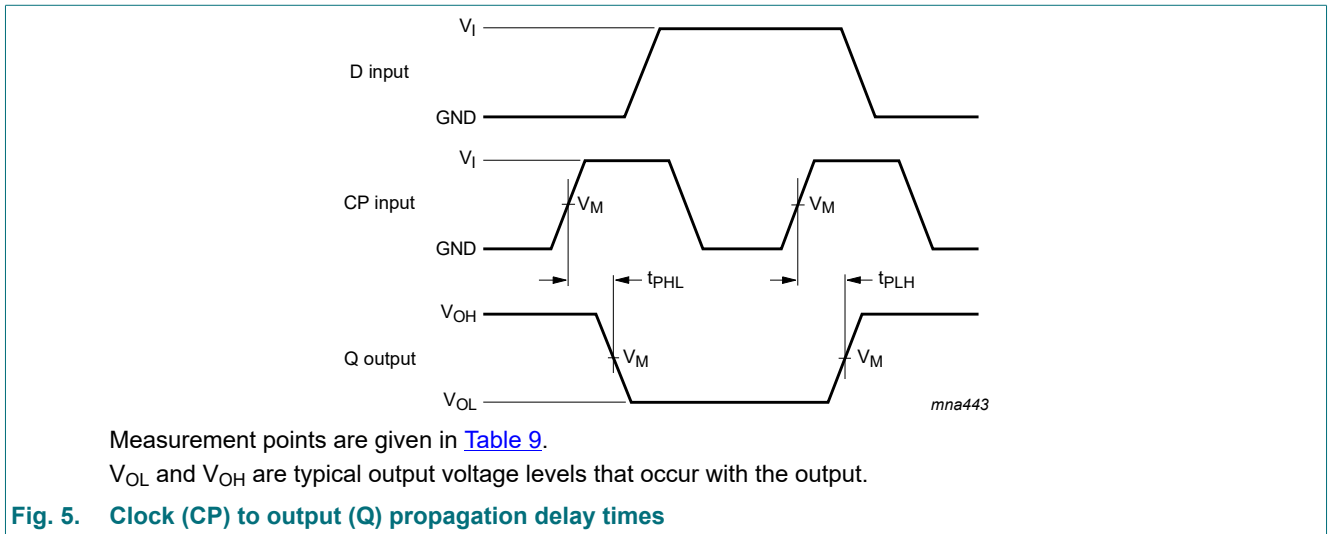
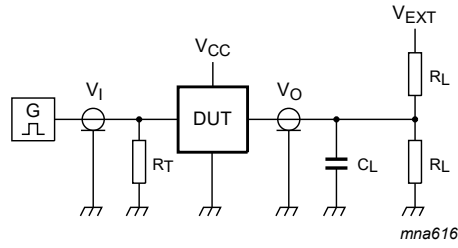


Table 9. Measurement points

| Supply voltage | Input | Output |
|------------------|---------------------|---------------------|
| V_{CC} | V_M | V_M |
| 1.65 V to 1.95 V | $0.5 \times V_{CC}$ | $0.5 \times V_{CC}$ |
| 2.3 V to 2.7 V | $0.5 \times V_{CC}$ | $0.5 \times V_{CC}$ |
| 2.7 V | 1.5 V | 1.5 V |
| 3.0 V to 3.6 V | 1.5 V | 1.5 V |
| 4.5 V to 5.5 V | $0.5 \times V_{CC}$ | $0.5 \times V_{CC}$ |



Test data is given in [Table 10](#).

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

Fig. 7. Test circuit for measuring switching times

Table 10. Test data

| Supply voltage | Input | | Load | | V_{EXT} |
|------------------|----------|---------------|-------|--------------|--------------------|
| V_{CC} | V_I | $t_r = t_f$ | C_L | R_L | t_{PLH}, t_{PHL} |
| 1.65 V to 1.95 V | V_{CC} | ≤ 2.0 ns | 30 pF | 1 k Ω | open |
| 2.3 V to 2.7 V | V_{CC} | ≤ 2.0 ns | 30 pF | 500 Ω | open |
| 2.7 V | 2.7 V | ≤ 2.5 ns | 50 pF | 500 Ω | open |
| 3.0 V to 3.6 V | 2.7 V | ≤ 2.5 ns | 50 pF | 500 Ω | open |
| 4.5 V to 5.5 V | V_{CC} | ≤ 2.5 ns | 50 pF | 500 Ω | open |

12. Package outline

TSSOP5: plastic thin shrink small outline package; 5 leads; body width 1.25 mm

SOT353-1



Fig. 8. Package outline SOT353-1 (TSSOP5)

Plastic surface-mounted package; 5 leads

SOT753

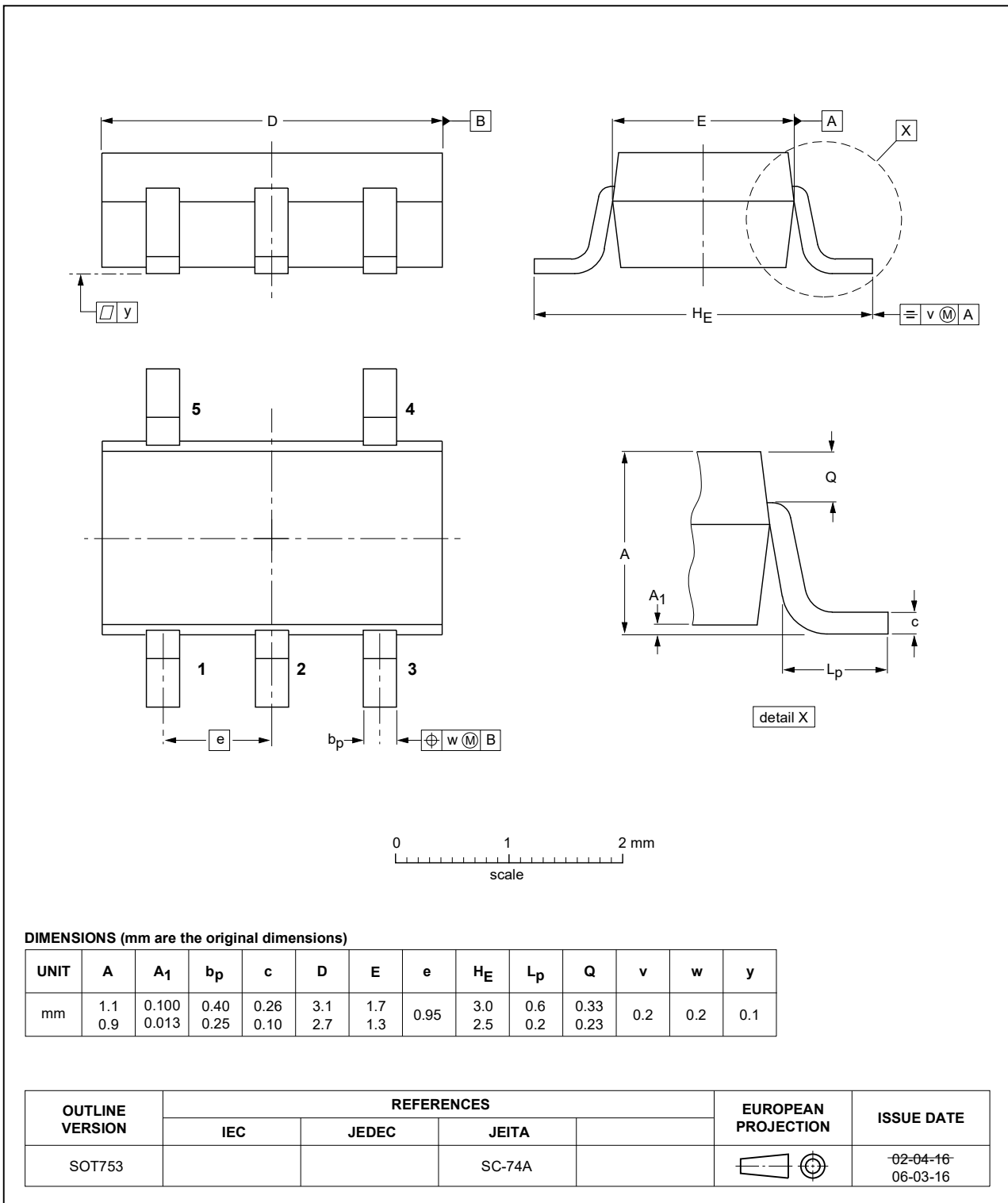


Fig. 9. Package outline SOT753 (SC-74A)

13. Abbreviations

Table 11. Abbreviations

| Acronym | Description |
|---------|---|
| CMOS | Complementary Metal Oxide Semiconductor |
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| MIL | Military |
| MM | Machine Model |
| TTL | Transistor-Transistor Logic |

14. Revision history

Table 12. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|--------------------|---|--------------------|---------------|--------------------|
| 74LVC1G79_Q100 v.3 | 20220201 | Product data sheet | - | 74LVC1G79_Q100 v.2 |
| Modifications: | <ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. Section 1 and Section 2 updated. Table 5: Derating values for P_{tot} total power dissipation updated. Fig. 8: Package outline drawing SOT353-1 (TSSOP5) has changed. | | | |
| 74LVC1G79_Q100 v.2 | 20161212 | Product data sheet | - | 74LVC1G79_Q100 v.1 |
| Modifications: | <ul style="list-style-type: none"> Table 7: The maximum limits for leakage current and supply current have changed. | | | |
| 74LVC1G79_Q100 v.1 | 20150512 | Product data sheet | - | - |

15. Legal information

Data sheet status

| Document status [1][2] | Product status [3] | Definition |
|--------------------------------|--------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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