NCP3155A, NCP3155B

3 A Synchronous Buck Regulator

The NCP3155 is a DC/DC synchronous switching regulator with fully integrated power switches and full fault protection. The switching frequency of 1 MHz and 500 kHz allows the use of small filter components, which results in smaller board space and reduced BOM cost. Available in a SOIC-8 package.

Features

- Input Voltage Range from 4.7 V to 24 V
- Adjustable Output Voltage
- 1 MHz Operation (NCP3155A – 500 kHz)
- Internally Programmed 1.2 ms Soft−Start (NCP3155A – 2.4 ms)
- 0.8 ± 1.0% Reference Voltage
- 48 mΩ HS−FET and 18 mΩ LS−FET
- Current Limit Protection
- Transconductance Amplifier with External Compensation
- Input Undervoltage Lockout
- Output Overvoltage and Undervoltage Detection
- These are Pb−Free Devices

Typical Applications

- Set Top Boxes
- DVD Drives and HDD
- LCD Monitors and TVs
- Cable Modems
- Telecom/Networking/Datacom Equipment

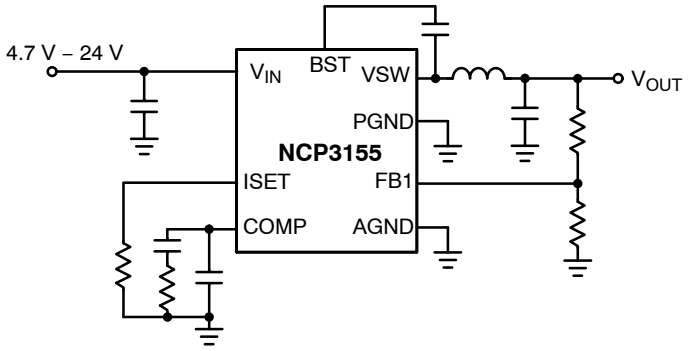


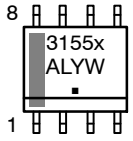
Figure 1. Typical Application Circuit

ON Semiconductor®

http://onsemi.com

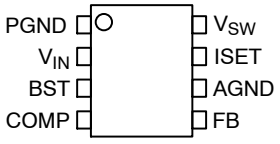
SOIC−8 NB
CASE 751

MARKING DIAGRAM



3155x	= Specific Device Code
	x = A or B
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
NCP3155ADR2G	SOIC−8 (Pb−Free)	2500 / Tape & Reel
NCP3155BDR2G	SOIC−8 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

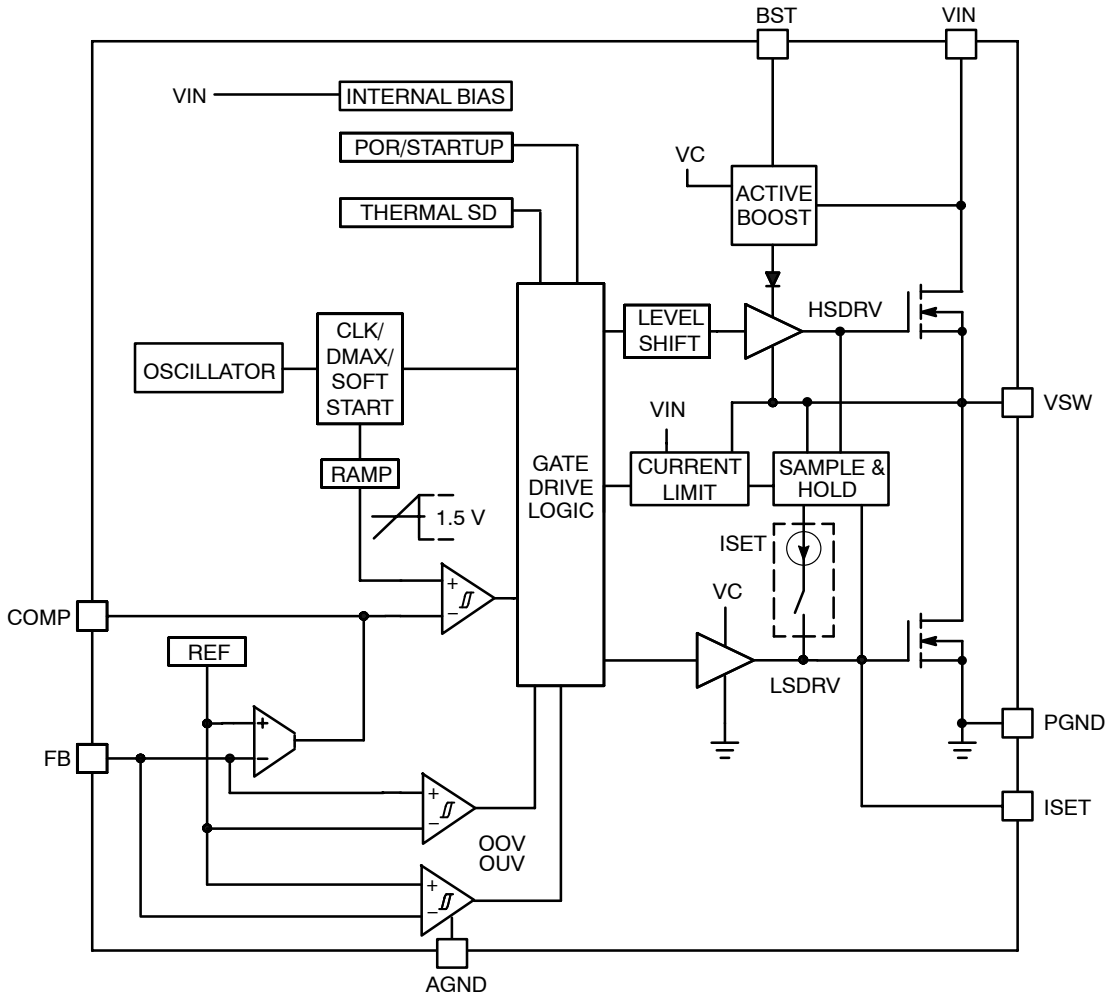


Figure 2. NCP3155 Block Diagram

PIN FUNCTION DESCRIPTION

Pin	Pin Name	Description
1	PGND	The PGND pin is the high current ground pin for the lower MOSFET and drivers which should be soldered to a large copper area to reduce thermal resistance.
2	V_{IN}	The V_{IN} pin powers the internal control circuitry and is monitored by an undervoltage comparator. The V_{IN} pin is also connected to the internal power NMOS switch. It is also used in conjunction with the V_{SW} pin to sense current in the high side MOSFET. The V_{IN} pin has high dI/dt edges and must be decoupled to PGND pin close to the pin of the device.
3	BST	Supply rail for the floating top gate driver. Connect a capacitor (CBST) between this pin and the V_{SW} pin. Typical values for CBST range from 1 nF to 100 nF.
4	COMP	Compensation pin. The comp pin is the output of the transconductance amplifier and the non−inverting input of the PWM comparator. The comp pin in conjunction with the FB pin are used to compensate the voltage−control feedback loop.
5	FB	Inverting input to the Operational Transconductance Amplifier (OTA). The FB pin in conjunction with the external compensation serves to stabilize and achieve the desired output voltage with voltage mode compensation.
6	AGND	The AGND pin serves as small−signal ground. All small−signal ground paths should connect to the AGND pin at a single point to avoid any high current ground returns.
7	ISET	Bottom gate MOSFET driver pin and the internal current set pin. Place a resistor to ground to set the current limit of the converter.
8	V_{SW}	The V_{SW} pin is the connection of the drain and source of the internal N MOSFETS. The V_{SW} pin swings from V_{IN} when the high side switch is on to small negative voltages when the low side switch is on with high dV/dt transitions.

ABSOLUTE MAXIMUM RATINGS (measured vs. GND pin 8, unless otherwise noted)

Rating	Symbol	V_{MAX}	V_{MIN}	Unit
Main Supply Voltage Input	V_{CC}	26.4	−0.3	V
Boost to V_{SW} differential voltage	BST−V_{SW}	13.2	−0.3	V
High Side Drive Boost Pin	BST	45	−0.3	V
Switch Voltage Node	V_{SW}	30	−0.6	V
Transconductance Amplifier Output	COMP	5.5	−0.3	V
Feedback	FB	6.0	−0.3	V
Current Limit Set	ISET	13.2	−0.3	V
Operating Junction Temperature Range (Note 1)	T_J	−40 to +125		°C
Maximum Junction Temperature	$T_{J(MAX)}$	+150		°C
Storage Temperature Range	T_{stg}	−55 to +150		°C
Thermal Characteristics − SOIC−8 Package (Note 2) Thermal Resistance Junction−to−Air (Note 3)	$R_{\theta JA}$	110 170		°C/W
Lead Temperature Soldering (10 sec): Reflow (SMD styles only) Pb−Free (Note 3)	R_F	260 Peak		°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. The maximum package power dissipation limit must not be exceeded.

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

2. The value of θ_{JA} is measured with the device mounted on 1 in2 FR − 4 board with 1 oz. copper, in a still air environment with T_A = 25°C. The value in any given application depends on the user's specific board design.
3. The value of θ_{JA} is measured with the device mounted on minimum footprint, in a still air environment with T_A = 25°C. The value in any given application depends on the user's specific board design.

ELECTRICAL CHARACTERISTICS ($-40°C < T_J < +125°C$, V_{CC} = 12 V, for min/max values unless otherwise noted)

Characteristic		Conditions	Min	Typ	Max	Unit
Input Voltage Range		–	4.7		24	V
SUPPLY CURRENT						
V_{CC} Supply Current	NCP3155A	V_{FB} = 0.8 V, Switching, V_{CC} = 4.7 V	–	11.1	–	mA
		V_{FB} = 0.8 V, Switching, V_{CC} = 24 V	–	31.5	–	mA
V_{CC} Supply Current	NCP3155B	V_{FB} = 0.8 V, Switching, V_{CC} = 4.7 V	–	16.5	–	mA
		V_{FB} = 0.8 V, Switching, V_{CC} = 24 V	–	54.7	–	mA
UNDER VOLTAGE LOCKOUT						
UVLO Rising Threshold		V_{CC} Rising Edge	4.0	4.3	4.7	V
UVLO Falling Threshold		V_{CC} Falling Edge	3.5	3.9	4.3	V
OSCILLATOR						
Oscillator Frequency	NCP3155A	T_J = +25°C, 4.7 V ≤ V_{CC} ≤ 24 V	415	500	585	kHz
		T_J = −40°C to +125°C, 4.7 V ≤ V_{CC} ≤ 24 V	400	500	600	kHz
Oscillator Frequency	NCP3155B	T_J = +25°C, 4.7 V ≤ V_{CC} ≤ 24 V	830	1000	1170	kHz
		T_J = −40°C to +125°C, 4.7 V ≤ V_{CC} ≤ 24 V	820	1000	1180	kHz
Ramp−Amplitude Voltage		$V_{peak} - V_{alley}$	–	1.5	–	V
Ramp Valley Voltage			0.46	0.71	0.85	V
PWM						
Minimum Duty Cycle		(Note 4)	–	7.0	–	%
Maximum Duty Cycle			80	84	–	%
Soft Start Ramp Time	NCP3155A NCP3155B	$V_{FB} = V_{COMP}$	– –	2.4 1.2	– –	ms
ERROR AMPLIFIER (GM)						
Transconductance			0.9	1.3	1.9	mS
Open Loop dc Gain		(Notes 4 and 6)	–	70	–	dB
Output Source Current		V_{FB} = 750 mV	45	70	100	μA
Output Sink Current		V_{FB} = 850 mV	45	70	100	μA
FB Input Bias Current			–	0.5	500	nA
Feedback Voltage		TJ = 25 C 4.7 V < V_{IN} < 24 V, −40°C < T_J < +125°C	0.792 0.784	0.8 0.8	0.808 0.816	V V
COMP High Voltage		V_{FB} = 750 mV	4.0	4.4	5.0	V
COMP Low Voltage		V_{FB} = 850 mV	–	72	250	mV
OUTPUT VOLTAGE FAULTS						
Feedback OOV Threshold			0.91	1.00	1.09	V
Feedback OUV Threshold			0.56	0.60	0.64	V
PWM OUTPUT STAGE						
High−Side Switch On Resistance		V_{IN} = 12 V V_{IN} = 4.7 V	– –	48 65	63 85	mΩ
Low−Side Switch On Resistance		V_{IN} = 12 V V_{IN} = 4.7 V	– –	18 21	35 50	mΩ
OVERCURRENT						
ISET Source Current			7	13.5	18	μA
Current Limit Set Voltage (Note 5)		R_{SET} = 22.1 kΩ	–	298	–	mV
THERMAL SHUTDOWN						
Thermal Shutdown		(Notes 4 and 7)	–	175	–	°C
Hysteresis		(Notes 4 and 7)	–	20	–	°C

4. Guaranteed by design.
5. The voltage sensed across the high side MOSFET during conduction.
6. This assumes 100 pF capacitance to ground on the COMP Pin and a typical internal R_o of > 10 MΩ.
7. This is not a protection feature.

TYPICAL PERFORMANCE CHARACTERISTICS

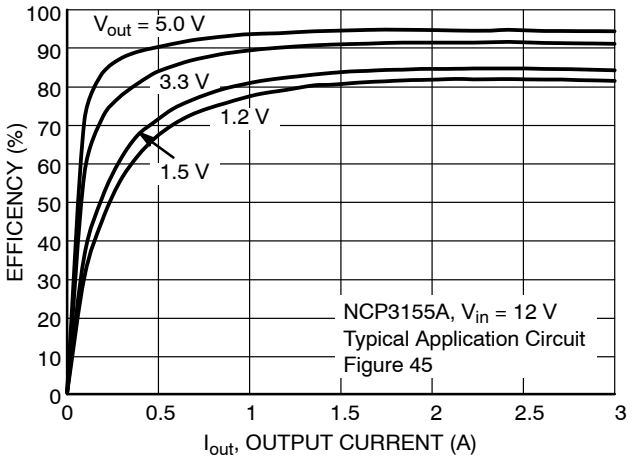


Figure 3. Efficiency vs Output Current and Output Voltage

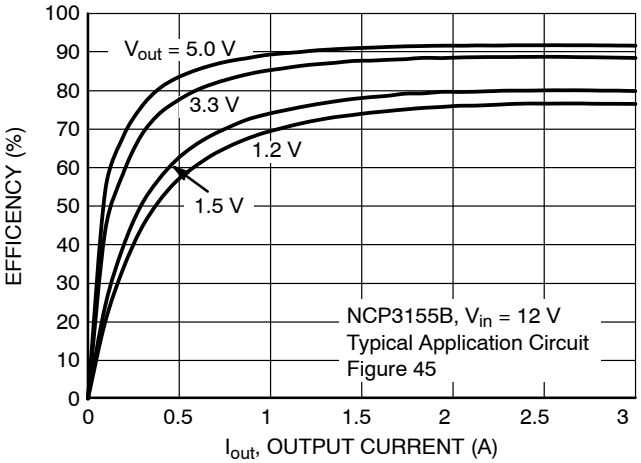


Figure 4. Efficiency vs Output Current and Output Voltage

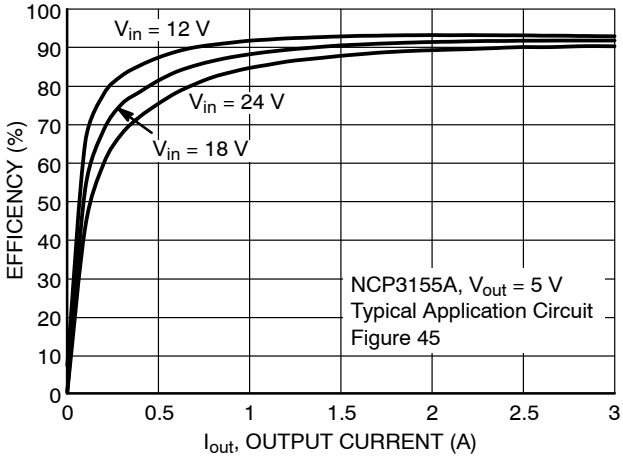


Figure 5. Efficiency vs Output Current and Input Voltage

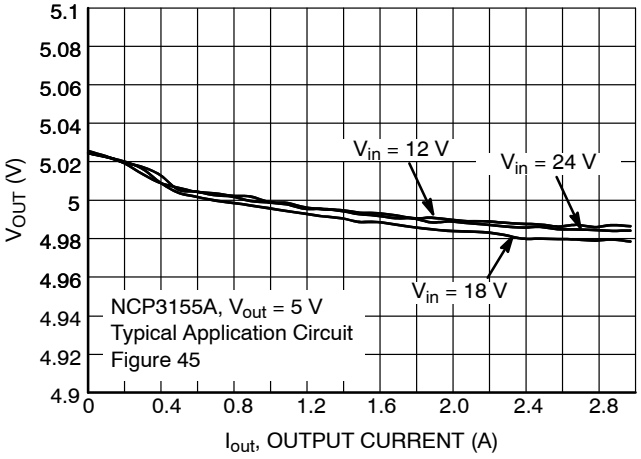
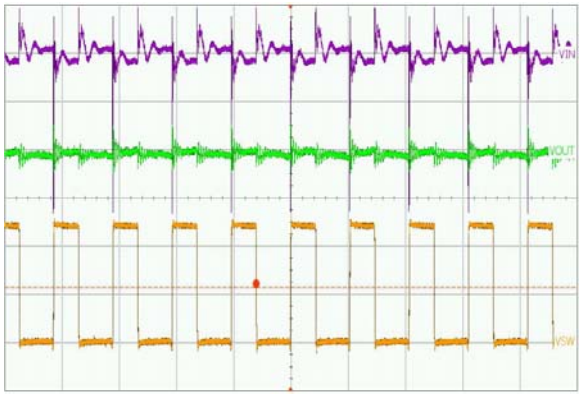
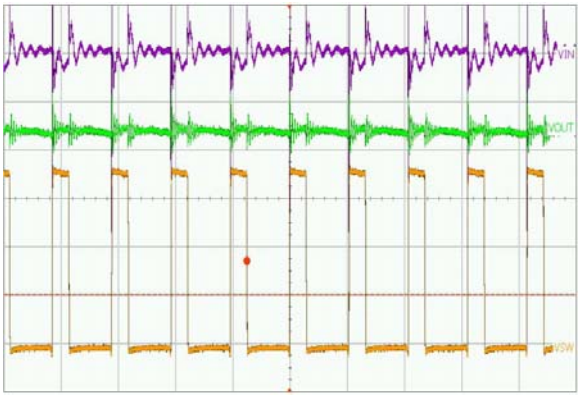


Figure 6. Load Regulation vs Input Voltage



Input = 12 V, Output = 5.0 V, Load = 2 A,
CH3 (Purple) = V_{IN}, (CH2) Green = V_{OUT}, CH1 (Yellow) = VSW
CH3: 200 mVac/div; CH2: 50 mVac/div; CH1: 5.0 V/div
Time Scale: 2.0 μs/div; Figure 45

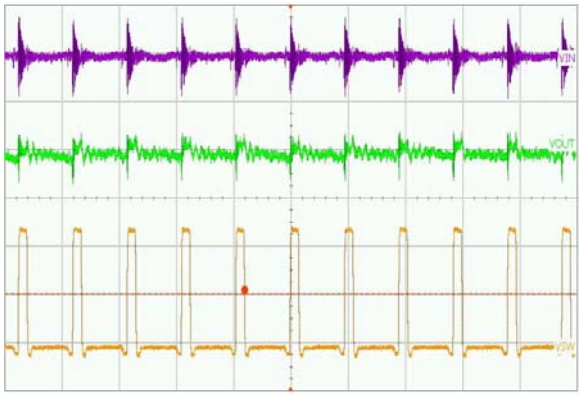
Figure 7. Switching Waveforms (NCP3155A)



Input = 18 V, Output = 5.0 V, Load = 2 A,
CH3 (Purple) = V_{IN}, (CH2) Green = V_{OUT}, CH1 (Yellow) = VSW
CH3: 200 mVac/div; CH2: 50 mVac/div; CH1: 5.0 V/div
Time Scale: 2.0 μs/div; Figure 45

Figure 8. Switching Waveforms (NCP3155A)

TYPICAL PERFORMANCE CHARACTERISTICS



Input = 12 V, Output = 1.8 V, Load = 2 A,
CH3 (Purple) = V_{IN}, (CH2) Green = V_{OUT}, CH1 (Yellow) = VSW
CH3: 200 mVac/div; CH2: 50 mVac/div; CH1: 5.0 V/div
Time Scale: 1.0 μs/div; Figure 46

Figure 9. Switching Waveforms (NCP3155B)

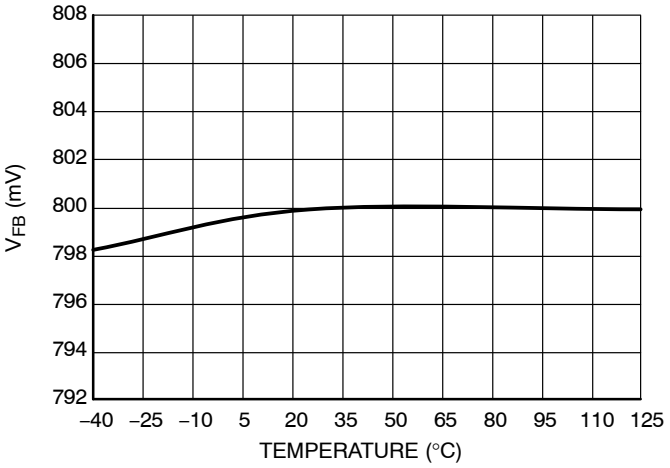


Figure 10. Feedback Reference Voltage vs Temperature

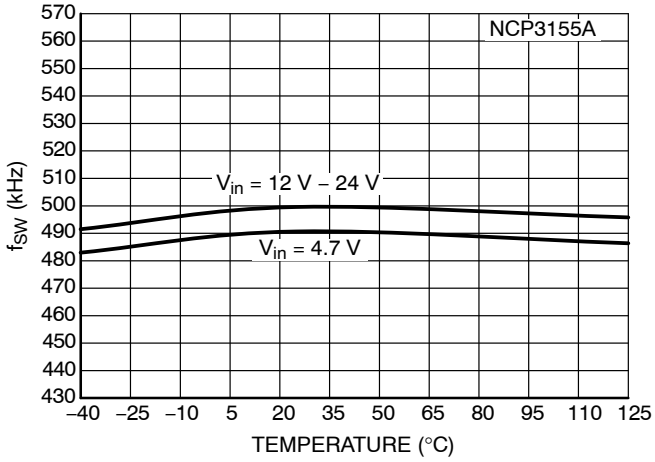


Figure 11. Switching Frequency vs Input Voltage and Temperature

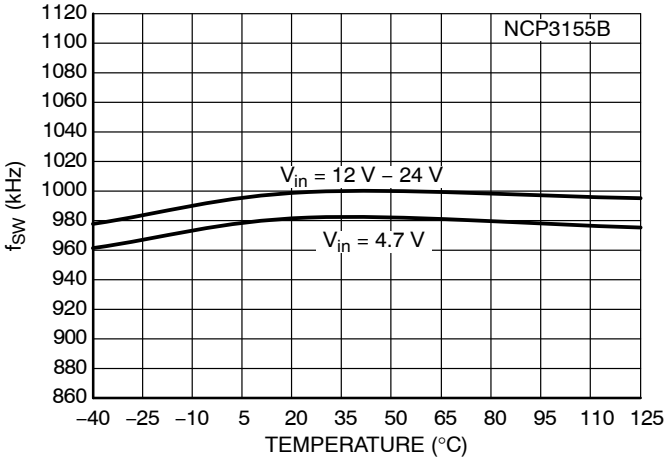


Figure 12. Switching Frequency vs Input Voltage and Temperature

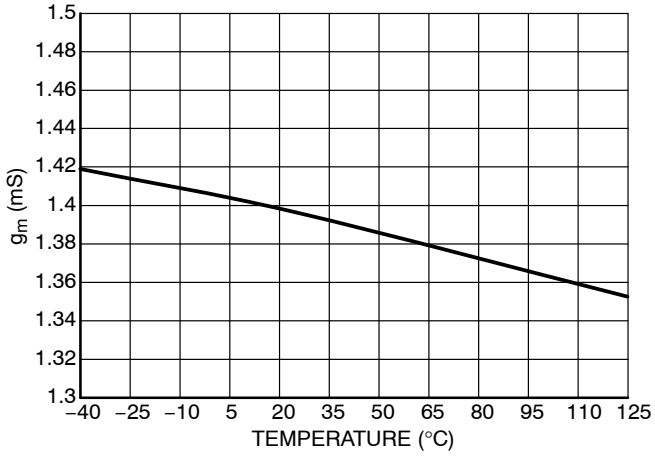


Figure 13. Transconductance vs Temperature

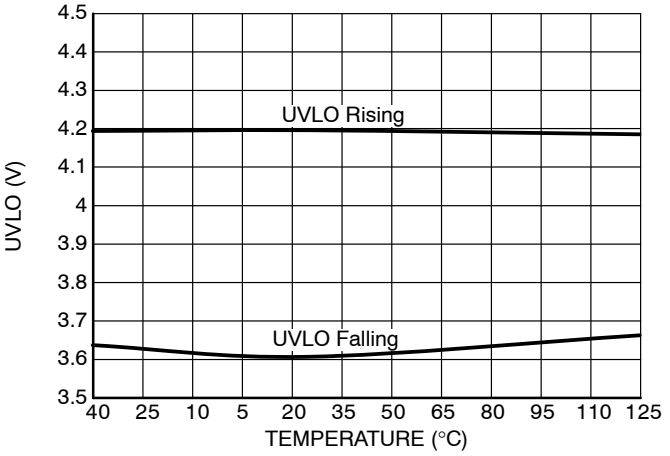


Figure 14. Input Undervoltage vs Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

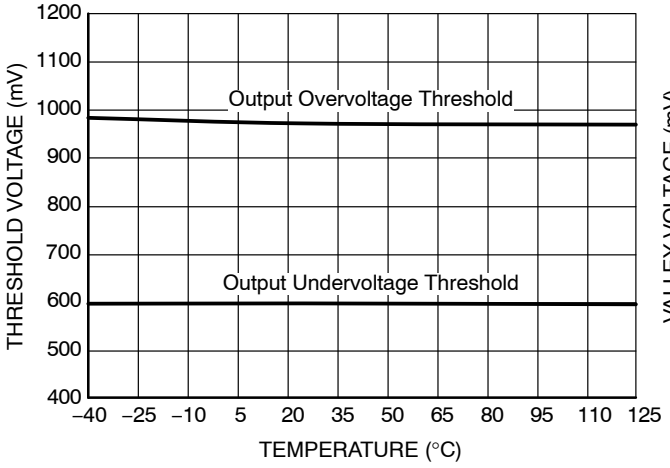


Figure 15. Output Protection vs Temperature

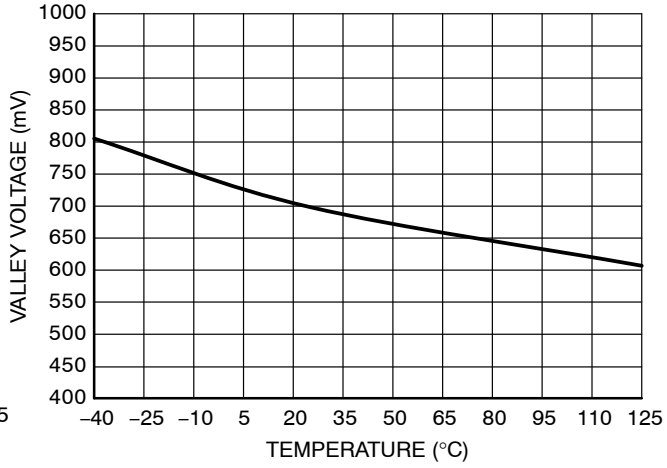


Figure 16. Ramp Valley Voltage vs Temperature

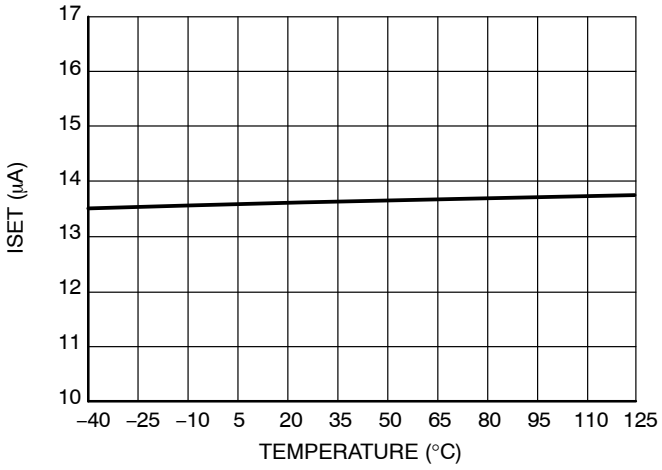
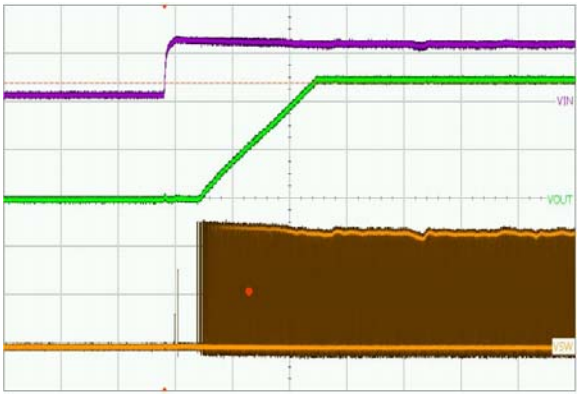
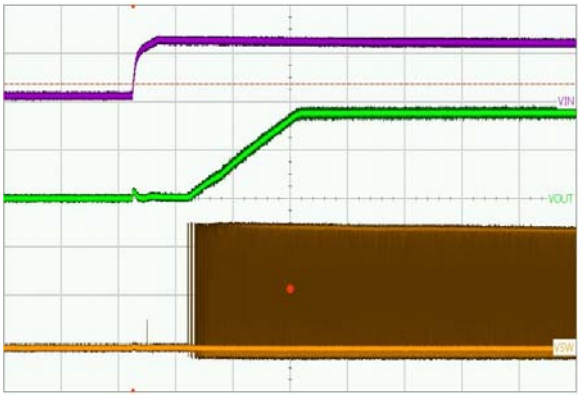


Figure 17. ISET Current vs Temperature



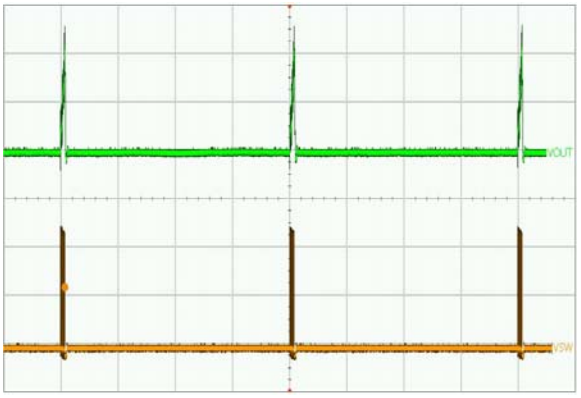
Input = 12 V, Output = 1.8 V, Load = 2 A,
CH3 (Purple) = V_{IN}, (CH2) Green = V_{OUT}, CH1 (Yellow) = VSW
CH3: 10 V/div; CH2: 2.0 V/div; CH1: 5.0 V/div
Time Scale: 1.0 ms/div; Figure 45

Figure 18. Startup Waveforms (NCP3155A)



Input = 12 V, Output = 1.8 V, Load = 2 A,
CH3 (Purple) = V_{IN}, (CH2) Green = V_{OUT}, CH1 (Yellow) = VSW
CH3: 10 V/div; CH2: 1.0 V/div; CH1: 5.0 V/div
Time Scale: 0.5 ms/div; Figure 46

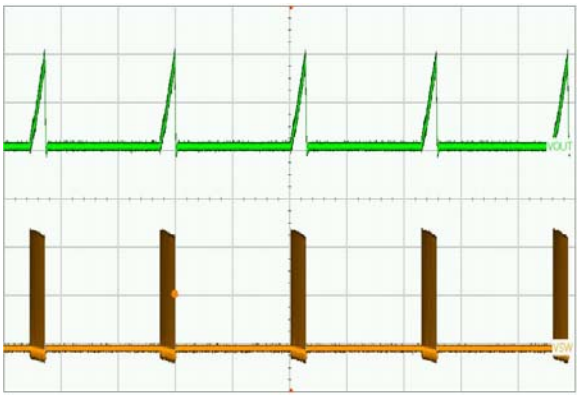
Figure 19. Startup Waveforms (NCP3155B)



Input = 12 V
(CH2) Green = V_{OUT}, CH1 (Yellow) = VSW
CH2: 0.5 V/div; CH1: 5.0 V/div
Time Scale: 2.0 ms/div; Figure 45

Figure 20. Current Limit Waveforms (NCP3155A)

TYPICAL PERFORMANCE CHARACTERISTICS



Input = 12 V
(CH2) Green = V_{OUT}, CH1 (Yellow) = VSW
CH2: 0.5 V/div; CH1: 5.0 V/div
Time Scale: 2.0 ms/div; Figure 46

Figure 21. Current Limit Waveforms (NCP3155B)

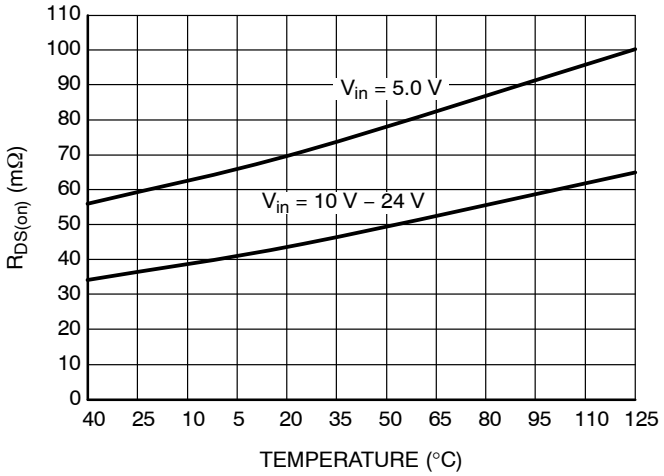


Figure 22. High−Side MOSFET $R_{DS(on)}$ vs Temperature

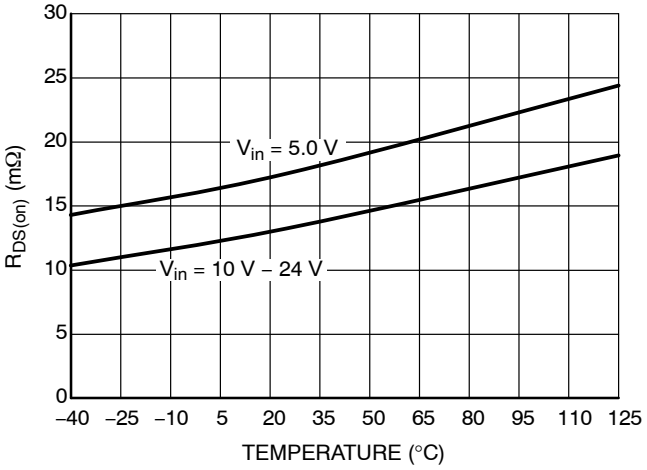


Figure 23. Low−Side MOSFET $R_{DS(on)}$ vs Temperature

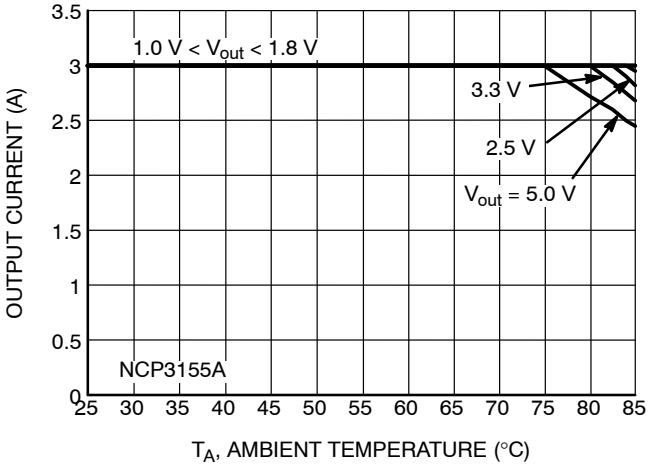


Figure 24. Derating Curve, 12 V Input

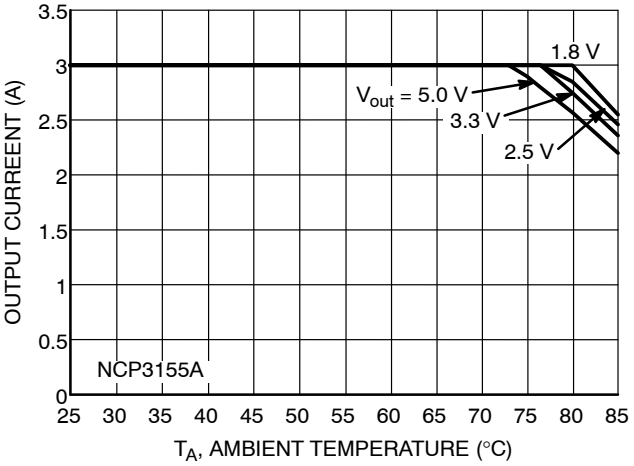


Figure 25. Derating Curve, 18 V Input

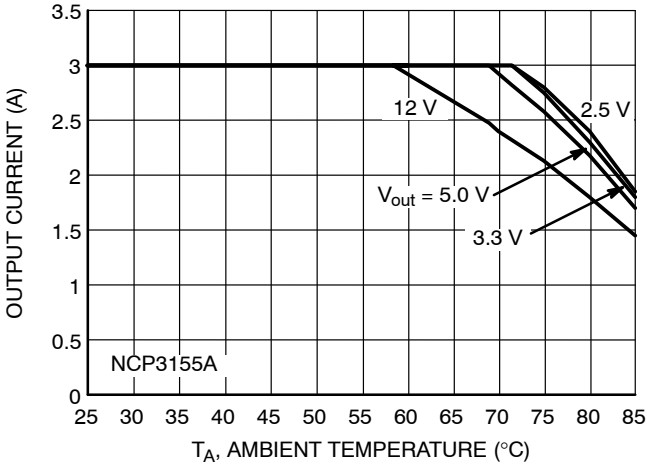


Figure 26. Derating Curve, 24 V Input

TYPICAL PERFORMANCE CHARACTERISTICS

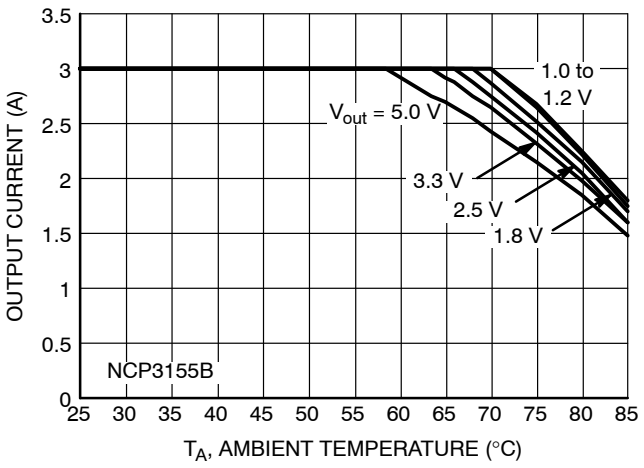


Figure 27. Derating Curve, 12 V Input

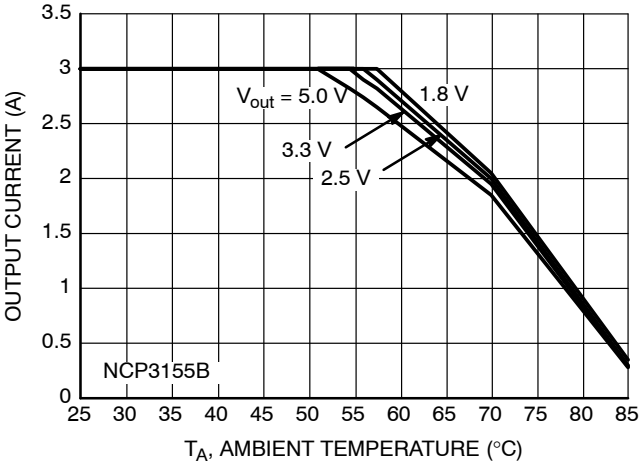


Figure 28. Derating Curve, 18 V Input

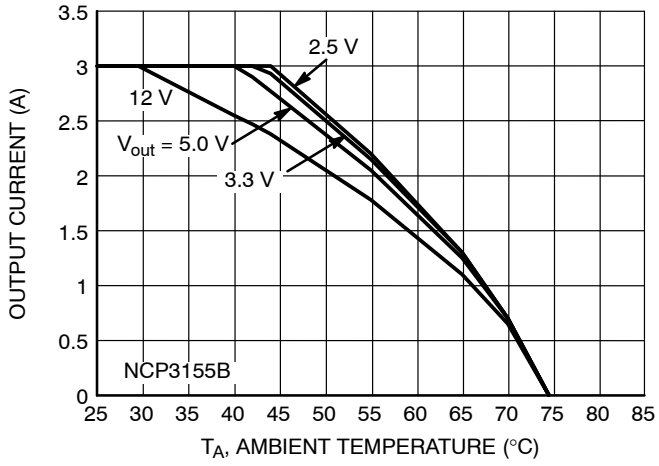


Figure 29. Derating Curve, 24 V Input

DETAILED DESCRIPTION

OVERVIEW

The NCP3155A/B operates as a 500 kHz/1.0 MHz, voltage mode, pulse width modulated, (PWM) synchronous buck converter. It drives high−side and low−side N−channel power MOSFETs. The NCP3155 incorporates an internal boost circuit consisting of a boost clamp and boost diode to provide supply voltage for the high side MOSFET gate driver. The NCP3155 also integrates several protection features including input undervoltage lockout (UVLO), output undervoltage (OUV), output overvoltage (OOV), adjustable high−side current limit (I_{SET} and I_{LIM}), and thermal shutdown (TSD).

The operational transconductance amplifier (OTA) provides a high gain error signal from Vout which is compared to the internal 1.5 V pk-pk ramp signal to set the duty cycle converter using the PWM comparator. The high side switch is turned on by the positive edge of the clock cycle going into the PWM comparator and flip flop following a non-overlap time. The high side switch is turned off when the PWM comparator output is tripped by the modulator ramp signal reaching a threshold level established by the error amplifier. The gate driver stage incorporates fixed non− overlap time between the high−side and low−side MOSFET gate drives to prevent cross conduction of the power MOSFET's.

POR and UVLO

The device contains an internal Power On Reset (POR) and input Undervoltage Lockout (UVLO) that inhibits the internal logic and the output stage from operating until V_{CC} reaches its respective predefined voltage levels (4.3 V typical).

Startup and Shutdown

Once V_{CC} crosses the UVLO rising threshold the device begins its startup process. Closed−loop soft−start begins after a 400 μs delay wherein the boost capacitor is charged, and the current limit threshold is set. During the 400 μs delay the OTA output is set to just below the valley voltage of the internal ramp. This is done to reduce delays and to ensure a consistent pre−soft−start condition. The device increases the internal reference from 0 V to 0.8 V in 32 discrete steps while maintaining closed loop regulation at each step. Each step contains 32 switching cycles. Some overshoot may be evident at the start of each step depending on the voltage loop phase margin and bandwidth. The total soft−start time is 2.4 ms for the NCP3155A and 1.2 ms for the NCP3155B.

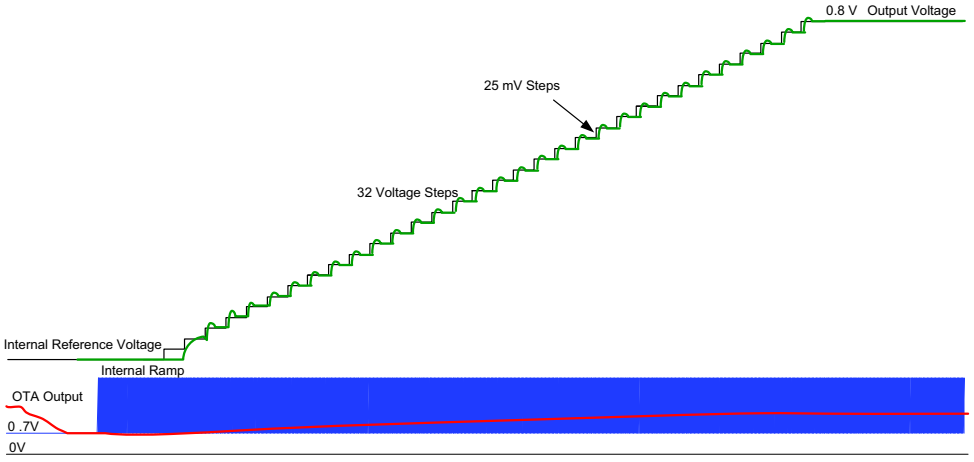


Figure 30. Soft−Start Details

OOV and OUV

The output voltage of the buck converter is monitored at the feedback pin of the output power stage. Two comparators are placed on the feedback node of the OTA to monitor the operating window of the feedback voltage as shown in Figures 31 and 32. All comparator outputs are ignored during the soft−start sequence as soft−start is regulated by the OTA and false trips would be generated. After the soft−start period has ended, if the feedback is below the reference voltage of comparator 2 (V_{FB} < 0.6 V), the output is considered “undervoltage” and the device will initiate a restart. When the feedback pin voltage rises between the reference voltages of comparator 1 and comparator 2 (0.6 < V_{FB} < 1.0), then the output voltage is considered “Power Good.” Finally, if the feedback voltage is greater than comparator 1 (V_{FB} > 1.0 V), the output voltage is considered “overvoltage,” and the device will latch off. To clear a latch fault, input voltage must be recycled. Graphical representation of the OOV and OUV is shown in Figures 33 and 34.

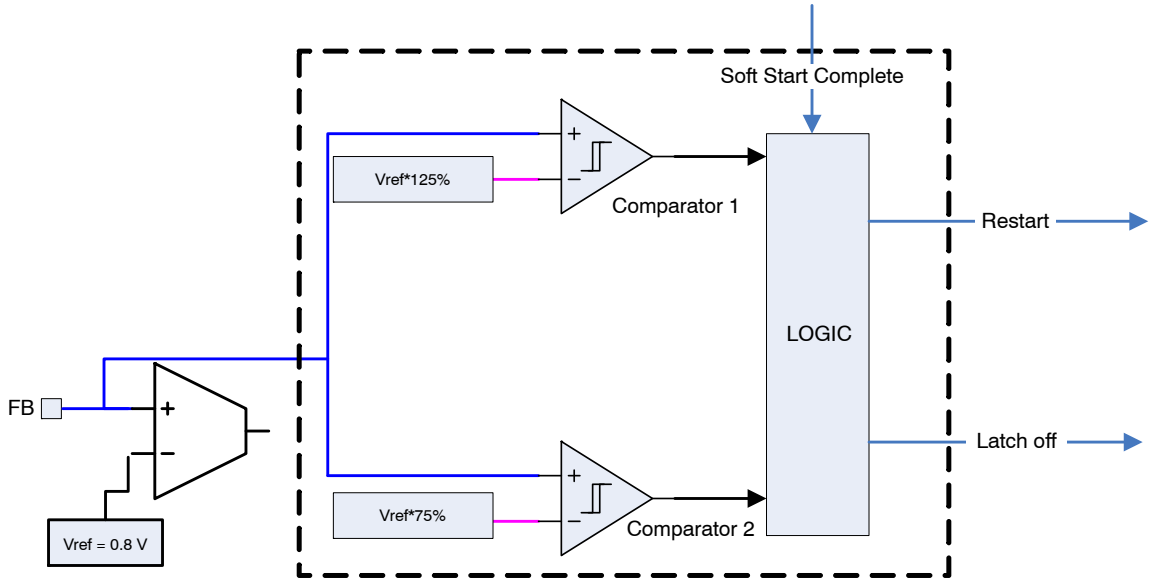


Figure 31. OOV and OUV Circuit Diagram

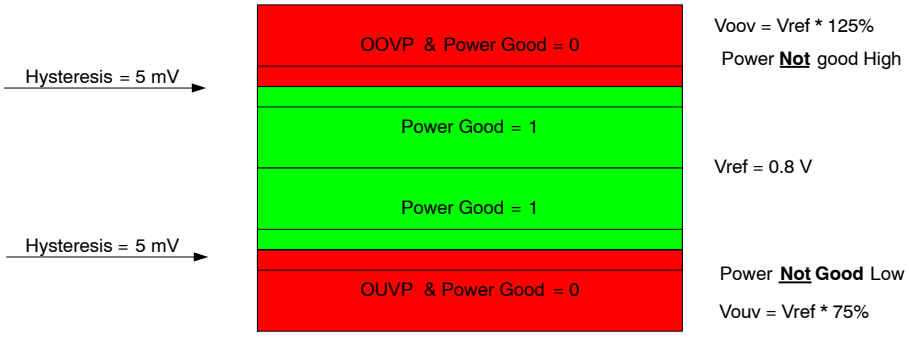


Figure 32. OOV and OUV Window Diagram

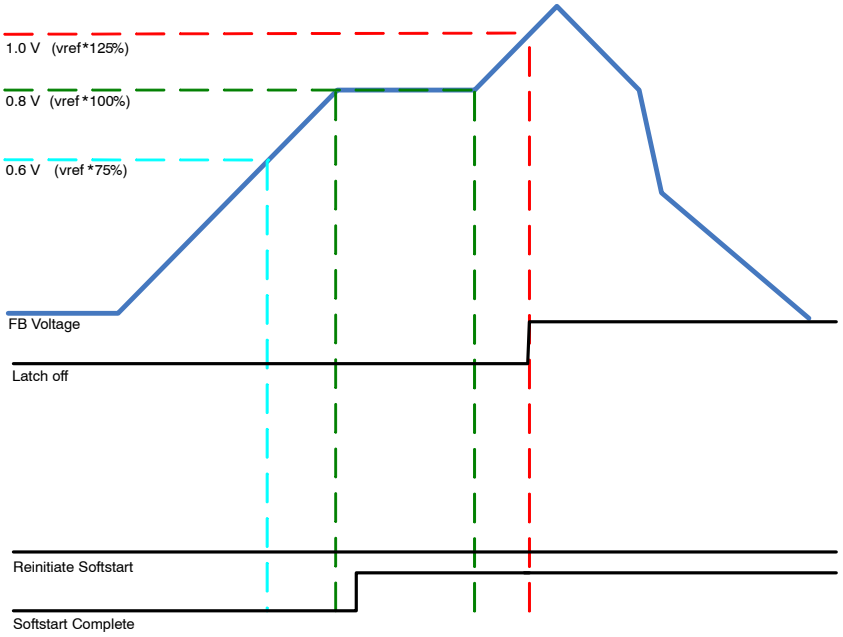


Figure 33. Powerup Sequence and Overvoltage Latch

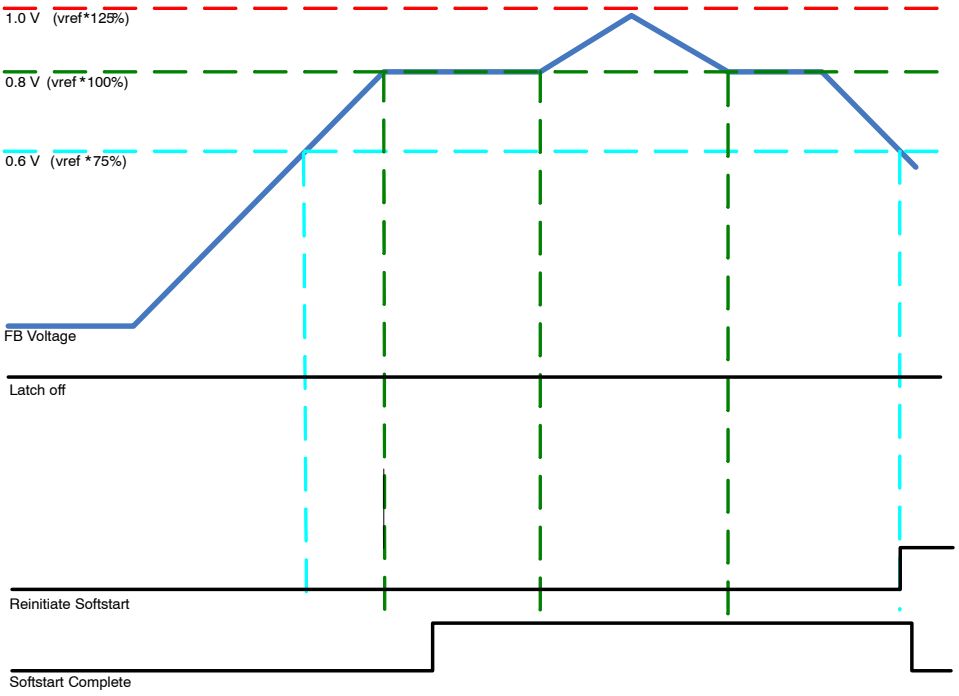


Figure 34. Powerup Sequence and Undervoltage Soft−Start

CURRENT LIMIT AND CURRENT LIMIT SET

Overview

The NCP3155 uses the voltage drop across the High Side MOSFET during the on time to sense inductor current. The I_{Limit} block consists of a voltage comparator circuit which compares the differential voltage across the V_{CC} Pin and the V_{SW} Pin with a resistor settable voltage reference. The sense portion of the circuit is only active while the HS MOSFET is turned ON.

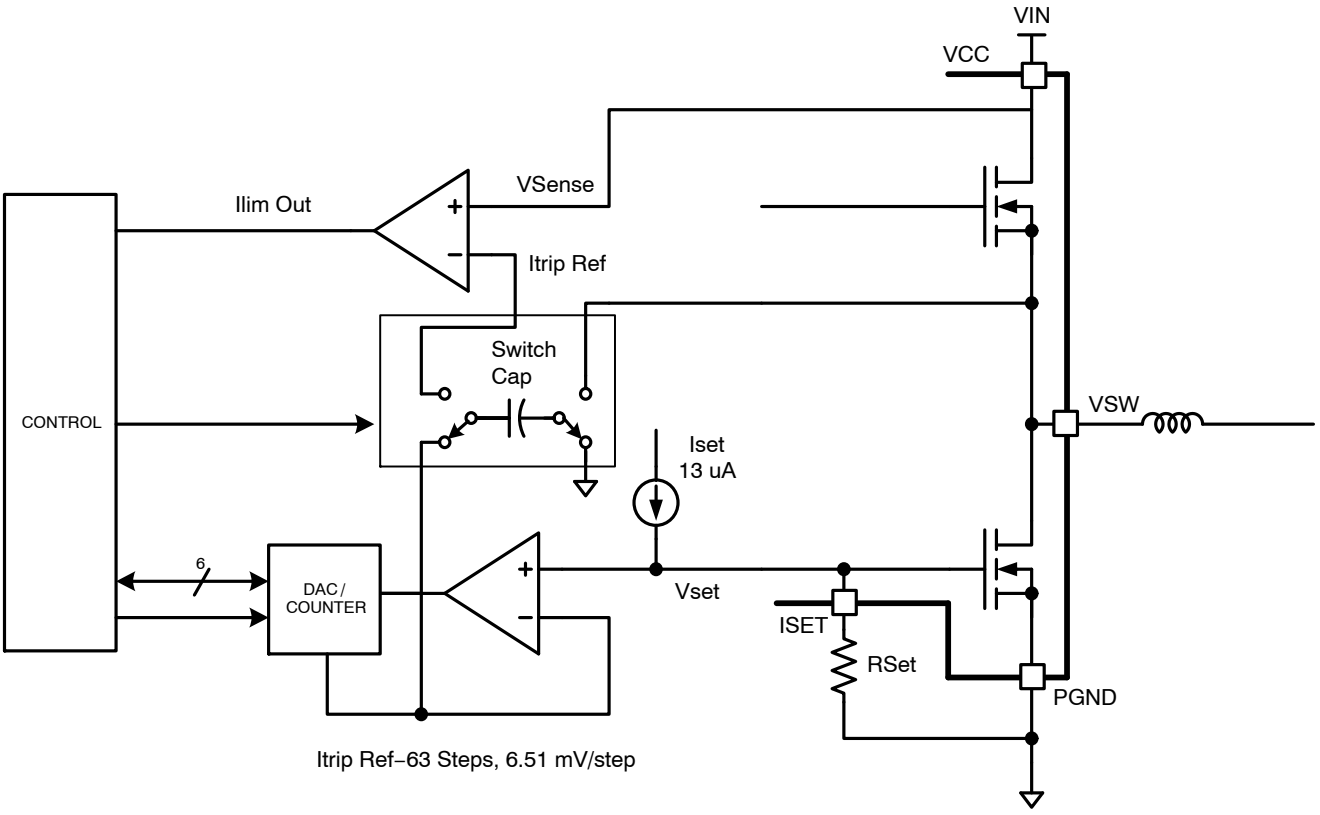


Figure 35. I_{set} / I_{Limit} Block Diagram

Current Limit Set

The I_{Limit} comparator reference is set during the startup sequence by forcing a typically 13 μA current through the low side gate drive resistor. The gate drive output will rise to a voltage level shown in the equation below:

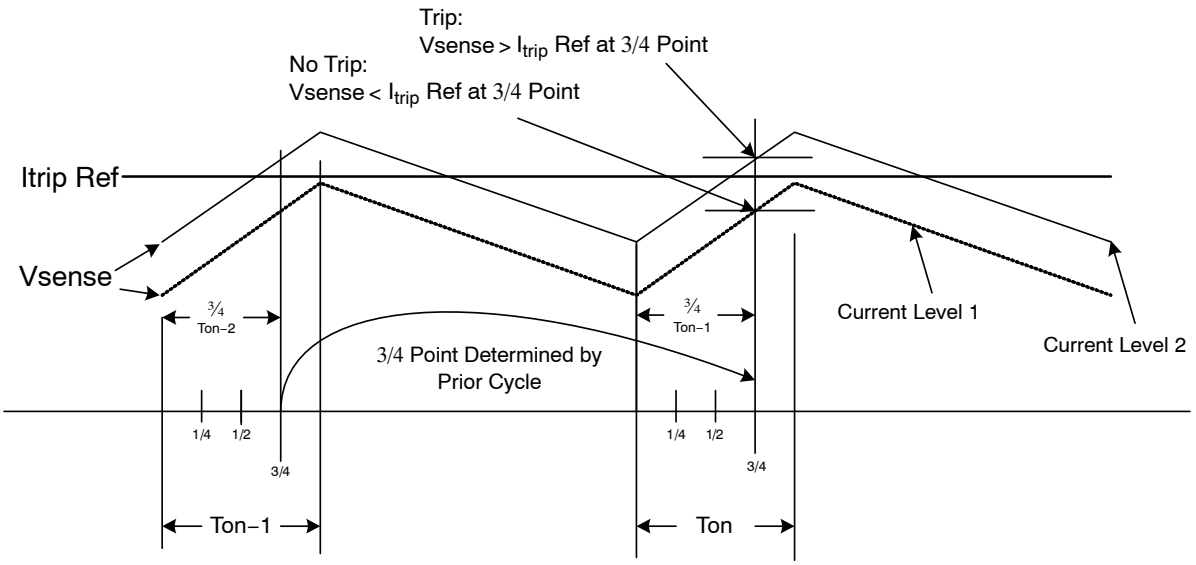
$$V_{set} = I_{set} * R_{set} \qquad \text{(eq. 1)}$$

Where I_{SET} is 13 μA and R_{SET} is the gate to source resistor on the low side MOSFET.

This resistor is normally installed to prevent MOSFET leakage from causing unwanted turn on of the low side MOSFET. In this case, the resistor is also used to set the I_{Limit} trip level reference through the I_{Limit} DAC. The I_{set} process takes approximately 350 μs to complete prior to Soft−Start stepping. The scaled voltage level across the I_{SET} resistor is converted to a 6 bit digital value and stored as the trip value. The binary I_{Limit} value is scaled and converted to the analog I_{Limit} reference voltage through a DAC counter. The DAC has 63 steps in 6.51 mV increments equating to a maximum sense voltage of 403 mV. During the I_{set} period prior to Soft−Start, the DAC counter increments the reference on the I_{SET} comparator until it crosses the V_{SET} voltage and holds the DAC reference output to that count value. This voltage is translated to the I_{Limit} comparator during the I_{Sense} portion of the switching cycle through the switch cap circuit. See Figure 35. Exceeding the maximum sense voltage results in no current limit. Steps 0 to 10 result in an effective current limit of 0 mV.

Current Sense Cycle

Figure 36 shows how the current is sampled as it relates to the switching cycle. Current level 1 in Figure 36 represents a condition that will not cause a fault. Current level 2 represents a condition that will cause a fault. The sense circuit is allowed to operate below the 3/4 point of a given switching cycle. A given switching cycle's 3/4 T_{on} time is defined by the prior cycle's T_{on} and is quantized in 10 ns steps. A fault occurs if the sensed MOSFET voltage exceeds the DAC reference within the 3/4 time window of the switching cycle.



Each switching cycle's Ton is counted in 10 nS time steps. The 3/4 sample time value is held and used for the following cycle's limit sample time

Figure 36. I_{Limit} Trip Point Description

Soft−Start Current limit

During soft−start the I_{SET} value is doubled to allow for inrush current to charge the output capacitance. The DAC reference is set back to its normal value after soft−start has completed.

V_{SW} Ringing

The I_{Limit} block can lose accuracy if there is excessive V_{SW} voltage ringing that extends beyond the 1/2 point of the high−side transistor on−time. Proper snubber design and keeping the ratio of ripple current and load current in the 10−30% range can help alleviate this as well.

Current Limit

A current limit trip results in completion of one switching cycle and subsequently half of another cycle T_{on} to account for negative inductor current that might have caused negative potentials on the output. Subsequently the power MOSFETs are both turned off and a 4 soft−start time period wait passes before another soft−start cycle is attempted.

I_{ave} vs Trip Point

The average load trip current versus R_{SET} value is shown the equation below:

$$I_{AveTRIP} = \frac{I_{set} \times R_{set}}{R_{DS(on)}} - \frac{1}{4}\left[\frac{V_{IN} - V_{OUT}}{L} \times \frac{V_{OUT}}{V_{IN}} \times \frac{1}{F_{SW}}\right] \quad \text{(eq. 2)}$$

Where:
L = Inductance (H)
I_{SET} = 13 μA
R_{SET} = Gate to Source Resistance (Ω)
$R_{DS(on)}$ = On Resistance of the HS MOSFET (48 mΩ)
V_{IN} = Input Voltage (V)
V_{OUT} = Output Voltage (V)
F_{SW} = Switching Frequency (Hz)

Boost Clamp Functionality

The boost circuit requires an external capacitor connected between the BST and V_{SW} pins to store charge for supplying the high and low−side gate driver voltage. This clamp circuit limits the driver voltage to typically 7.5 V when V_{IN} > 9 V, otherwise this internal regulator is in dropout and typically V_{IN} − 1.25 V.

The boost circuit regulates the gate driver output voltage and acts as a switching diode. A simplified diagram of the boost circuit is shown in Figure 37. While the switch node is grounded, the sampling circuit samples the voltage at the boost pin, and regulates the boost capacitor voltage. The sampling circuit stores the boost voltage while the V_{SW} is high and the linear regulator output transistor is reversed biased.

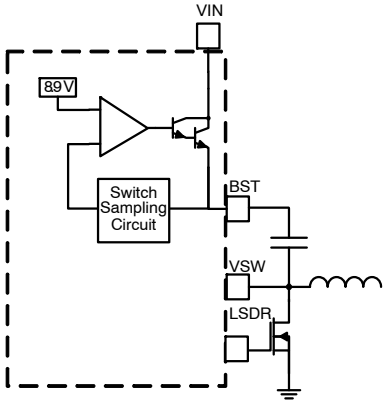


Figure 37. Boost Circuit

Reduced sampling time occurs at high duty cycles where the low side MOSFET is off for the majority of the switching period. Reduced sampling time causes errors in the regulated voltage on the boost pin. High duty cycle / input voltage induced sampling errors can result in increased boost ripple voltage or higher than desired DC boost voltage. Figure 38 outlines all operating regions.

The recommended operating conditions are shown in Region 1 (Green) where a 0.1 μF, 25 V ceramic capacitor can be placed on the boost pin without causing damage to the device or MOSFETS. Larger boost ripple voltage occurring over several switching cycles is shown in Region 2 (Yellow). The boost ripple frequency is dependent on the output capacitance selected. The ripple voltage will not damage the device or ±12 V gate rated MOSFETs.

Conditions where maximum boost ripple voltage could damage the device or ±12 V gate rated MOSFETs can be seen in Region 3 (Orange). Placing a boost capacitor that is no greater than 3.3 nF on the boost pin limits the maximum boost voltage < 12 V. The typical drive waveforms for Regions 1, 2 and 3 (green, yellow, and orange) regions of Figure 38 are shown in Figure 39.

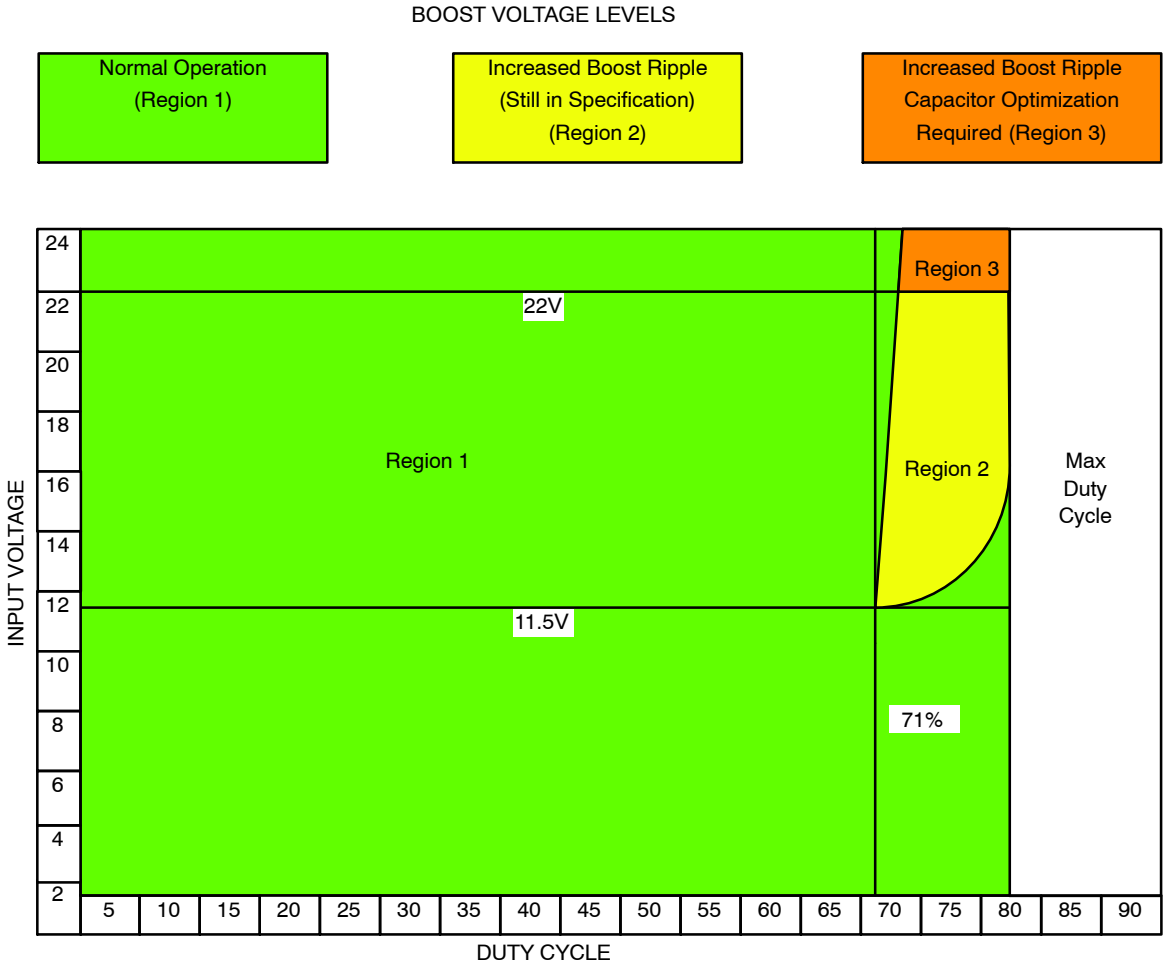


Figure 38. Safe Operating Area for Boost Voltage with a 0.1 μF Capacitor

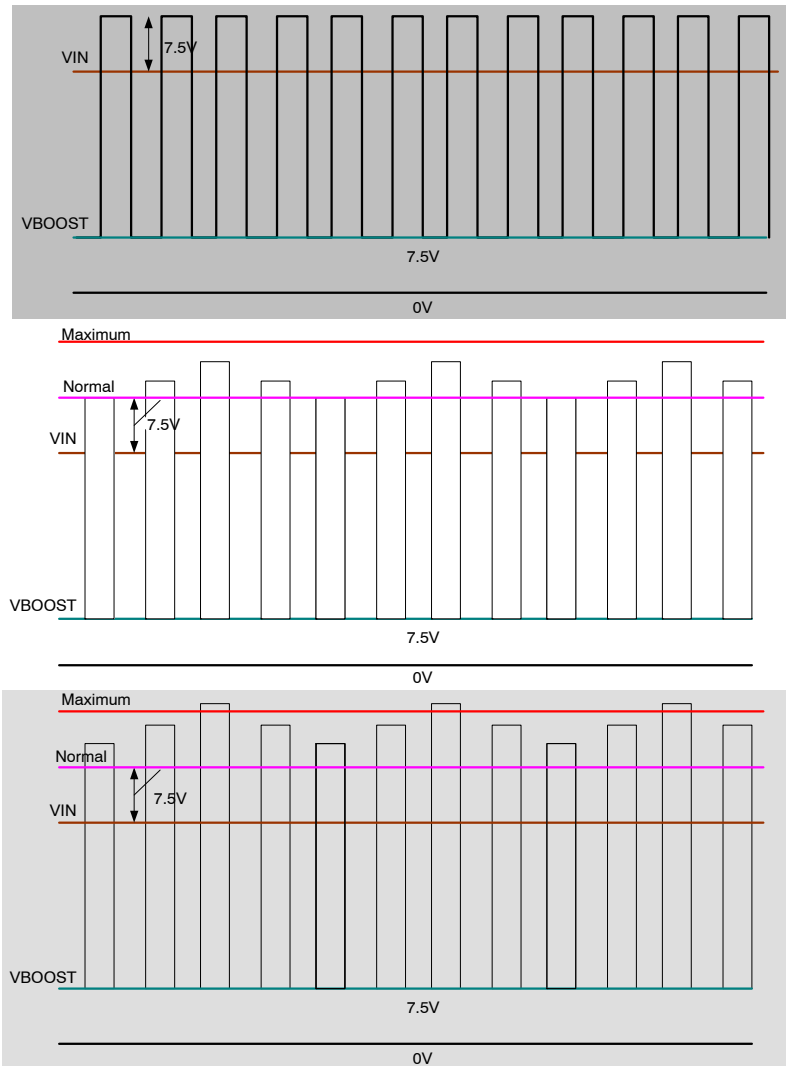


Figure 39. Typical Waveforms for Region 1 (top), Region 2 (middle), and Region 3 (bottom)

To illustrate, a 0.1 μF boost capacitor operating at > 80% duty cycle and > 22.5 V input voltage will exceed the specifications for the driver supply voltage. See Figure 40.

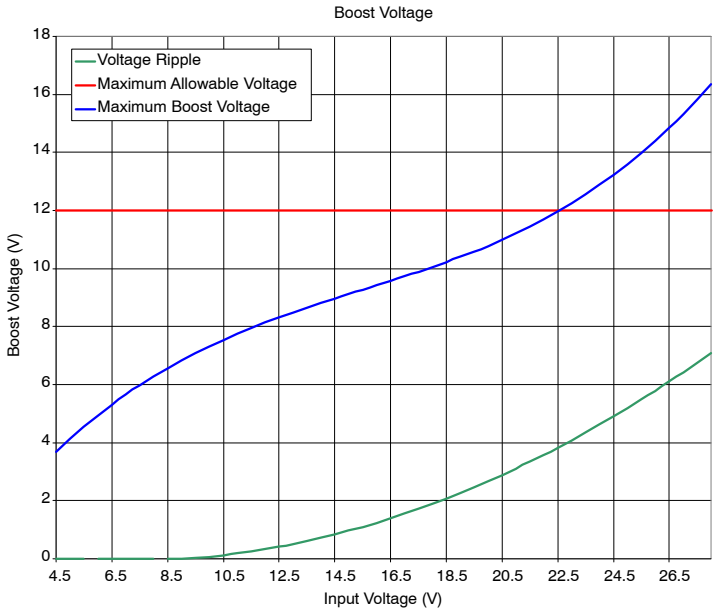


Figure 40. Boost Voltage at 80% Duty Cycle

Inductor Selection

When selecting the inductor, it is important to know the input and output requirements. Some example conditions are listed below to assist in the process.

Table 1. DESIGN PARAMETERS

Design Parameter		Example Value
Input Voltage	(V_{IN})	9 V to 16 V
Nominal Input Voltage	(V_{IN})	12 V
Output Voltage	(V_{OUT})	3.3 V
Input ripple voltage	(VIN_{RIPPLE})	300 mV
Output ripple voltage	($VOUT_{RIPPLE}$)	50 mV
Output current rating	(I_{OUT})	3 A
Operating frequency	(Fsw)	500 kHz

A buck converter produces input voltage (V_{IN}) pulses that are LC filtered to produce a lower dc output voltage (V_{OUT}). The output voltage can be changed by modifying the on time relative to the switching period (T) or switching frequency. The ratio of high side switch on time to the switching period is called duty cycle (D). Duty cycle can also be calculated using V_{OUT}, V_{IN}, the low side switch voltage drop V_{LSD}, and the High side switch voltage drop V_{HSD}.

$$F = \frac{1}{T} \qquad \text{(eq. 3)}$$

$$D = \frac{T_{ON}}{T}(-D) = \frac{T_{OFF}}{T} \qquad \text{(eq. 4)}$$

$$D = \frac{V_{OUT} + V_{LSD}}{V_{IN} - V_{HSD} + V_{LSD}} \approx D = \frac{V_{OUT}}{V_{IN}} \qquad \text{(eq. 5)}$$

$$\rightarrow 27.5\% = \frac{3.3\ V}{12\ V}$$

The ratio of ripple current to maximum output current simplifies the equations used for inductor selection. The formula for this is given in Equation 6.

$$ra = \frac{\Delta I}{I_{OUT}} \qquad \text{(eq. 6)}$$

The designer should employ a rule of thumb where the percentage of ripple current in the inductor lies between 10% and 40%. When using ceramic output capacitors the ripple current can be greater thus a user might select a higher ripple current, but when using electrolytic capacitors a lower ripple current will result in lower output ripple. Now, acceptable values of inductance for a design can be calculated using Equation 7.

$$L = \frac{V_{OUT}}{I_{OUT} \cdot ra \cdot F_{SW}} \cdot (1 - D) \rightarrow 8.2\ \mu H \qquad \text{(eq. 7)}$$

$$= \frac{3.3\ V}{3\ A \cdot 20\% \cdot 500\ kHz} \cdot (1 - 27.5\%)$$

The relationship between ra and L for this design example is shown in Figure 41.

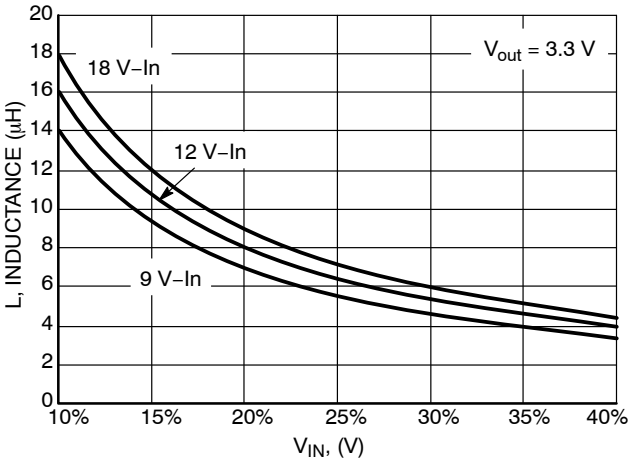


Figure 41. Ripple Current Ratio vs. Inductance

To keep within the bounds of the parts maximum rating, calculate the RMS current and peak current.

$$I_{RMS} = I_{OUT} \cdot \sqrt{1 + \frac{ra^2}{12}} \rightarrow 3.01\ A = 3\ A \cdot \sqrt{1 + \frac{(0.2)^2}{12}} \quad \text{(eq. 8)}$$

$$I_{PK} = I_{OUT} \cdot \left(1 + \frac{ra}{2}\right) \rightarrow 3.3\ A = 3\ A \cdot \left(1 + \frac{(0.2)}{2}\right) \quad \text{(eq. 9)}$$

An inductor for this example would be around 8.2 μH and should support an rms current of 3.01 A and a peak current of 3.3 A.

The final selection of an output inductor has both mechanical and electrical considerations. From a mechanical perspective, smaller inductor values generally correspond to smaller physical size. Since the inductor is often one of the largest components in the regulation system, a minimum inductor value is particularly important in space−constrained applications. From an electrical perspective, the maximum current slew rate through the output inductor for a buck regulator is given by Equation 10.

$$SlewRate_{LOUT} = \frac{V_{IN} - V_{OUT}}{L_{OUT}} \rightarrow 1.1\frac{A}{\mu s} = \frac{12\ V - 3.3\ V}{8.2\ \mu H} \quad \text{(eq. 10)}$$

This equation implies that larger inductor values limit the regulator's ability to slew current through the output inductor in response to output load transients. Consequently, output capacitors must supply the load current until the inductor current reaches the output load current level. This results in larger values of output capacitance to maintain tight output voltage regulation. In contrast, smaller values of inductance increase the regulator's maximum achievable slew rate and decrease the necessary capacitance, at the expense of higher ripple current. The peak−to−peak ripple current for the NCP3155A is given by the following equation:

$$I_{PP} = \frac{V_{OUT}(1 - D)}{L_{OUT} \cdot F_{SW}} \quad \text{(eq. 11)}$$

Ipp is the peak to peak current of the inductor. From this equation it is clear that the ripple current increases as L_{OUT} decreases, emphasizing the trade−off between dynamic response and ripple current.

The power dissipation of an inductor consists of both copper and core losses. The copper losses can be further categorized into dc losses and ac losses. A good first order approximation of the inductor losses can be made using the DC resistance as they usually contribute to 90% of the losses of the inductor shown below:

$$LP_{CU} = I_{RMS}^{\ 2} \cdot DCR \quad \text{(eq. 12)}$$

The core losses and ac copper losses will depend on the geometry of the selected core, core material, and wire used. Most vendors will provide the appropriate information to make accurate calculations of the power dissipation then the total inductor losses can be capture buy the equation below:

$$LP_{tot} = LP_{CU\_DC} + LP_{CU\_AC} + LP_{Core} \quad \text{(eq. 13)}$$

Input Capacitor Selection

The input capacitor has to sustain the ripple current produced during the on time of the upper MOSFET, so it must have a low ESR to minimize the losses. The RMS value of this ripple is:

$$Iin_{RMS} = I_{OUT} \cdot \sqrt{D \cdot (1 - D)} \quad \text{(eq. 14)}$$

D is the duty cycle, Iin_{RMS} is the input RMS current, and I_{OUT} is the load current.

The equation reaches its maximum value with D = 0.5. Loss in the input capacitors can be calculated with the following equation:

$$P_{CIN} = ESR_{CIN} \cdot \left(I_{IN-RMS}\right)^2 \quad \text{(eq. 15)}$$

P_{CIN} is the power loss in the input capacitors and ESR_{CIN} is the effective series resistance of the input capacitance. Due to large dI/dt through the input capacitors, electrolytic or ceramics should be used. If a tantalum must be used, it must by surge protected. Otherwise, capacitor failure could occur.

Input Start−up Current

To calculate the input startup current, the following equation can be used.

$$I_{INRUSH} = \frac{C_{OUT} \cdot V_{OUT}}{t_{SS}} \quad \text{(eq. 16)}$$

I_{inrush} is the input current during startup, C_{OUT} is the total output capacitance, V_{OUT} is the desired output voltage, and t_{SS} is the soft start interval. If the inrush current is higher than the steady state input current during max load, then the input fuse should be rated accordingly, if one is used.

Output Capacitor Selection

The important factors to consider when selecting an output capacitor is dc voltage rating, ripple current rating, output ripple voltage requirements, and transient response requirements.

The output capacitor must be rated to handle the ripple current at full load with proper derating. The RMS ratings given in datasheets are generally for lower switching frequency than used in switch mode power supplies but a multiplier is usually given for higher frequency operation. The RMS current for the output capacitor can be calculated below:

$$Co_{RMS} = I_O \cdot \frac{ra}{\sqrt{12}} \quad \text{(eq. 17)}$$

The maximum allowable output voltage ripple is a combination of the ripple current selected, the output capacitance selected, the equivalent series inductance (ESL) and ESR.

The main component of the ripple voltage is usually due to the ESR of the output capacitor and the capacitance selected.

$$V_{ESR\_C} = I_O \cdot ra \cdot \left(ESR_{Co} + \frac{1}{8 \cdot F_{SW} \cdot Co} \right) \quad \text{(eq. 18)}$$

The ESL of capacitors depends on the technology chosen but tends to range from 1 nH to 20 nH where ceramic capacitors have the lowest inductance and electrolytic capacitors then to have the highest. The calculated contributing voltage ripple from ESL is shown for the switch on and switch off below:

$$V_{ESLON} = \frac{ESL \cdot I_{PP} \cdot F_{SW}}{D} \quad \text{(eq. 19)}$$

$$V_{ESLOFF} = \frac{ESL \cdot I_{PP} \cdot F_{SW}}{(1 - D)} \quad \text{(eq. 20)}$$

The output capacitor is a basic component for the fast response of the power supply. In fact, during load transient, for the first few microseconds it supplies the current to the load. The controller immediately recognizes the load transient and sets the duty cycle to maximum, but the current slope is limited by the inductor value.

During a load step transient the output voltage initially drops due to the current variation inside the capacitor and the ESR (neglecting the effect of the effective series inductance (ESL)).

$$\Delta V_{OUT-ESR} = \Delta I_{TRAN} \cdot ESR_{Co} \quad \text{(eq. 21)}$$

A minimum capacitor value is required to sustain the current during the load transient without discharging it. The voltage drop due to output capacitor discharge is approximated by the following equation:

$$\Delta V_{OUT-DISCHG} = \frac{(I_{TRAN})^2 \cdot L_{OUT}}{C_{OUT} \cdot (V_{IN} - V_{OUT})} \quad \text{(eq. 22)}$$

In a typical converter design, the ESR of the output capacitor bank dominates the transient response. It should be noted that ΔVOUT−DISCHARGE and ΔVOUT−ESR are out of phase with each other, and the larger of these two voltages will determine the maximum deviation of the output voltage (neglecting the effect of the ESL).

Conversely during a load release, the output voltage can increase as the energy stored in the inductor dumps into the output capacitor. The ESR contribution from Equation 18 still applies in addition to the output capacitor charge which is approximated by the following equation:

$$\Delta V_{OUT-CHG} = \frac{(I_{TRAN})^2 \cdot L_{OUT}}{C_{OUT} \cdot V_{OUT}} \quad \text{(eq. 23)}$$

As with any power design, proper laboratory testing should be performed to insure the design will dissipate the required power under worst case operating conditions. Variables considered during testing should include maximum ambient temperature, minimum airflow, maximum input voltage, maximum loading, and component variations.

Feedback and Compensation

The NCP3155 is a voltage mode buck convertor with a transconductance error amplifier compensated by an external compensation network. Compensation is needed to achieve accurate output voltage regulation and fast transient response. The goal of the compensation circuit is to provide a loop gain function with the highest crossing frequency and adequate phase margin (minimally 45°). The transfer function of the power stage (the output LC filter) is a double pole system. The resonance frequency of this filter is expressed as follows:

$$f_{P0} = \frac{1}{2 \cdot \pi \cdot \sqrt{L \cdot C_{OUT}}} \quad \text{(eq. 24)}$$

Parasitic Equivalent Series Resistance (ESR) of the output filter capacitor introduces a high frequency zero to the filter network. Its value can be calculated by using the following equation:

$$f_{Z0} = \frac{1}{2 \cdot \pi \cdot C_{OUT} \cdot ESR} \quad \text{(eq. 25)}$$

The main loop zero crossover frequency f0 can be chosen to be 1/10 − 1/5 of the switching frequency. Table 2 shows the three methods of compensation.

Table 2. COMPENSATION TYPES

Zero Crossover Frequency Condition	Compensation Type	Typical Output Capacitor Type
$f_{P0} < f_{Z0} < f_0 < f_S/2$	Type II	Electrolytic, Tantalum
$f_{P0} < f_0 < f_{Z0} < f_S/2$	Type III Method I	Tantalum, Ceramic
$f_{P0} < f_0 < f_S/2 < f_{Z0}$	Type III Method II	Ceramic

Compensation Type II

This compensation is suitable for electrolytic capacitors. Components of the Type II (Figure 42) network can be specified by the following equations:

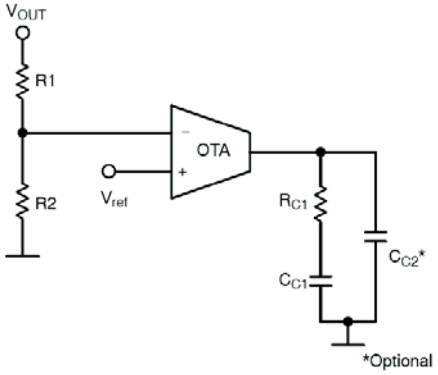


Figure 42. Type II Compensation

$$R_{C1} = \frac{2 \cdot \pi \cdot f_0 \cdot L \cdot V_{RAMP} \cdot V_{OUT}}{ESR \cdot V_{IN} \cdot V_{ref} \cdot gm} \quad \text{(eq. 26)}$$

$$C_{C1} = \frac{1}{0.75 \cdot 2 \cdot \pi \cdot f_{P0} \cdot R_{C1}} \quad \text{(eq. 27)}$$

$$C_{C2} = \frac{1}{\pi \cdot R_{C1} \cdot f_S} \quad \text{(eq. 28)}$$

$$R1 = \frac{V_{OUT} - V_{ref}}{V_{ref}} \cdot R2 \quad \text{(eq. 29)}$$

V_{RAMP} is the peak−to−peak voltage of the oscillator ramp and gm is the transconductance error amplifier gain. Capacitor C_{C2} is optional.

Compensation Type III

Tantalum and ceramics capacitors have lower ESR than electrolytic, so the zero of the output LC filter goes to a higher frequency above the zero crossover frequency. This requires a Type III compensation network as shown in Figure 43.

There are two methods to select the zeros and poles of this compensation network. Method I is ideal for tantalum output capacitors, which have a higher ESR than ceramic:

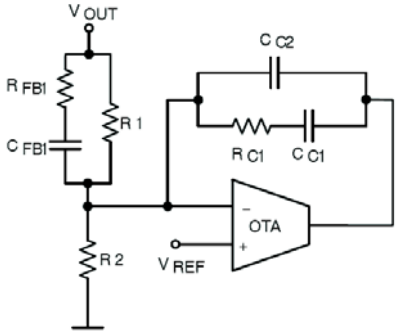


Figure 43. Type III Compensation

$$f_{Z1} = 0.75 \cdot f_{P0} \quad \text{(eq. 30)}$$

$$f_{Z2} = f_{P0} \quad \text{(eq. 31)}$$

$$f_{P2} = f_{Z0} \quad \text{(eq. 32)}$$

$$f_{P3} = \frac{f_S}{2} \quad \text{(eq. 33)}$$

Method II is better suited for ceramic capacitors that typically have the lowest ESR available:

$$f_{Z2} = f_0 \cdot \sqrt{\frac{1 - \sin\theta\,max}{1 + \sin\theta\,max}} \quad \text{(eq. 34)}$$

$$f_{P2} = f_0 \cdot \sqrt{\frac{1 + \sin\theta\,max}{1 - \sin\theta\,max}} \quad \text{(eq. 35)}$$

$$f_{Z1} = 0.5 \cdot f_{Z2} \quad \text{(eq. 36)}$$

$$f_{P3} = 0.5 \cdot f_S \quad \text{(eq. 37)}$$

θmax is the desired maximum phase margin at the zero crossover frequency, f_0. It should be 45° − 75°. Convert degrees to radians by the formula:

$$\theta\,max = \theta\,max_{degress} \cdot \left(\frac{2 \cdot \pi}{360}\right) : Units = radians \quad \text{(eq. 38)}$$

The remaining calculations are the same for both methods.

$$R_{C1} >> \frac{2}{gm} \quad \text{(eq. 39)}$$

$$C_{C1} = \frac{1}{2 \cdot \pi \cdot f_{Z1} \cdot R_{C1}} \quad \text{(eq. 40)}$$

$$C_{C2} = \frac{1}{2 \cdot \pi \cdot f_{P3} \cdot R_{C1}} \quad \text{(eq. 41)}$$

$$C_{FB1} = \frac{2 \cdot \pi \cdot f_0 \cdot L \cdot V_{RAMP} \cdot C_{OUT}}{V_{IN} \cdot R_{C1}} \quad \text{(eq. 42)}$$

$$R_{FB1} = \frac{1}{2\pi \cdot C_{FB1} \cdot f_{P2}} \quad \text{(eq. 43)}$$

$$R1 = \frac{1}{2 \cdot \pi \cdot C_{FB1} \cdot f_{Z2}} - R_{FB1} \quad \text{(eq. 44)}$$

$$R2 = \frac{V_{ref}}{V_{OUT} - V_{ref}} \cdot R1 \quad \text{(eq. 45)}$$

If the equation in Equation 46 is not true, then a higher value of R_{C1} must be selected.

$$\frac{R1 \cdot R2 \cdot R_{FB1}}{R1 \cdot R_{FB1} + R2 \cdot R_{FB1} + R1 \cdot R2} > \frac{1}{gm} \quad \text{(eq. 46)}$$

Output Current Derating

The NCP3155 has a wide input voltage and output voltage capability. It also operates in a variety of thermal environments. These thermal conditions limit the maximum output current for a given input and output voltage. Therefore, proper output current derating must be considered, taking into account ambient temperature, airflow, the input and output conditions, and the need for increased reliability. Figures 24 – 29 show safe operating conditions vs. output current for input voltages of 12 V, 18 V, and 24 V. These curves assumed 300 mm^2 of 2 oz copper. Sufficient cooling could also be provided to ensure reliable operation. Finally, to maintain operation in the safe operating areas shown in the curves, it is recommended to use the NCP3155 with input to output conditions as shown in Figure 44.

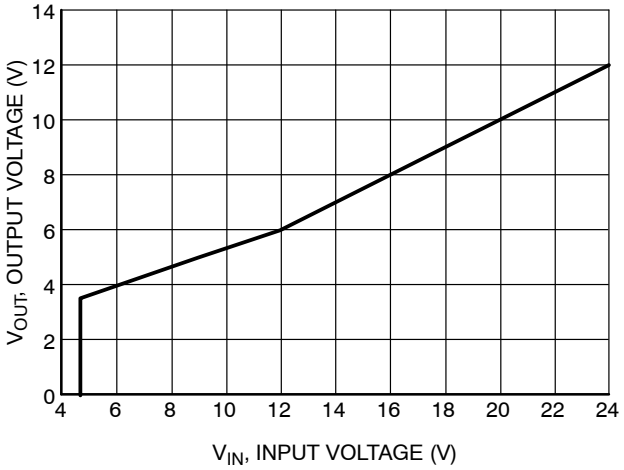
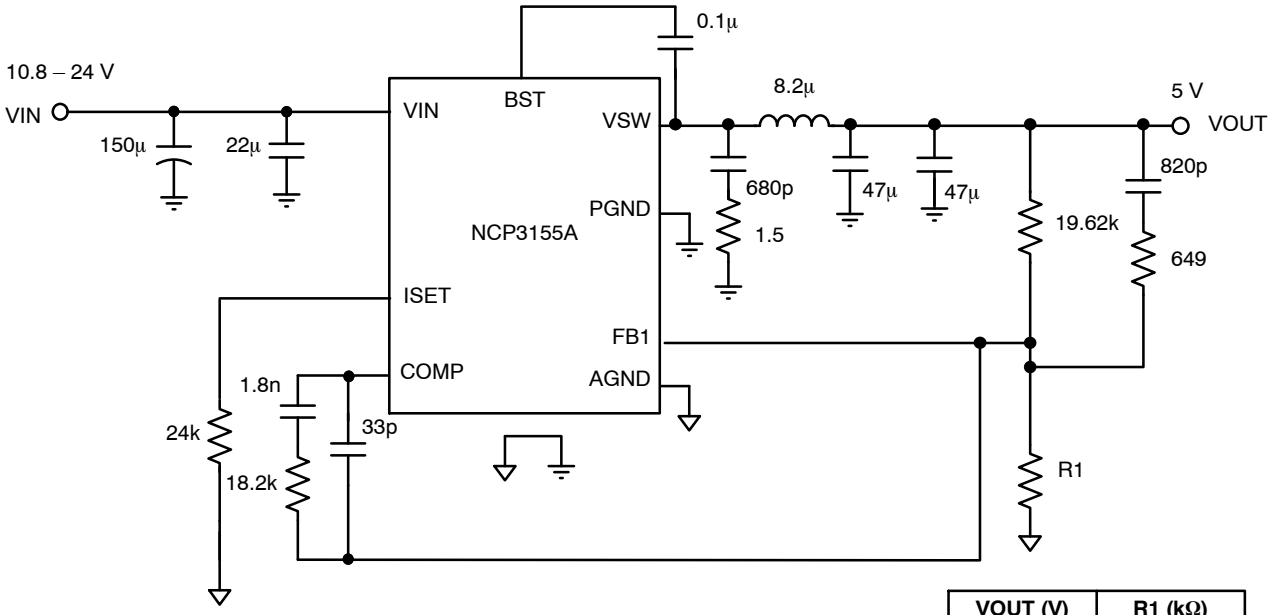


Figure 44. Recommended Maximum Output Voltage vs Input Voltage



VOUT (V)	R1 (kΩ)
1.2	39.2k
1.5	22.1k
3.3	6.19k
5.0	3.74k

Figure 45. Typical Application Circuit

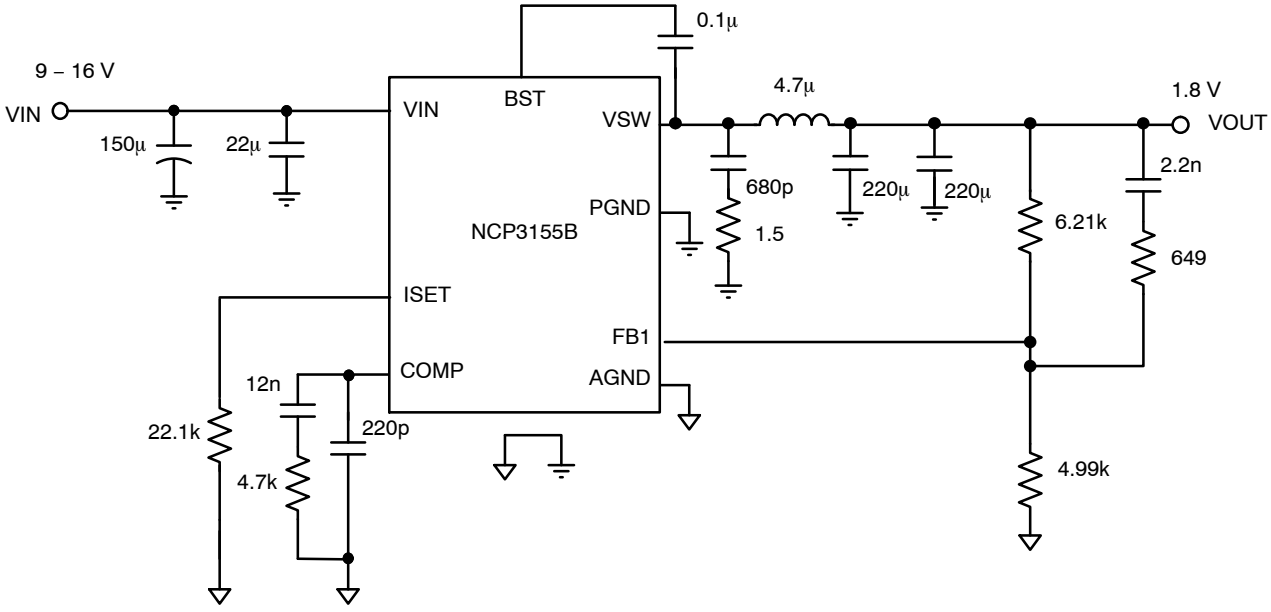


Figure 46. Typical Application Circuit

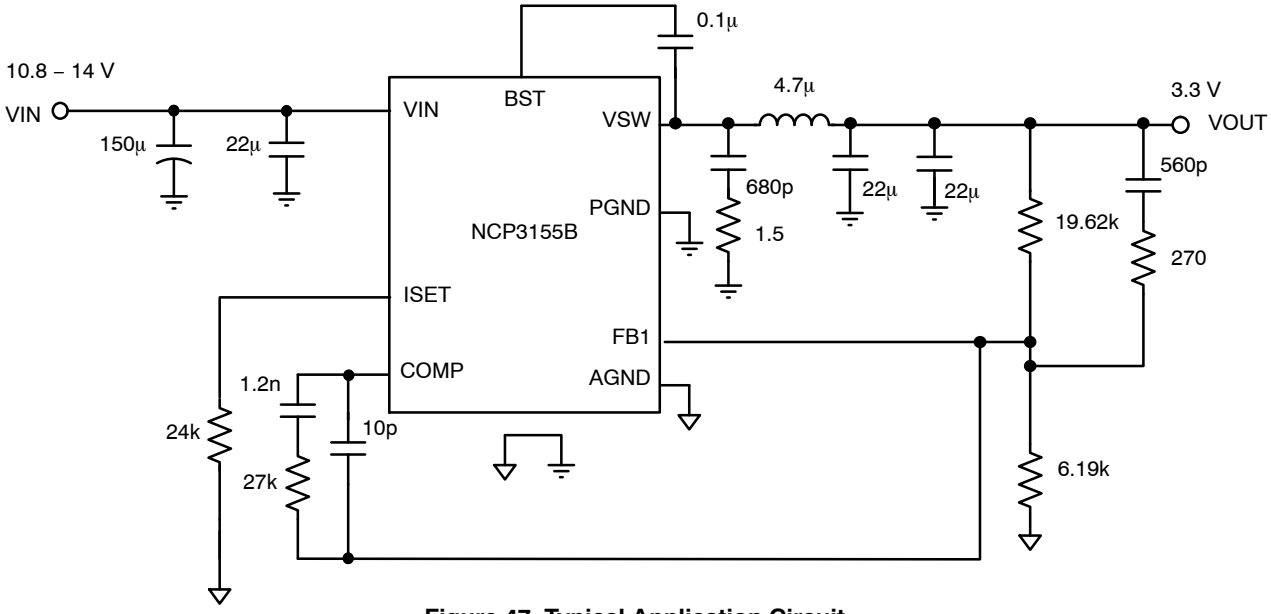


Figure 47. Typical Application Circuit

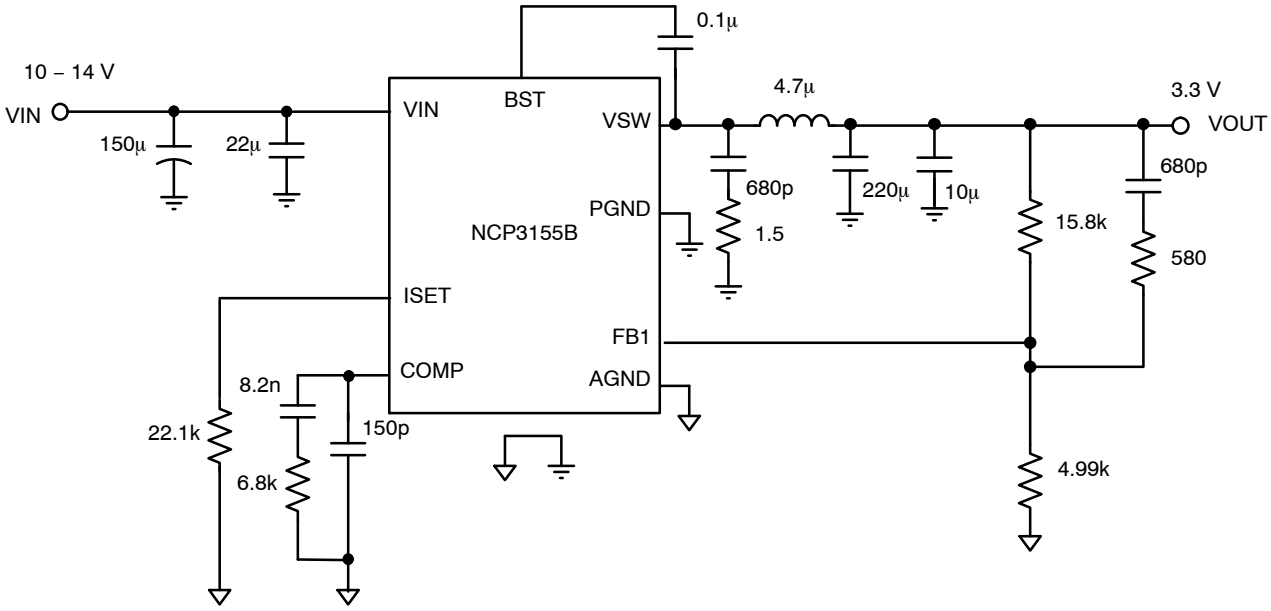


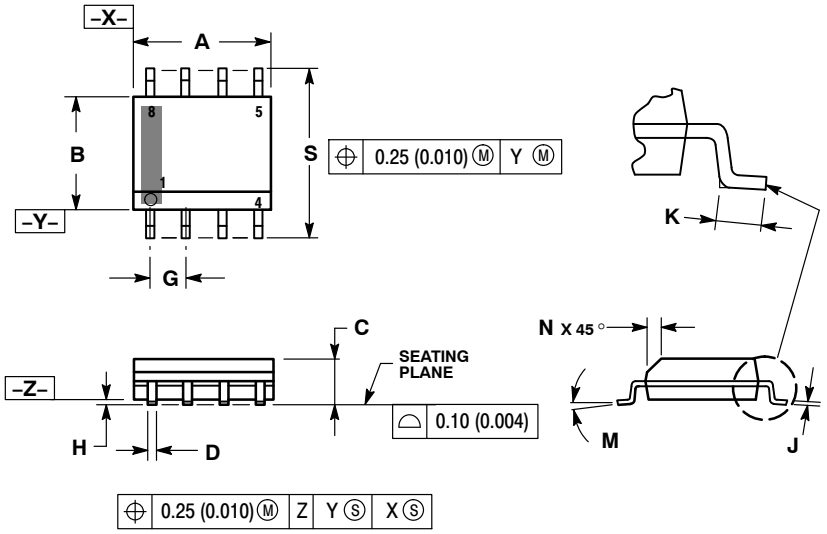
Figure 48. Typical Application Circuit

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AK

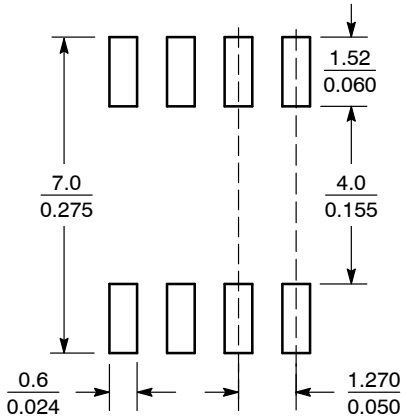
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

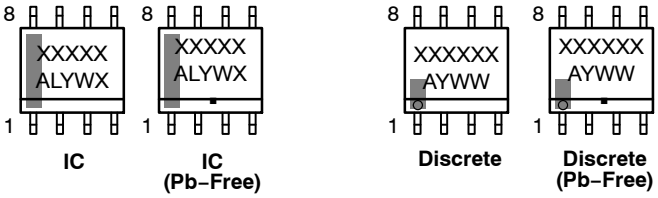
SOLDERING FOOTPRINT*



SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



IC | IC (Pb−Free) | Discrete | Discrete (Pb−Free)

XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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DESCRIPTION:	**SOIC−8 NB**	**PAGE 1 OF 2**

SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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