Released Data Sheet - Confidential

80-36-08400• Rev 1.01• October 2017

SanDisk iNAND® *7550*

e.MMC 5.1 with Command-Queue and HS400 Interface

REVISION HISTORY

Doc. No	Revision	Date	Description
80-36-08400	1.0	17-Sep-2017	Initial version
80-36-08400	1.0.1	26-Oct-2017	DR & Write Endurance spec updates in Reliability section Ordering information update

SanDisk® general policy does not recommend the use of its products in life support applications where in a failure or malfunction of the product may directly threaten life or injury. Per SanDisk® Terms and Conditions of Sale, the user of SanDisk® products in life support applications assumes all risk of such use and indemnifies SanDisk® against all damages. See "Disclaimer of Liability."

This document is for information use only and is subject to change without prior notice. SanDisk® assumes no responsibility for any errors that may appear in this document, nor for incidental or consequential damages resulting from the furnishing, performance or use of this material. No part of this document may be reproduced, transmitted, transcribed, stored in a retrievable manner or translated into any language or computer language, in any form or by any means, electronic, mechanical, magnetic, optical, chemical, manual or otherwise, without the prior written consent of an officer of SanDisk®.

TABLE OF CONTENTS

1. INTRODUCTION

1.1. General Description

Overview SanDisk iNAND 7550 is an Embedded Flash Drive (EFD) for boosting the overall performance of existing flash-based product lines like smartphones, tablets, automotive and infotainment systems as well as enabling manufacturers to bring the benefits of flash (rapid boot-up, high reliability, robustness, consistent performance) to new markets such as entry-level notebooks.

Providing up to 256GB of capacity and technology for features such as low-power consumption, the iNAND 7550 is the ideal choice to deliver amazing performance for storage-hungry applications like imaging, video, music, GPS, gaming, email, office and other applications on 4G smartphones, embedded systems or other devices.

The design of the iNAND 7550 is based on JEDEC compatible form factors to lower integration costs and accelerate time-to-market.

Architecture iNAND 7550 combines an embedded thin flash controller with advanced Triple-Level Cell (TLC) NAND flash technology enhanced by SanDisk's embedded flash management software running as firmware on the flash controller. iNAND 7550 employs an industry-standard eMMC 5.1[1] interface featuring Command-Queue, HS400, FFU, as well as legacy eMMC 4.51 features such as Power Off Notifications, Packed commands, Cache, Boot / RPMB partitions, HPI, and HW Reset, make it an optimal device for both reliable code and data storage.

Technology iNAND 7550 is based on SanDisk 256Gb X3 3D NAND memory, using 64-layer technology. The memory architecture brings new levels of density, scalability and performance to the Embedded Flash Drive. SanDisk 3D NAND memory also provides enhanced write/erase endurance, write speeds and energy efficiency relative to conventional 2D NAND

iNAND 7550 architecture and embedded firmware fully emulates a hard disk to the host processor, enabling read/write operations that are identical to a standard, sector-based hard drive. In addition, SanDisk firmware employs patented methods, such as virtual mapping, dynamic and static wear-leveling, and automatic block management to ensure high data reliability and maximizing flash life expectancy.

iNAND 7550 also includes an intelligent controller, which manages interface protocols, data storage and retrieval, error correction code (ECC) algorithms, defect handling and diagnostics, power management and clock control.

Combining high performance with features for easy integration and exceptional reliability, iNAND 7550 is an EFD designed to exceed the demands of both manufacturers and their customers.

1.2. Plug-and-Play Integration

iNAND's optimized architecture eliminates the need for complicated software integration and testing processes thereby enabling plug-and-play integration into the host system. The

[1] Compatible to JESD84-B51

replacement of one iNAND device with another, of a newer generation, requires virtually no changes to the host. This allows manufacturers to adopt advanced NAND Flash technologies and update product lines with minimal integration or qualification efforts.

With JEDEC form factors measuring 11.5x13mm (153 balls) for all capacities, iNAND 7550 is ideally suited for a wide variety of portable devices such as multimedia mobile handsets, tablets, and automotive infotainment.

iNAND 7550 features a MMC interface allows easy integration regardless of the host (chipset) type used. All device and interface configuration data (such as maximum frequency and device identification) are stored on the device.

Figure 1 shows a block diagram of the SanDisk iNAND 7550 with MMC Interface.

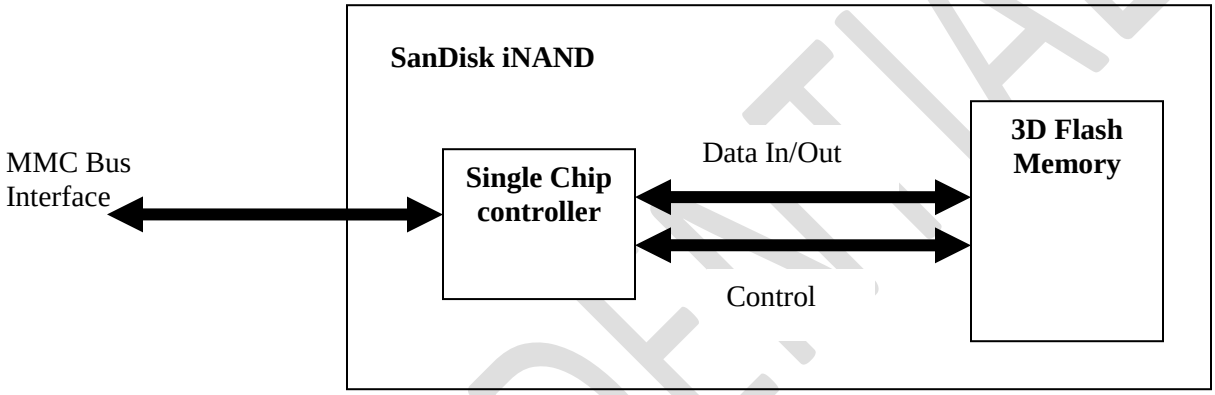


Figure 1 - SanDisk iNAND 7550 with MMC Interface Block Diagram

1.3. Feature Overview

SanDisk iNAND 7550, with MMC interface, includes the following features:

- Memory controller and NAND flash
- Mechanical design complies with JEDEC Specification
- Offered in three TFBGA packages of eMMC 5.1[2]
  - 11.5mm x 13mm x 1.0mm (32GB-256GB)
- Operating temperature range: –25C° to +85C°
- Dual power system
- Core voltage (VCC) 2.7-3.6 V
- I/O (VCCQ) voltage, either: 1.7-1.95V or 2.7-3.6V
  - Note: Device operation under 3.3V VCCQ is limited to Max 1 hour
- Up to 256GB of data storage
- Supports three data bus widths: 1bit (default), 4bit, 8bit
- Complies with eMMC Specification Ver. 5.1 HS400
- Variable clock frequencies of 0-20 MHz, 0-26 MHz (default), 0-52 MHz (high-speed), 0-200 MHz SDR (HS200), 0-200 MHz DDR (HS400)
- Up to 400 MB/sec bus transfer rate, using 8 parallel data lines at 400 MHz, HS400 Mode
- Correction of memory field errors
- Designed for portable and stationary applications that require high performance and reliable data storage
- RPMB Key Reset

max 1 hours? what is this mean?

1.4. Defect and Error Management

The SanDisk iNAND 7550 contains a sophisticated defect and error management system for exceptional data reliability. iNAND 7550 will rewrite data from a defective sector to a good sector. This is completely transparent to the host and does not consume additional user data space. In the extremely rare case that a read error does occur, iNAND has innovative algorithms to recover the data.

1.5. MMC bus and Power Lines

SanDisk iNAND 7550 with MMC interface supports the MMC protocol. For more details regarding these buses refer to JEDEC standards No. JESD84-B51.

The iNAND bus has the following communication and power lines:

[2] Refer to JEDEC Standards No. JESD84-B51

- CMD: Command is a bidirectional signal. The host and iNAND operate in two modes, open drain and push-pull.
- DAT0-7: Data lines are bidirectional signals. Host and iNAND operate in push-pull mode.
- CLK: Clock input.
- RST_n: Hardware Reset Input.
- VCCQ: VCCQ is the power supply line for host interface.
- VCC: VCC is the power supply line for internal flash memory.
- VDDi: VDDi is iNAND's internal power node, not the power supply. Connect 0.1uF capacitor from VDDi to ground.
- VSS, VSSQ: Ground lines.
- RCLK: Data strobe.
- VSF: Vendor specific functions used for debugging purposes.

1.5.1. Bus operating conditions

Table 1 - Bus operating conditions

Parameter	Min	Max	Unit
Peak voltage on all lines	-0.5	VCCQ+0.5	V
Input Leakage Current (before initializing and/or connecting the internal pull-up resistors)	-100	100	µA
Input Leakage Current (after changing the bus width and disconnecting the internal pull-up resistors)	-2	2	µA
Output Leakage Current (before initializing and/or connecting the internal pull-up resistors)	-100	100	µA
Output Leakage Current (after changing the bus width and disconnecting the internal pull-up resistors)	-2	2	µA

Table 2 – Power supply voltage

Parameter	Symbol	Min	Max	Unit
Supply Voltage	VCCQ (Low)	1.7	1.95	V
	VCCQ (High)	2.7	3.6	V
	VCC	2.7	3.6	V
	VSS-VSSQ	-0.3	0.3	V

Note1: HS200, HS400 modes support only the 1.7 – 1.95 V VCCQ option

Note2: Device operation under 3.3V VCCQ is limited to Max 1 hour

2. E.MMC 5.1 SELECTED FEATURES OVERVIEW

iNAND 7550 supported feature list:

e.MMC	Device Features	Benefit	Support
N/A	INTERFACE	Speed	HS400
N/A	BUS SPEED	Max theoretical Speed	Up to 400MB/s
4.41	SECURE ERASE/TRIM	"True Wipe"	Yes
4.41	BOOT AND MASS STORAGE	One storage device (reduced BOM)	Yes
4.41	PARTITIONING & PROTECTION	Flexibility	Yes
4.41	BACKGROUND OPERATIONS	Better User Experience (low latency)	Yes
4.41	POWER OFF NOTIFICATION	Faster Boot; Responsiveness	Yes
4.41	HARDWARE RESET	Robust System Design	Yes
4.41	HPI	Control Long Reads/Writes	Yes
4.41	RPMB	Secure Folders	Yes
4.5	EXTENDED PARTITION ATTRIBUTE	Flexibility	Yes
4.5	LARGE SECTOR SIZE	Potential performance	No
4.5	SANITIZE (4.51)	"True Wipe"	Yes
4.5	PACKED COMMANDS	Reduce Host Overhead	Yes
4.5	DISCARD	Improved Performance on Full Media	Yes
4.5	DATA TAG	Performance and/or Reliability	Yes (API only)
4.5	CONTEXT MANAGEMENT	Performance and/or Reliability	Yes (API only)
4.5	CACHE	Better Sequential & Random Writes	Yes
5.0	FIELD FIRMWARE UPGRADE (FFU)	Enables feature enhancements in the field	Yes
5.0	PRODUCTION STATE AWARENESS	Different operation during production	Yes
5.0	DEVICE HEALTH	Vital NAND info	Yes
5.1	ENHANCE STROBE	Sync between Device and Host in HS400	Yes
5.1	COMMAND QUEUE	Responsiveness	Yes
5.1	RPMB THROUGHPUT	Faster RPMB write throughput	Yes
5.1	CACHE FLUSH AND BARRIER	Ordered Cache flushing	Yes
5.1	BKOPS CONTROLLER	Host control on BKOPs	Yes
5.1	SECURE WP	Secure Write Protect	Yes
5.2	HS400 TUNING	DLL Tuning command in HS400	Yes
Propriety	SMART-SLC	Fast write speed per application need	Yes
Propriety	VSF	Enable on-board debugging	Yes
Propriety	PNM	Special product name	Yes
Propriety	DEVICE REPORT	Device Firmware status	Yes
Propriety	CONTENT-PRELOADING	Preloading content at production line	Yes
Propriety	RPMB-KEY-RESET	Resetting RPMB partition key	Yes

2.1. Field Firmware Upgrade (FFU)

Field Firmware Updates (FFU) enables features enhancement in the field. Using this mechanism, the host downloads a new version of the firmware to the e.MMC device and instructs the e.MMC device to install the new downloaded firmware into the device. The entire FFU process occurs in the background without affecting the user / OS data. During the FFU process, the host can replace firmware files or single / all file systems.

The secure FFU (sFFU) usage model for firmware upgrades is as follows:

1. sFFU files are generated and signed at the SanDisk lab
2. The sFFU files are handed to SanDisk's customer
3. SanDisk's customer can push the firmware updates to their end-users in a transparent way

   Note 1: The sFFU process and sFFU files are protected against leakage to unauthorized entities.

   Note 2: During the sFFU process the Host may retrieve the exact status of the process using the smart report feature.

For additional information please refer to JESD84-B51 standard and the SanDisk application note on this subject.

2.2. Cache

The e.MMC cache is dedicated volatile memory. Caching enables to improve iNAND performance for both sequential and random access. For additional information please refer to JESD84-B51 standard.

2.3. Discard

iNAND supports discard command as defined in e.MMC 5.1 spec[3]. This command allows the host to identify data which is not needed, without requiring the device to remove the data from the Media. It is highly recommended for use to guarantee optimal performance of iNAND and reduce amount of housekeeping operation.

2.4. Power off Notifications

iNAND supports power off notifications as defined in e.MMC 5.1 spec. The usage of power off notifications allows the device to prepare itself to power off, and improve user experience during power-on. Note that the device may be set into sleep mode while power off notification is enabled.

Power off notification long allows the device to shutdown properly and save important data for fast boot time on the next power cycle.

[3] For additional information refer to JEDEC Standard No. JESD84-B51

2.5. Packed Commands

To enable optimal system performance, iNAND supports packed commands as defined in e.MMC 5.1 spec. It allows the host to pack Read or Write commands into groups (of single type of operation) and transfer these to the device in a single transfer on the bus. Thus, it allows reducing overall bus overheads.

2.6. Boot Partition

iNAND supports e.MMC 5.1 boot operation mode: Factory configuration supplies two boot partitions each 4MB in size for 32GB-256GB.

2.7. RPMB Partition

iNAND supports e.MMC 5.1 RPMB operation mode: Factory configuration supplies one RPMB partition 16MB in size for 32GB-256GB.

2.8. Automatic Sleep Mode

A unique feature of iNAND is automatic entrance and exit from sleep mode. Upon completion of an operation, iNAND enters sleep mode to conserve power if no further commands are received. The host does not have to take any action for this to occur, however, in order to achieve the lowest sleep current, the host needs to shut down its clock to the memory device. In most systems, embedded devices are in sleep mode except when accessed by the host, thus conserving power. When the host is ready to access a memory device in sleep mode, any command issued to it will cause it to exit sleep and respond immediately.

2.9. Sleep (CMD5)

An iNAND 7550 device may be switched between a Sleep and a Standby state using the SLEEP/AWAKE (CMD5). In the Sleep state the power consumption of the memory device is minimized and the memory device reacts only to the commands RESET (CMD0) and SLEEP/AWAKE (CMD5). All the other commands are ignored by the memory device.

The VCC power supply may be switched off in Sleep state to enable even further system power consumption saving.

For additional information please refer to JESD84-B51.

2.10. Enhanced Reliable Write

iNAND 7550 supports enhanced reliable write as defined in e.MMC 5.1 spec.

Enhanced reliable write is a special write mode in which the old data pointed to by a logical address must remain unchanged until the new data written to same logical address has been successfully programmed. This is to ensure that the target address updated by the reliable write transaction never contains undefined data. When writing in reliable write, data will remain valid even if a sudden power loss occurs during programming.

2.11.Sanitize

The Sanitize operation is used to remove data from the device. The use of the Sanitize operation requires the device to physically remove data from the unmapped user address space. The device will continue the sanitize operation, with busy asserted, until one of the following events occurs:

- Sanitize operation is complete
- HPI is used to abort the operation
- Power failure
- Hardware reset

Following a sanitize operation completion, no data should remain in the unmapped host address space.

2.12.Secure Erase

For backward compatibility reasons, in addition to the standard erase command the iNAND 7550 supports the optional Secure Erase command[4].

This command allows the host to erase the provided range of LBAs and ensure no older copies of this data exist in the flash.

2.13.Secure Trim

For backward compatibility reasons, iNAND 7550 supports Secure Trim command. The Secure Trim[5] command is similar to the Secure Erase command but performs a secure purge operation on write blocks instead of erase groups.

The secure trim command is performed in two steps:

1) Marks the LBA range as candidate for erase.
2) Erases the marked address range and ensures no old copies are left.

2.14.Partition Management

iNAND 7550 offers the possibility for the host to configure additional split local memory partitions with independent addressable space starting from logical address 0x00000000 for different usage models. Therefore, memory block area scan be classified as follows

- Factory configuration supplies two boot partitions (refer to section 2.7) implemented as enhanced storage media and one RPMB partitioning of 4MB in size (refer to section 2.8).
- Up to four General Purpose Area Partitions can be configured to store user data or sensitive data, or for other host usage models. The size of these partitions is a multiple of the write protect group. Size can be programmed once in device life-cycle (one-time programmable).

[4] For additional information refer to JEDEC Standards No. JESD84-B51

[5] For additional information refer to JEDEC Standards No. JESD84-B51

2.15.Device Health

Device Health is similar to SMART features of modern hard disks; it provides only vital NAND flash program/erase cycles information in percentage of the flash life span.

The host can query Device Health information utilizing standard MMC command, to get the extended CSD structure:

DEVICE_LIFE_TIME_EST_TYP_A[268], The host may use it to query SLC device health information

DEVICE_LIFE_TIME_EST_TYP_B[269], The host may use it to query TLC device health information

The device health feature will provide a % of the wear of the device in 10% fragments.

2.16.EOL Status

EOL status is implemented according to the e.MMC 5.1 spec. One additional state (state 4) was added to INAND 7550 which indicates that the device is in EOL mode.

2.17.Enhanced Write Protection

To allow the host to protect data against erase or write iNAND 7550 supports two levels of write protect command

- The entire iNAND 7550 (including the Boot Area Partitions, General Purpose Area Partition, and User Area Partition) may be write-protected by setting the permanent or temporary write protect bits in the CSD
- Specific segments of iNAND 7550 may be permanently, power-on or temporarily write protected. Segment size can be programmed via the EXT_CSD register

For additional information please refer to the JESD84-B51 standard.

2.18.High Priority Interrupt (HPI)

The operating system usually uses demand-paging to launch a process requested by the user. If the host needs to fetch pages while in a middle of a write operation the request will be delayed until the completion of the write command.

The high priority interrupt (HPI) as defined in JESD84-B51 enables low read latency operation by suspending a lower priority operation before it is actually completed.

For additional information on the HPI function, refer to JESD84-B51.

2.19.H/W Reset

Hardware reset may be used by host to reset the device, moving the device to a Pre-idle state and disabling the power-on period write protect on blocks that were power-on write protected before the reset was asserted. For more information, refer to JESD84-B51 standard.

2.20.Host-Device Synchronization Flow (Enhanced STROBE)

The Enhanced STROBE feature as implemented in iNAND 7550 allows utilizing STROBE to synchronize also the CMD response:

- CMD clocking stays SDR (similar to legacy DDR52)
- Host commands are clocked out with the rising edge of the host clock (as done in legacy e.MMC devices)
- iNAND 7550 will provide STROBE signaling synced with the CMD response in addition to DATA Out
- Host may use the STROBE signaling for DAT and CMD-Response capturing eliminating the need for a tuning mechanism

This feature requires support by the host to enable faster and more reliable operation.

2.21.Command-Queue

e.MMC Command Queue enables device visibility of next commands and allows performance improvement. The protocol allows the host to queue up to 32 data-transfer commands in the device by implementing 5 new commands.

The benefits of command queuing are:

- Random Read performance improvement (higher IOPs)
- Reducing protocol overhead
- Command issuance allowed while data transfer is on-going
- Device order the tasks according to best access to/from flash

2.22.Frequent Used Commands in CmdQ

The Frequent Used Commands feature permits the following commands to be sent by the host when queue is non-empty FLUSH, BARRIER and DISCARD. In addition, the Frequent Used Commands feature provides alternative encodings for these commands to facilitate faster processing in device.

This feature can increase the effective performance when using Command Queue mode.

2.23.HS400 tuning

This feature enables tuning command (CMD21) in HS400 mode, which may be used for calibration of DLL to compensate of PCB design/manufacturing differences. The Host may use adjustable sampling to determine the correct sampling point. A predefined tuning block stored in Device may be used by the Host as an aid for finding the optimal data sampling point. The Host can use CMD21 tuning command to read the tuning block.

3. PRODUCT SPECIFICATIONS

3.1. Typical Power Requirements

Table 3 – iNAND 7550 **Power Consumption Sleep** (Ta=25°C@3.3/1.8V)

	32GB	64GB	128GB	256GB	Units
HS400 Sleep (CMD5 – VCCQ, VCC off)	150	150	150	150	uA
HS200 Sleep (CMD5 – VCCQ, VCC off)	150	150	150	150	uA

Table 4 - iNAND 7550, **Power Consumption Peak** (Max) VCC / VCCQ (Ta=25°C@3.3V/1.8V)

		32GB	64GB	128GB	256GB	Units
Active HS400	Peak [2µs window] VCC	170	270	450	450	mA
	Max [1ms window] VCCQ	330	340	360	360	mA
Active HS200	Peak [2µs window] VCC	170	270	450	450	mA
	Max [1ms window] VCCQ	170	180	200	200	mA

Table 5 - iNAND 7550, **Power Consumption RMS** VCC / VCCQ (Ta=25°C@3.3V/1.8V)

			32GB	64GB	128GB	256GB	Units
HS400	RMS [100ms window] VCC	Read	70	80	80	80	mA
		Write	50	90	125	125	mA
	RMS [100ms window] VCCQ	Read	235	245	265	265	mA
		Write	130	160	190	190	mA
HS200	RMS [100ms window] VCC	Read	50	65	75	75	mA
		Write	50	75	85	85	mA
	RMS [100ms window] VCCQ	Read	150	160	175	175	mA
		Write	130	145	160	160	mA

3.2. Operating Conditions

3.2.1. Operating and Storage Temperature Specifications

Table 6 - Operating and Storage Temperatures

Temperature	Minimum and Maximum Operating*	-25° C to 85° C
	Minimum and Maximum Non-Operating: After soldered onto PCBA	-40° C to 85° C

* Per e.MMC 5.1 specification (JESD84-B51): To achieve optimized power/performance, maximum Tcase temperature should not exceed 85°C.

3.2.2. Moisture Sensitivity

The moisture sensitivity level for iNAND 7550 is MSL = 3.

3.3. Reliability

SanDisk iNAND 7550 product meets or exceeds NAND type of products Endurance and Data Retention requirements as per evaluated representative usage models for designed market and relevant sections of JESD47I standard.

Table 7 - Critical Reliability Characteristics

Reliability Characteristics	Description	Value
Uncorrectable Bit Error Rate (UBER)	Uncorrectable bit error rate will not exceed one sector in the specified number of bits read. In such rare events data can be lost.	**1 sector in 10^{15} bits read**

Write Endurance Specification (TBW)	Write endurance is commonly classified in Total Terabytes Written (TBW) to a device. This is the total amount of data that can be written to the device over its useful life time and depends on workload written at certain operated temperature range.
	Representative workload description:
	• 80% Sequential write, 20% Random Write.
	• Distribution of IO Transaction Sizes:
	  ○ <16KB: 82%
	  ○ 16KB-128KB: 17%
	  ○ >128KB: 1%
	• Cache On, Packed Off
	• Host data is 4K aligned
	• 30% of product lifetime operate @85° C T-case
	• 70% of product lifetime operate @55° C T-case
		Total Terabytes Written [TBW] Per representative Android workload:
		32GB: 40[TB]
		64GB: 80[TB]
		128GB: 160[TB]
		256GB: 320[TB]

Data Retention Specification (Years)	Fresh or Early Life Device (A device whose total write cycles to the flash is less than 10% of the maximum endurance specification)	**10 years of Data Retention @ 25°C & 55°C**
	Cycled Device (Any device whose total write cycles are between 10% of the maximum write endurance specification and equal to or exceed the maximum write endurance specification)	**1 year of Data Retention @ 25°C & 55°C** Note: In the case where the number of writes exceed the endurance spec read and Write performance can be intermediately reduced.

3.4. Typical System Performance

Table 8 – Typical Sequential Performance

	HS400		HS200	
	Write (MBs)	**Read (MBs)**	**Write (MBs)**	**Read (MBs)**
32GB	150	300	130	160
64GB	230	300	130	170
128GB	260	300	130	170
256GB	260	300	130	170

Table 9 – Typical Random Performance

	HS400		HS200	
	Write (IOPS)	**Read (IOPS)**	**Write (IOPS)**	**Read (IOPS)**
32GB	15K	20K	6K	10K
64GB	15K	20K	6K	10K
128GB	15K	20K	6K	10K
256GB	15K	20K	6K	10K

Note 1: Sequential Read/Write performance is measured under HS400 mode with a bus width of 8 bit at 200 MHz DDR mode, chunk size of 512KB, and data transfer of 1GB.

Note 2: Random performance is measured with a chunk size of 4KB and address range of 1GB.

Note 3: All performance is measured using SanDisk proprietary test environment, without file system overhead and host turn-around time (HTAT).

Note 4: Write performance is measured for 100MB host payloads.

4. PHYSICAL SPECIFICATIONS

The SanDisk iNAND 7550 is a 153-pin, thin fine-pitched ball grid array (BGA). See Figure 2 and Tables 10/11/12 for physical specifications and dimensions.

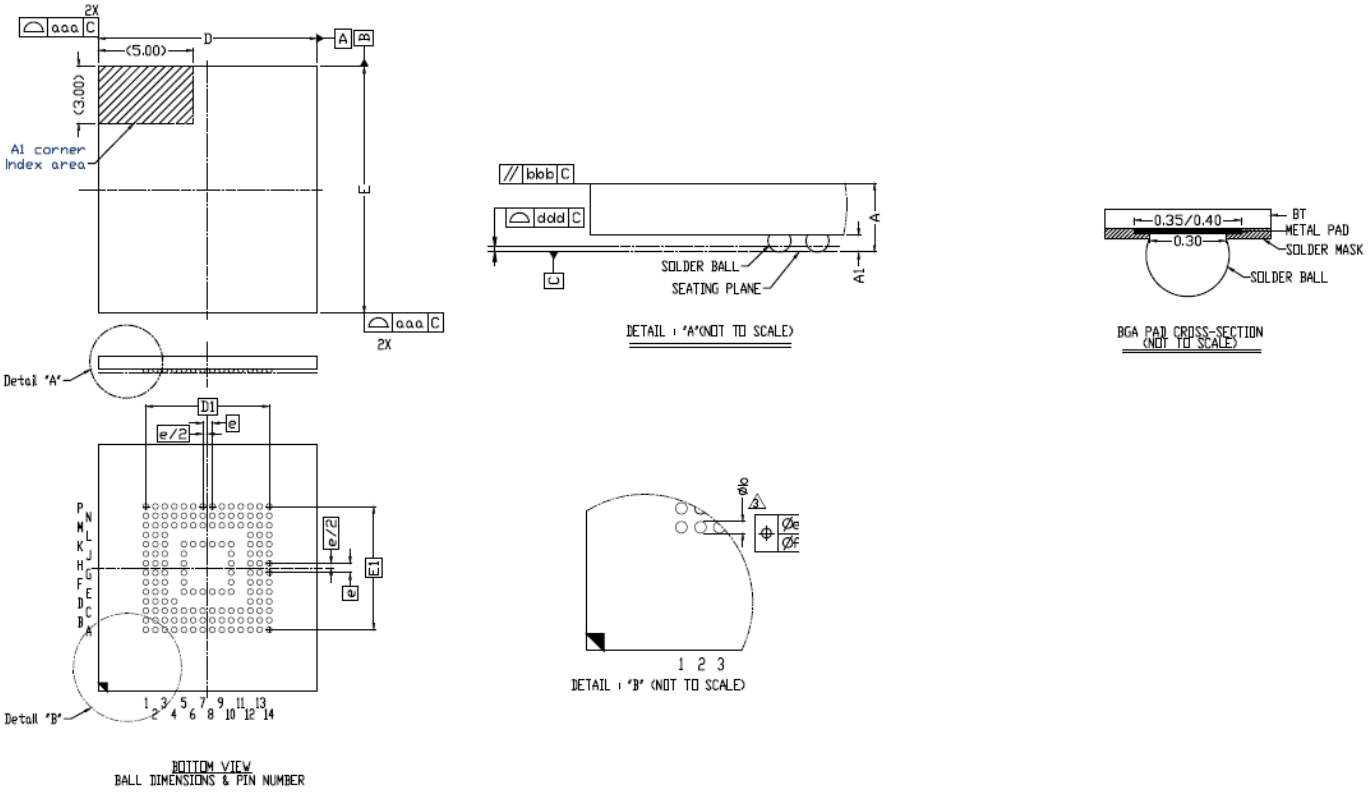


Figure 2 - INAND 7550 Package Outline Drawing

Table 10 –Package Specification 32-256GB

32GB/64GB/128GB/256GB			
Symbol	Dimension in millimeters		
	Minimum	Nominal	Maximum
A	0.8		1
A1	0.17	0.22	0.27
D	11.4	11.5	11.6
E	12.9	13	13.1
D1	-	6.5	-
E1	-	6.5	-
e	-	0.5	-
b	0.25	0.3	0.35
aaa	0.1		
bbb	0.1		
ddd	0.08		
eee	0.15		
fff	0.05		

5. INTERFACE DESCRIPTION

5.1. MMC I/F Ball Array

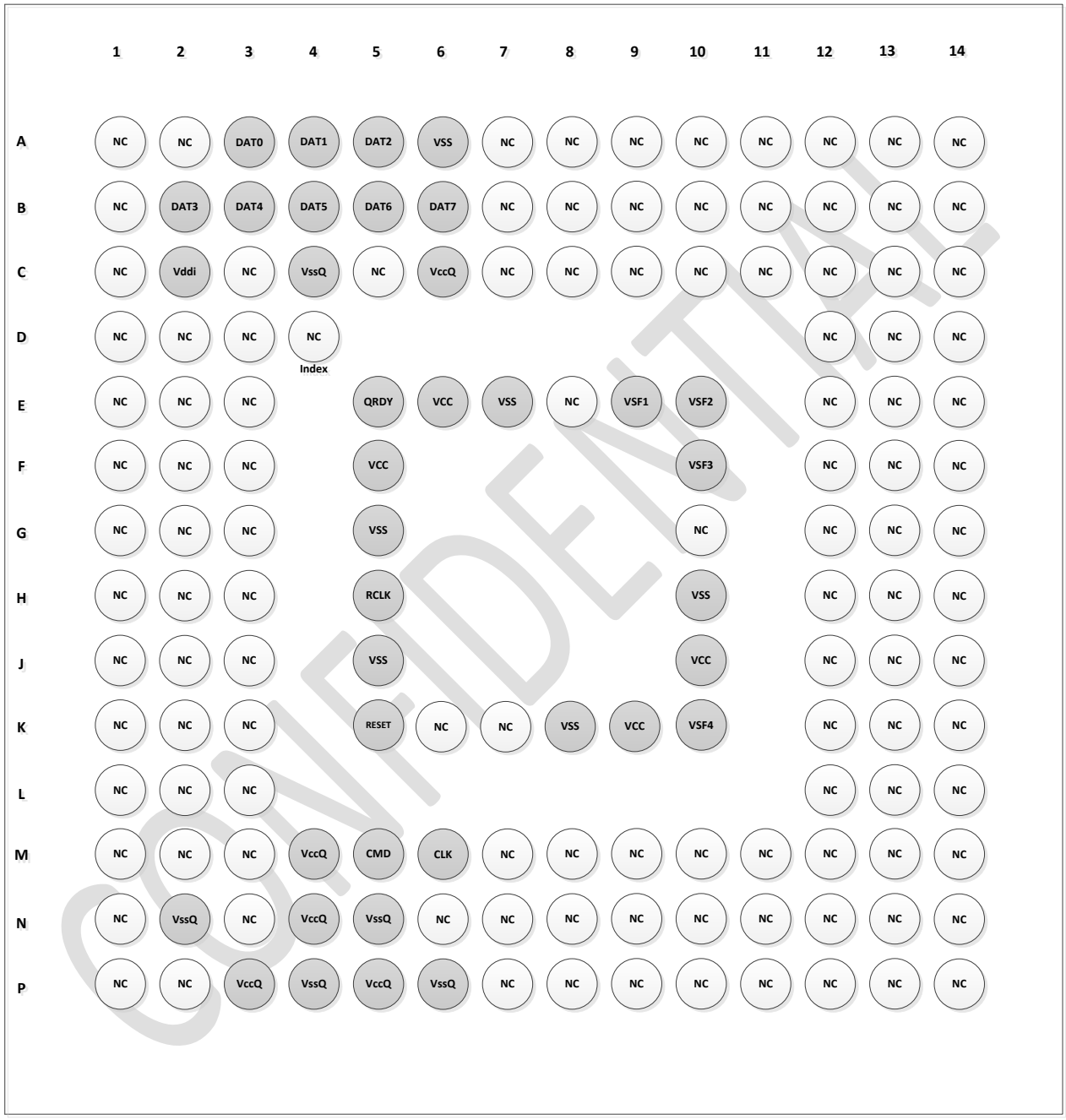


Figure 3 - 153 balls - Ball Array (Top View)

5.2. Pins and Signal Description

Table 13 contains the SanDisk iNAND 7550, with MMC interface (153 balls), functional pin assignment.

Table 11 – Functional Pin Assignment, 153 balls

Ball No.	Ball Signal	Type	Description
A3	DAT0	I/O	Data I/O: Bidirectional channel used for data transfer
A4	DAT1		
A5	DAT2		
B2	DAT3		
B3	DAT4		
B4	DAT5		
B5	DAT6		
B6	DAT7		
M5	CMD	I/O	Command: A bidirectional channel used for device initialization and command transfers.
E5	QRDY	O	An optional pin, disabled by default, toggled by the device when the value of QSR changes.
M6	CLK	Input	Clock: Each cycle directs a 1-bit transfer on the command and DAT lines
K5	RST_n		Hardware Reset
H5	RCLK	Output	Data Strobe
E6	VCC	Supply	Flash I/O and memory power supply
F5	VCC		
J10	VCC		
K9	VCC		
C6	VCCQ	Supply	Memory controller core and MMC I/F I/O power supply
M4	VCCQ		
N4	VCCQ		
P3	VCCQ		
P5	VCCQ		
E7	VSS	Supply	Flash I/O and memory ground connection
G5	VSS		
H10	VSS		
K8	VSS		
A6	VSS		
J5	VSS		
C4	VSSQ	Supply	Memory controller core and MMC I/F ground connection
N2	VSSQ		
N5	VSSQ		
P4	VSSQ		
P6	VSSQ		
C2	VDDi		Internal power node. Connect 0.1uF capacitor from VDDi to ground
E9	VSF1	VSF	Vendor Specific Function balls for test/debug. VSF balls should be floating and be brought out to test pads.
E10	VSF2		
F10	VSF3		
K10	VSF4		

Note: All other pins are not connected [NC] and can be connected to GND or left floating

5.3. Registers value

5.3.1. OCR Register

Parameter	DSR slice	Description	Value	Width
Access Mode	[30:29]	Access mode	2h	2
	[23:15]	VDD: 2.7 - 3.6 range	1FFh	9
	[14:8]	VDD: 2.0 - 2.6 range	00h	7
	[7]	VDD: 1.7 - 1.95 range	1h	1

Note: Bit 30 is set because the device is High Capacity; bit 31 will be set only when the device is ready.

5.3.2. CID Register

Parameter	DSR slice	Description	Value	Width
MMC MID	[127:120]	Manufacturer ID	45h	8
CBX	[113:112]	Device BGA	01h	2
OID	[111:104]	OEM/Application ID	00h	8
PNM	[103:56]	Product name	32GB-DA4032 64GB-DA4064 128GB-DA4128 256GB-DA4256	48
PRV	[55:48]	Product revision	01h	8
PSN	[47:16]	Product serial number	Random by Production	32
MDT	[15:8]	Manufacturing date	month, year	8
CRC	[7:1]	Calculated CRC	CRC7 Generator	7

Note: Please refer to the definition of the MDT field as defined in e.MMC Spec version 5.0.

5.3.3. DSR Register

Parameter	DSR slice	Description	Value	Width
RSRVD	[15:8]	Reserved	04h	8
RSRVD	[7:0]	Reserved	04h	8

Note: DSR is not implemented; in case of read, a value of 0x0404 will be returned.

5.3.4. CSD Register

Parameter	CSD Slice	Description	Value	Width
CSD_STRUCTURE	[127:126]	CSD structure	3h	3
SPEC_VERS	[125:122]	System specification version	4h	4
TAAC	[119:112]	Data read access-time 1	0Fh	8
NSAC	[111:104]	Data read access-time 2 in CLK cycles (NSAC*100)	00h	8
TRAN_SPEED	[103:96]	Max. bus clock frequency	32h	8
CCC	[95:84]	Card command classes	8F5h	12
READ_BL_LEN	[83:80]	Max. read data block length	9h	4
READ_BL_PARTIAL	[79:79]	Partial blocks for read allowed	0b	1
WRITE_BLK_MISALIGN	[78:78]	Write block misalignment	0b	1
READ_BLK_MISALIGN	[77:77]	Read block misalignment	0b	1
DSR_IMP	[76:76]	DSR implemented	0b	1
*C_SIZE	[73:62]	Device size	FFFh	12
VDD_R_CURR_MIN	[61:59]	Max. read current @ VDD min	7h	3
VDD_R_CURR_MAX	[58:56]	Max. read current @ VDD max	7h	3
VDD_W_CURR_MIN	[55:53]	Max. write current @ VDD min	7h	3
VDD_W_CURR_MAX	[52:50]	Max. write current @ VDD max	7h	3
C_SIZE_MULT	[49:47]	Device size multiplier	7h	3
ERASE_GRP_SIZE	[46:42]	Erase group size	1Fh	5
ERASE_GRP_MULT	[41:37]	Erase group size multiplier	1Fh	5
WP_GRP_SIZE	[36:32]	Write protect group size	0Fh	5
WP_GRP_ENABLE	[31:31]	Write protect group enable	1h	1
DEFAULT_ECC	[30:29]	Manufacturer default	0h	2
R2W_FACTOR	[28:26]	Write speed factor	2h	3
WRITE_BL_LEN	[25:22]	Max. write data block length	9h	4
WRITE_BL_PARTIAL	[21:21]	Partial blocks for write allowed	0h	1
CONTENT_PROT_APP	[16:16]	Content protection application	0h	1
FILE_FORMAT_GRP	[15:15]	File format group	0h	1
COPY	[14:14]	Copy flag (OTP)	1h	1
PERM_WRITE_PROTECT	[13:13]	Permanent write protection	0h	1
TMP_WRITE_PROTECT	[12:12]	Temporary write protection	0h	1
FILE_FORMAT	[11:10]	File format	0h	2
ECC	[9:8]	ECC code	0h	2
CRC	[7:1]	Calculated CRC	CRC7 Generator	7

5.3.5. EXT_CSD Register

Parameter	ECSD slice	Description	Value
S_CMD_SET	[504]	Supported Command Sets	1h
HPI_FEATURES	[503]	HPI Features	1h
BKOPS_SUPPORT	[502]	Background operations support	1h
MAX_PACKED_READS	[501]	Max packed read commands	3Fh
MAX_PACKED_WRITES	[500]	Max packed write commands	3Fh
DATA_TAG_SUPPORT	[499]	Data Tag Support	1h
TAG_UNIT_SIZE	[498]	Tag Unit Size	3h
TAG_RES_SIZE	[497]	Tag Resources Size	3h
CONTEXT_CAPABILITIES	[496]	Context management capabilities	5h
LARGE_UNIT_SIZE_M1	[495]	Large Unit size	0h
EXT_SUPPORT	[494]	Extended partitions attribute support	3h
SUPPORTED_MODES	[493]	FFU supported modes	3h
FFU_FEATURES	[492]	FFU features	0h
OPERATION_CODES_TIMEOUT	[491]	Operation codes timeout	10h
FFU_ARG	[490:487]	FFU Argument	0h
BARRIER_SUPPORT	[486]	Cache barrier support	1h
CMDQ_SUPPORT	[308]	Command queue support	1h
CMDQ_DEPTH	[307]	Command queue depth	1Fh
NUMBER_OF_FW_SECTORS_CORRECTLY_PROGRAMMED	[305:302]	Number of FW sectors correctly programmed	0h
VENDOR_PROPRIETARY_HEALTH_REPORT	[301:270]	Vendor proprietary health report	0h
DEVICE_LIFE_TIME_EST_TYP_B	[269]	Device life time estimation type B (MLC)	1h
DEVICE_LIFE_TIME_EST_TYP_A	[268]	Device life time estimation type A (SLC)	1h
PRE_EOL_INFO	[267]	Pre EOL information	1h
OPTIMAL_READ_SIZE	[266]	Optimal read size	8h
OPTIMAL_WRITE_SIZE	[265]	Optimal write size	8h
OPTIMAL_TRIM_UNIT_SIZE	[264]	Optimal trim unit size	8h
DEVICE_VERSION	[263:262]	Device version	5051h
FIRMWARE_VERSION	[261:254]	Firmware version	FW Version
PWR_CL_DDR_200_360	[253]	Power class for 200MHz, DDR at VCC= 3.6V	0h
CACHE_SIZE	[252:249]	Cache size	1000h
GENERIC_CMD6_TIME	[248]	Generic CMD6 timeout	19h
POWER_OFF_LONG_TIME	[247]	Power off notification(long) timeout	19h
BKOPS_STATUS	[246]	Background operations status	Default = 0h

Parameter	ECSD slice	Description	Value
CORRECTLY_PRG_SECTORS_NUM	[245:242]	Number of correctly programmed sectors	Default = 0h
INI_TIMEOUT_AP	[241]	1st Initialization time after partitioning	FFh
CACHE_FLUSH_POLICY	[240]	Cache Flush Policy	1h
PWR_CL_DDR_52_360	[239]	Power class for 52MHz, DDR at VCC = 3.6V	0h
PWR_CL_DDR_52_195	[238]	Power class for 52MHz, DDR at VCC = 1.95V	0h
PWR_CL_200_195	[237]	Power class for 200MHz at VCCQ =1.95V, VCC = 3.6V	0h
PWR_CL_200_130	[236]	Power class for 200MHz, at VCCQ =1.3V, VCC = 3.6V	0h
MIN_PERF_DDR_W_8_52	[235]	Minimum Write Performance for 8bit at 52MHz in DDR mode	0h
MIN_PERF_DDR_R_8_52	[234]	Minimum Read Performance for 8bit at 52MHz in DDR mode	0h
TRIM _MULT	[232]	TRIM Multiplier	3h
SEC_FEATURE_SUPPORT	[231]	Secure Feature support	55h
SEC_ERASE_MULT	[230]	Secure Erase Multiplier	A6h
SEC_TRIM_MULT	[229]	Secure TRIM Multiplier	A6h
BOOT_INFO	[228]	Boot Information	7h
BOOT_SIZE_MULT	[226]	Boot partition size	20h
ACCESS_SIZE	[225]	Access size	8h
HC_ERASE_GROUP_SIZE	[224]	High Capacity Erase unit size	1h (see WP group size table below)
ERASE_TIMEOUT_MULT	[223]	High capacity erase time out	3h
REL_WR_SEC_C	[222]	Reliable write sector count	1h
HC_WP_GRP_SIZE	[221]	High capacity write protect group size	10h (see WP group size table below)
S_C_VCC	[220]	Sleep current [VCC]	32GB: 7h 64GB: 8h 128GB: 9h 256GB: Ah
S_C_VCCQ	[219]	Sleep current [VCCQ]	7h
PRODUCTION_STATE_AWARENESS_TIMEOUT	[218]	Production state awareness timeout	17h
S_A_TIMEOUT	[217]	Sleep/Awake time out	13h
SLEEP_NOTIFICATION_TIME	[216]	Sleep notification timeout	17h
SEC_COUNT	[215:212]	Sector count	See exported capacity table below
SECURE_WP_INFO	[211]	Secure Write Protect Info	1h
MIN_PERF_W_8_52	[210]	Minimum Write Performance for 8bit @52MHz	Ah
MIN_PERF_R_8_52	[209]	Minimum Read Performance for 8bit @52MHz	Ah

Parameter	ECSD slice	Description	Value
MIN_PERF_W_8_26_4_52	[208]	Minimum Write Performance for 4bit @52MHz or 8bit @26MHz	Ah
MIN_PERF_R_8_26_4_52	[207]	Minimum Read Performance for 4bit @52MHz or 8bit @26MHz	Ah
MIN_PERF_W_4_26	[206]	Minimum Write Performance for 4bit @26MHz	Ah
MIN_PERF_R_4_26	[205]	Minimum Read Performance for 4bit @26MHz	Ah
PWR_CL_26_360	[203]	Power Class for 26MHz @ 3.6V	0h
PWR_CL_52_360	[202]	Power Class for 52MHz @ 3.6V	0h
PWR_CL_26_195	[201]	Power Class for 26MHz @ 1.95V	0h
PWR_CL_52_195	[200]	Power Class for 52MHz @ 1.95V	0h
PARTITION_SWITCH_TIME	[199]	Partition switching timing	3h
OUT_OF_INTERRUPT_TIME	[198]	Out-of-interrupt busy timing	19h
DRIVER_STRENGTH	[197]	I/O Driver Strength	1Fh (Reporting four strengths, but supporting only one)
CARD_TYPE	[196:195]	Card Type	57h
CSD_STRUCTURE	[194]	CSD Structure Version	2h
EXT_CSD_REV	[192]	Extended CSD Revision	8h
CMD_SET	[191]	Command Set	Default = 0h Updated in runtime
CMD_SET_REV	[189]	Command Set Revision	0h
POWER_CLASS	[187]	Power Class	Dh
HS_TIMING	[185]	High Speed Interface Timing	Default = 0h Updated in runtime by the host
DATA_STRB_MODE_SUPPORT	[184]	Data strobe mode support	1h
BUS_WIDTH	[183]	Bus Width Mode	Default = 0h Updated in runtime by the host
ERASE_MEM_CONT	[181]	Content of explicit erased memory range	0h
PARTITION_CONFIG	[179]	Partition Configuration	Default = 0h Updated in runtime by the host
BOOT_CONFIG_PROT	[178]	Boot config protection	Default = 0h Updated in runtime by the host
BOOT_BUS_CONDITIONS	[177]	Boot bus width1	Default = 0h Updated in runtime by the host
ERASE_GROUP_DEF	[175]	High-density erase group definition	Default = 0h Updated in runtime by the host
BOOT_WP_STATUS	[174]	Boot write protection status registers	Default = 0h Updated in runtime
BOOT_WP	[173]	Boot area write protect register	0h

Parameter	ECSD slice	Description	Value
USER_WP	[171]	User area write protect register	0h
FW_CONFIG	[169]	FW Configuration	0h
RPMB_SIZE_MULT	[168]	RPMB Size	80h
WR_REL_SET	[167]	Write reliability setting register	1Fh
WR_REL_PARAM	[166]	Write reliability parameter register	15h
SANITIZE_START	[165]	Start Sanitize operation	Default = 0h Updated in runtime by the host
BKOPS_START	[164]	Manually start background operations	Default = 0h Updated in runtime by the host
BKOPS_EN	[163]	Enable background operations handshake	2h
RST_n_FUNCTION	[162]	H/W reset function	Default = 0h Updated by the host
HPI_MGMT	[161]	HPI management	Default = 0h Updated by the host
PARTITIONING SUPPORT	[160]	Partitioning support	7h Note: EUDA is not supported
MAX_ENH_SIZE_MULT	[159:157]	Max Enhanced Area Size	0h
PARTITIONS_ATTRIBUTE	[156]	Partitions Attribute	Default = 0h Updated by the host
PARTITION_SETTING_ COMPLETED	[155]	Partitioning Setting	Default = 0h Updated by the host
GP_SIZE_MULT	[154:143]	General Purpose Partition Size (GP4)	0h
GP_SIZE_MULT	[151:149]	General Purpose Partition Size (GP3)	0h
GP_SIZE_MULT	[148:146]	General Purpose Partition Size (GP2)	0h
GP_SIZE_MULT	[145:143]	General Purpose Partition Size (GP1)	0h
ENH_SIZE_MULT	[142:140]	Enhanced User Data Area Size	0h
ENH_START_ADDR	[139:136]	Enhanced User Data Start Address	0h
SEC_BAD_BLK_MGMNT	[134]	Bad Block Management mode	0h
PRODUCTION_STATE_AWARE NESS	[133]	Production state awareness	0h
TCASE_SUPPORT	[132]	Package Case Temperature is controlled	0h
PERIODIC_WAKEUP	[131]	Periodic Wake-up	0h
PROGRAM_CID_CSD_DDR_S UPPORT	[130]	Program CID/CSD in DDR mode support	0h
VENDOR_SPECIFIC_FIELD	[127:64]	Vendor Specific Fields	Reserved
NATIVE_SECTOR_SIZE	[63]	Native sector size	0h
USE_NATIVE_SECTOR	[62]	Sector size emulation	0h
DATA_SECTOR_SIZE	[61]	Sector size	0h

Parameter	ECSD slice	Description	Value
INI_TIMEOUT_EMU	[60]	1st initialization after disabling sector size emulation	Ah
CLASS_6_CTRL	[59]	Class 6 commands control	0h
DYNCAP_NEEDED	[58]	Number of addressed group to be Released	0h
EXCEPTION_EVENTS_CTRL	[57:56]	Exception events control	0h
EXCEPTION_EVENTS_STATUS	[55:54]	Exception events status	0h
EXT_PARTITIONS_ATTRIBUTE	[53:52]	Extended Partitions Attribute	0h
CONTEXT_CONF	[51:37]	Context configuration	Default = 0h
PACKED_COMMAND_STATUS	[36]	Packed command status	Default = 0h Updated in runtime
PACKED_FAILURE_INDEX	[35]	Packed command failure index	Default = 0h Updated in runtime
POWER_OFF_NOTIFICATION	[34]	Power Off Notification	Default = 0h Updated in runtime by the host
CACHE_CTRL	[33]	Control to turn the Cache ON/OFF	0h
FLUSH_CACHE	[32]	Flushing of the cache	0h
BARRIER_CTRL	[31]	Cache barrier	0h
MODE_CONFIG	[30]	Mode config	0h
MODE_OPERATION_CODES	[29]	Mode operation codes	0h
FFU_STATUS	[26]	FFU status	0h
PRE_LOADING_DATA_SIZE	[25:22]	Pre loading data size	0h
MAX_PRE_LOADING_DATA_SIZE	[21:18]	Max pre loading data size	See Max Preloading size table below
PRODUCT_STATE_AWARENESS_ENABLEMENT	[17]	Product state awareness enablement	3h AUTO_PRE_SOLDERING
SECURE_REMOVAL_TYPE	[16]	Secure Removal Type	8h
CMDQ_MODE_EN	[15]	Command queue	0h

5.3.6. User Density

The following table shows the capacity available for user data for the different device sizes:

Table 12: Capacity for user data

Capacity	LBA [Hex]
32GB	0x3A3E000
64GB	0x747C000
128GB	0xE8F6000
256GB	0x1D1F0000

Table 13: Write protect group size

Capacity	HC_ERASE_GROUP_SIZE	HC_WP_GRP_SIZE	Erase Unit Size [MB]	Write Protect Group Size [MB]
32GB	0x1	0x10	0.5MB	8MB
64GB	0x1	0x10	0.5MB	8MB
128GB	0x1	0x10	0.5MB	8MB
256GB	0x1	0x10	0.5MB	8MB

Table 14: Max Preloading Data Size

Capacity	Max preloading Image size (in LBA Hex)	Max preloading Image in MB
32GB	1,338,4C8	9,840
64GB	2,670,998	19,681
128GB	4,CE0,8A0	39,361
256GB	9,9C2,660	78,724

6. HW APPLICATION GUIDELINES

6.1. Design Guidelines

- The e.MMC specification enforces single device per host channel; multi-device configuration per a single host channel is not supported.
- CLK, RCLK(DS), CMD and DATx lines should be connected to respected host signals. The e.MMC specification requires that all signals will be connected point-to-point, i.e. a single e.MMC device per host channel.
- The e.MMC hardware reset signal (RST_n) is not mandatory and could be connected to the host reset signal or left unconnected (floating) if not used.
- All power supply and ground pads must be connected.
- Make sure pull-up resistors are placed on schematic in case these are external. For further details please refer to “Table 16 - Pull-ups Definition”
- Bypass capacitors shall be placed as close to the e.MMC device as possible; normally it is recommended to have 0.1uF and 4.7uF capacitors per power supply rail, though specific designs may include a different configuration in which there are more than two capacitors:
    - VCC and VCCQ slew rates shall be minimally affected by any bypass capacitors configuration
    - It is recommended to verify the bypass capacitors requirement in the product data sheet
- VDDi bypass capacitor shall be placed on the PCB. The VDDi is an internal power node for the controller and requires capacitor in range 0.1uF – 2.2uF connected between VDDi pad and ground
- Vendor Specific Function (VSF) pins should be connected to accessible test points on the PCB (TP on schematic below). It’s recommended to have accessible ground (GND) pads near each TP on PCB
- It is recommended to layout e.MMC signals with controlled impedance of 45-55 Ohm referencing to adjusted ground plane

6.2. Capacitor Selection & Layout Guidelines

SanDisk iNAND 7550 has three power domains assigned to VCCQ, VCC and VDDi, as shown in Table 17 below.

Pin	Power Domain	Comments
VCCQ	Host Interface	Supported voltage ranges: Low Voltage Region: 1.8V (nominal)
VCC	Memory	Supported voltage range: High Voltage Region: 3.3V (nominal)
VDDi	Internal	VDDi is the internal regulator connection to an external decoupling capacitor.

Table 15- 7550 Power Domains

It is recommended that the power domains connectivity will follow figure 4:

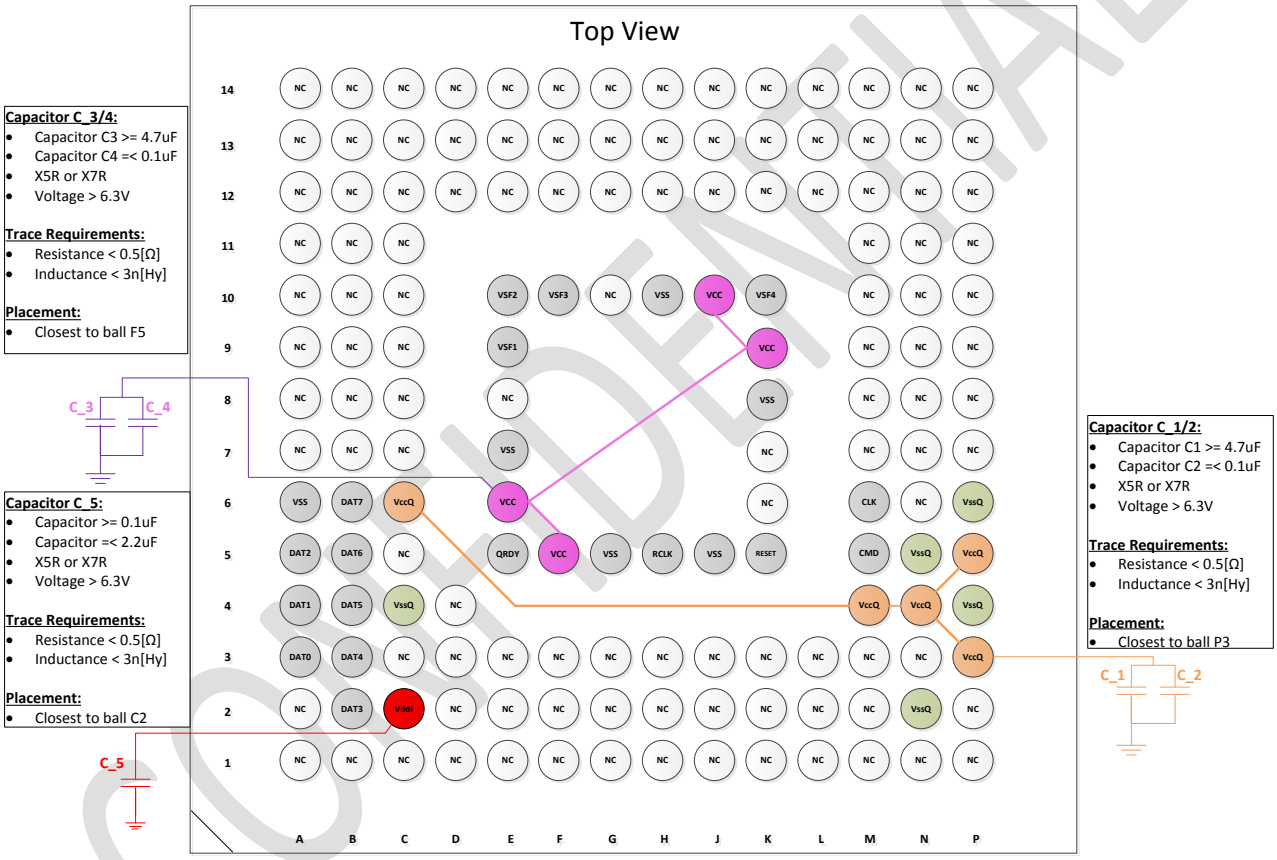


Figure 4 - Recommended Power Domain Connectivity

Note: Signal routing in the diagram is for illustration purposes only and the final routing depends final PCB layout.

For clarity, the diagram does not include VSS connection. All balls marked VSS shall be connected to a ground (GND) plane.

It is recommended to use a X5R/X7R SMT-Ceramic capacitors rated for 6.3V/10V with footprint of 0402 or above.

When using ceramic capacitor, it should be located as close to the supply ball as possible. This will eliminate mounting inductance effects and give the internal IC rail a cleaner voltage supply

Make all of the power (high current) traces as short, direct, and thick as possible. The capacitors should be as close to each other as possible, as it reduces EMI radiated by the power traces due to the high switching currents through them. In addition, it shall also reduce mounting inductance and resistance as well, which in turn reduces noise spikes, ringing, and IR drop which produce voltage errors.

The grounds of the IC capacitors should be connected close together directly to a ground plane. It is also recommended to have a ground plane on both sides of the PCB, as it reduces noise by reducing ground loop.

The loop inductance per capacitor shall not exceed 3nH (both on VCC/VCCQ & VSS/VSSQ loops).

Cin2 shall be placed closer (from both distance & inductance POV) to the iNAND power & ground balls.

Multiple via connections are recommended per each capacitor pad. It is recommended to place the power and ground vias of the capacitor as close to each other as possible.

On test platforms, where the iNAND socket is in use, the loop inductance per capacitor shall not exceed 5nH (both on VCC/VCCQ & VSS/VSSQ loop).

No passives should be placed below the iNAND device (between iNAND & PCB).

VSF balls (VSF1/4) should have exposed and floated test pads on the PCB, with near exposed GND for better measurement.

Signal Traces:

- Data, CMD, CLK & RCLK bus trace length mismatch should be minimal (up to +/-1mm).
- Traces should be45-55 ohm controlled impedance.

6.3. Reference Schematics

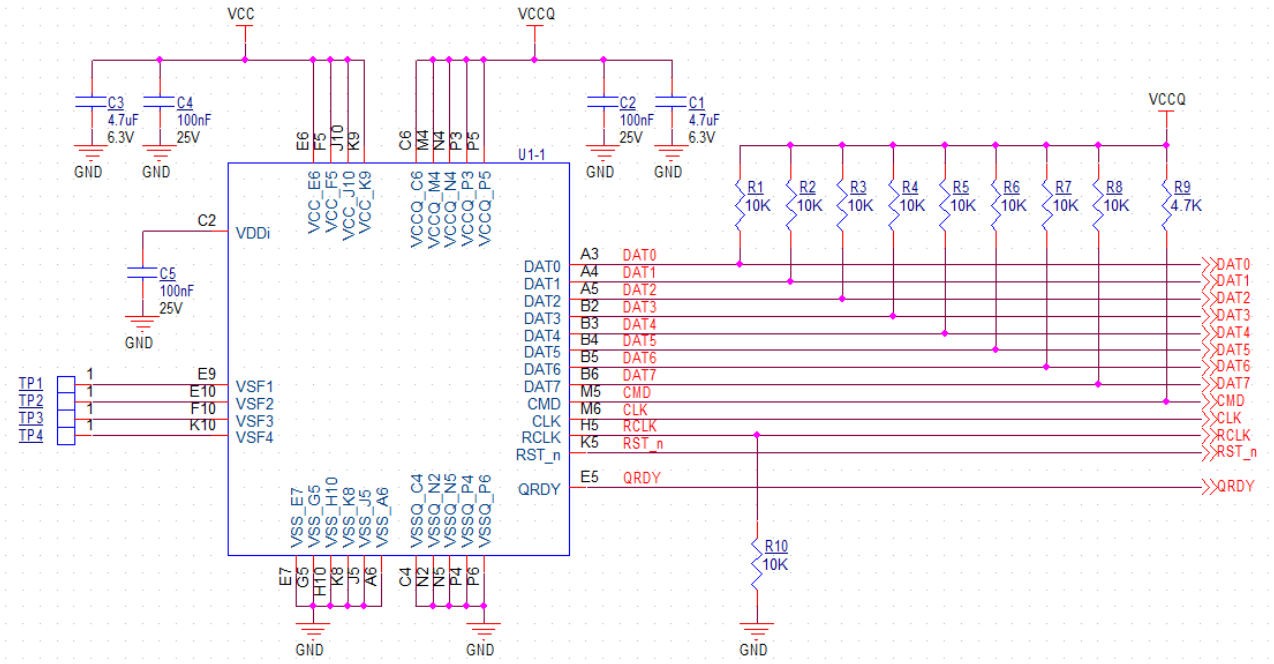


Figure 5 – e.MMC Reference Schematics

Parameter	Symbol	Min	Typ	Max	Unit	Remark
Pull-up resistance for DAT0–7	R_{DAT}	10		100(1)	Kohm	to prevent bus floating
Pull-up resistance for CMD	R_{CMD}	4.7		100(1)	Kohm	to prevent bus floating
Pull-down resistance for Data Strobe (RCLK)	R_{PD}	10		47	Kohm	At HS400 mode

Table 16 – Pull-ups Definition

(1) Recommended maximum pull-up is 50Kohm for 1.8V interface supply voltages. A 3V part may use the whole range up to 100Kohms

Recommended capacitors:

CAPACITOR VALUE	MANUFACTURER	MANUFACTURER P/N
4.7uF	MURATA	GRM185R60J475ME15D
	TAIYO YUDEN	JMK107BJ475MK-T
0.1uF	MURATA	GRM155R71A104KA01D
	KYOCERA	CM05X5R104K06AH
2.2uF	PANASONIC	ECJ0EB0J225M
	SAMSUNG	CL05A225MQ5NSNC

7. PROPRIETY iNAND 7550 FEATURE OVERVIEW

7.1. Content Preloading Operation Mode

High temperature during IR-Reflow process on 3D - X3 flash devices cause significant increase of read errors on TLC blocks (Uncorrectable read errors of data that was programmed before the IR Reflow process).

This high level of read errors is higher compared to previous flash technologies

Currently this level of errors cannot be fixed by special error correction algorithms (as it was done in previous flash technologies)

To overcome these challenges iNAND 7550 introduced the Pre-Loading feature, which solves the IR-Reflow process's reliability, by writing the preloaded data to the SLC area of the device.

Every iNAND 7550 fresh device is defined to start in Implicit Loading state. There are several of exit triggers that will switch it to Migration state. Once Migration is completed the device will start to work in normal state.

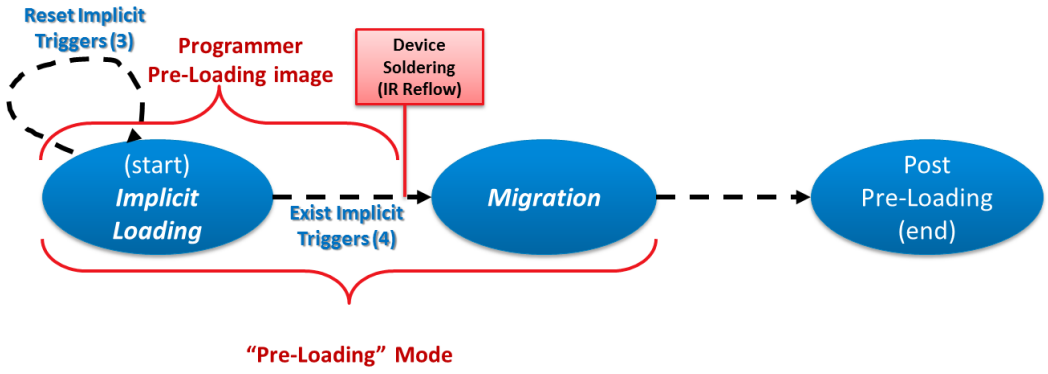


Figure 6 - Pre-Loading flow

During Implicit mode all written data (the preloaded data before IR-Reflow) will be written to the SLC area of the device.

Max preloading data allowed is 33% from device exported capacity.

Triggers to exit implicit mode and start Migration stage are:

- Host accumulated written data payload that is >33% of the exported capacity.
- Host switches interface to High-Speed bus (HS200/HS400).
- (Recommended) Host issues Vendor Specific command signals to device signaling "IR-Reflow completed".

Triggers to reset Implicit mode counters (Only possible during Implicit mode and if device switched already to Migration stage there is no option to reverse/reset it to Implicit stage anymore)

- Host erases the whole written user area.

- Host issues Vendor Specific command of “Production Restore To Default”
- Firmware Download

During Migration state the device will do automatic relocation of the preloaded data written to SLC blocks during implicit mode to TLC blocks, after IR reflow.

It is recommended to allow system BKOPs during IDLE time that will expedite the folding of the preloaded data from SLC to the TLC.

7.2. SmartSLC

The iNAND SmartSLC feature gives the customer the write performance they require, so that they will have a UX experience that makes an X3 memory look better than X2. The iNAND SmartSLC provides the following value to the system:

- Auto-adjust iNAND performance per application need
- Improves system efficiency and UX
  - Reduce system WRITE-BUSY time by improving IO throughput
- Vertical iNAND technology:
  - Host access to iNAND NAND flash performance capabilities
  - Controller and Firmware auto-detections of hosts needs and auto-adjustment device behavior based on these host needs
  - Host (e.MMC driver) customizations and modifications in IDLE time management to allow optimized utilization of SmartSLC capabilities

iNAND 7550 uses allocated SLC blocks within the SanDisk NAND design to implement the feature. The allocation of these blocks does not impact the as sold capacity of the device (Exported Capacity). The device uses a detection mechanism and once a pattern requiring sequential write performance is detected, the device postpones any background management operations, if feasible,) and dedicates resources to SLC programing. Any IDLE state bigger than tIDLE [ms], shall trigger migration operations to free up enough space for the next burst and eliminate potential performance drop.

iNAND SmartSLC buffer size and Performance for SDINBDA4-xxxG products (BigFile Mode):

Capacity (GB)	Buffer Size (GB)	Write speed* (MB/s)
32GB	8	150
64GB	16	230
128GB	32	260
256GB	64	260

* Sequential write Performance is measured using SanDisk proprietary test environment, without file system overhead and host turn-around time (HTAT), 512KB chunk, enough recovery time before measurement @ HS400.

Emptying the iNAND SmartSLC buffer

There are a number of host enabled mechanisms that can be used to empty the SmartSLC buffer (migration). All of these modes can be enabled at the same time or only a single or a few modes can be selected. The more modes that are supported by the host, the more the buffer will be available and empty for use in observing host high speed payloads. During migration time there won't be degradation of device performance and no impact on latency and system responsiveness. Host optional configuration for iNAND SmartSLC:

1. IDLE only mode (PoN=1) – Recommended option.

2. BKOPs APIs with HPI
3. Sleep Notification before standby (CMD5)

	1. Host allow House-Keeping during IDLE (Auto BKOPs)		2. Host periodically send BKOPs API (Manual BKOPs)
SmartSLC Buffer migration	**Migration during in system IDLE with HPI**	**Migration during in system IDLE with HPI**	**Migration during BKOPs Busy**
EXT_CSD REV[192]	7h (e.MMC 5.0)	8h (e.MMC 5.1)	7h or 8h (e.MMC 5.0/5.1)
AUTO_EN BKOPS_EN[163][1]	Don't care	1h	0h
POWER_OFF_NOTIFICATION [34] (PON activated)	1h (POWERED_ON)	1h (POWERED_ON)	Don't care
BKOPS_EN BKOPS_EN[163][0]	Don't care	Don't care	1h
POWER_OFF_NOTIFICATION [34] (Sleep Notification)	No	No	No
Standby mode CMD5	If system uses CMD5 it is requires 5-10sec delay before CMD5 transmission	If system uses CMD5 it is requires 5-10sec delay before CMD5 transmission	Don't care

7.3. Device Report

iNAND 7550 introduce new proprietary Device Report feature that reflects the Firmware and Device status.

- Enabling Device Report Mode: Send CMD62 with argument of 0x96C9D71C - R1b Response will be returned
- Reading Device Report Data: Once the host enters Device Report mode, CMD63 with argument 0x00000000 will retrieve the report - 512 Bytes will be returned to the host (Note: CMD63 behaves similarly to CMD17)
- Resume Normal Operation Mode: Once the Device Report read command (CMD63) was completed, the device automatically goes out of Device Report mode, and resumes normal operation mode.

Field Name	Description	Motivation (Host perspective)	Offset (Dec)	Size (Bytes)
Average Erase Cycles Type C (Enhanced)	The Average Erase cycles value out of all Enhanced area Blocks	To check real life product endurance and lifetime	0	4
Average Erase Cycles Type A (SLC)	The Average Erase cycles value out of all SLC Blocks	To check real life product endurance and lifetime	4	4
Average Erase Cycles Type B (TLC)	The Average Erase cycles value out of all TLC Blocks	To check real life product endurance and lifetime	8	4
Read reclaim count Type C (Enhanced)	The amount of Enhanced Reads operations which passed Read-Scrub thresholds and requires reclaim	To check iNAND data-retention preventions mechanism on management area	12	4
Read reclaim count Type A (SLC)	The amount of SLC Reads operations which passed Read-Scrub thresholds and requires reclaim	To check iNAND data-retention preventions mechanism on SLC area	16	4
Read reclaim count Type B (TLC)	The amount of TLC Reads operations which passed Read-Scrub thresholds and requires reclaim	To check iNAND data-retention preventions mechanism on TLC area	20	4
Bad Block Manufactory	Number of Bad Blocks detected during manufacturing process	To check device number of Bad-Blocks	24	4
Bad Block Runtime Type C (Enhanced)	All Bad Blocks related to the Enhanced area that were detected during run-time	To check device runtime number of Bad-Blocks on Management area	28	4
Bad Block Runtime Type A (SLC)	All Bad Blocks related to the SLC area that were detected during run-time	To check device runtime number of Bad-Blocks on SLC area	32	4
Bad Block Runtime Type B (TLC)	All Bad Blocks related to the TLC area that were detected during run-time	To check device runtime number of Bad-Blocks on TLC area	36	4
Field FW Updates Count	Number of secure Field Firmware Upgrades (sFFU) done	To know that number of times sFFU operations	40	4

	from the beginning of the device life time	were done on the device		
FW Release Date	Firmware Release date	To identify device Firmware	44	12
FW Release Time	Firmware Release hour	To identify device Firmware	56	8
Cumulative Host Write data size	Accumulate the amount of Host Written payload in resolution of 100MB	To analyze host total write payload and typical daily workload	64	4
Number Vcc Voltage Drops Occurrences	Cumulative counter for voltage drops (Power-Off) during all device states (Idle/Read/Write/Erase).	To identify unstable power supply platform behavior	68	4
Number Vcc Voltage Droops Occurrences	Counts the times VDET indication was triggered due to Power-Droop (Slight power-droop below certain threshold and for a very short period of time).	To identify unstable power supply platform behavior	72	4
Number of failures recover new host data (After Write Abort)	Count the number of times iNAND dismiss new Host data due to Write Abort (either due to corrupted data or broken) command	To analyze write abort behaver by device	76	4
Total Recovery Operation After VDET	The total amount of recovery operations required to be done by the device while detecting internal slight power-droop	To analyze device recovery after VDET event occurs	80	4
Cumulative SmartSLC write payload	Accumulate the amount of Host written payload that was written to SmartSLC buffer in resolution of 100MB	To Track and analyze iNAND SmartSLC behavior	84	4
Cumulative SmartSLC BigFile mode write payload	Accumulate the amount of Host written payload that was written to SmartSLC BigFile buffer in resolution of 100MB	To Track and analyze iNAND SmartSLC BigFile mode behavior	88	4
Number of times SmartSLC BigFile mode was operated during device lifetime	Count the number of times Host wrote payload to SmartSLC BigFile mode	To Track and analyze iNAND SmartSLC BigFile mode behavior	92	4
Average Erase Cycles of SmartSLC BigFile mode	The Average Erase count of SmartSLC BigFile buffer	To track and analyze iNAND SmartSLC BigFile mode behavior	96	4
Cumulative Initialization Count	Number of device power ups event from beginning of life	To analyze number of initialization events happened during device lifetime	100	4
Max Erase Cycles Type C (Enhanced)	The Maximum Erase value out of all enhanced Blocks	To Check product endurance variance	104	4
Max Erase Cycles Type A (SLC)	The Maximum Erase value out of all SLC Blocks	To Check product endurance variance	108	4
Max Erase Cycles Type B (TLC)	The Maximum Erase value out of all TLC Blocks	To Check product endurance variance	112	4
Min Erase Cycles Type C (Enhanced)	The Minimum Erase value out of all enhanced Blocks	To Check product endurance variance	116	4

Min Erase Cycles Type A (SLC)	The Minimum Erase value out of all SLC Blocks	To Check product endurance variance	120	4
Min Erase Cycles Type B (TLC)	The Minimum Erase value out of all TLC Blocks	To Check product endurance variance	124	4
Reserved			128-151	24
Pre EOL warning level Type C (Enhanced)	Pre end-of-life (EOL) levels for device enhanced area: 1 – Normal 2 – Warning 3 – Urgent 4 – Device at EOL and entered Read Only mode.	To predict early lifetime of device	152	4
Pre EOL warning level Type B (TLC)	Pre end-of-life (EOL) levels for device TLC area: 1 – Normal 2 – Warning 3 – Urgent 4 – Device at EOL and entered Read Only mode.	To predict early lifetime of device	156	4
Uncorrectable Error Correction Code	The amount of UECC by the device	To analyze UECC probability during real lifetime	160	4
Current temperature	Indicates the current temperature of the device, in degrees Celsius	To track device environmental status	164	4
Min Temperature	Indicates the min temperature recorded in the device, in degrees Celsius, throughout power cycles.	To track device environmental status	168	4
Max Temperature	Indicates the max temperature recorded in the device, in degrees Celsius, throughout power cycles.	To track device environmental status	172	4
Reserved			176	4
Enriched Device Health Type C (Enhanced)	Device health (age) Level in resolution of 1% (1-100) for Enhanced area	To check real life product endurance and lifetime	180	4
Enriched Device Health Type B (TLC)	Device health (age) Level in resolution of 1% (1-100) for TLC area	To check real life product endurance and lifetime	184	4
reserved			188-190	3
Current Power mode	Device internal power state (5 states: highest 4 – lowest 0)	To know internal device power/performance state	191	1
Enriched Device Health Type A (SLC)	Device health (age) Level in resolution of 1% for SLC area	To check real life product endurance and lifetime	192	4
Pre EOL warning level Type A (SLC)	Pre end-of-life (EOL) levels for SLC area: 1 – Normal 2 – Warning 3 – Urgent 4 – Device at EOL and entered Read Only mode.	To predict early lifetime of device	196	4

Power-Loss indications:

iNAND 7550 is also serving the host by notifying him on cases of Power-Loss events and internal handling of those events. A dedicated field in the EXT_CSD register was allocated to indicate the occurrence of Power Loss/Write Abort during the last power down. This field reports if a Power Loss was detected and recovered during the last power-up.
In order to retrieve this field, the host should issue CMD8 command – SEND_EXT_CSD. This command returns full EXT_CSD structure – 512 bytes as block of data. Following is the EXT_CSD field details:

Name	Field	Size (bytes)	Cell Type	Hex Offset	Dec. Offset
Power Loss indication	POWER_LOSS_REPORT	1	R	0x79	121

POWER_LOSS_REPORT[121] details:

- Bit[2]: RECOVERY_SUCCESS
  0x1: Recovery passed successfully
  0x0: Recovery failed
- Bit[1]: RECOVER_OLD_DATA
  0x1: Recovery to old copy of data
  0x0: No data recovery required
- Bit[0]: POWER_LOSS_DETECTED
  0x1: Unexpected Power Loss was detected - Detection is done during initialization, immediately after Power-Up

Note: In case Power Loss did not occur on last shut down, this register will show 0x00

Unstable Power-Supply indications:

In case of Flash voltage drop, the iNAND may not be able to recover the data that was already transferred to the iNAND device, but wasn't committed in the Flash. In this case the iNAND will "abort" the current host write and return back to the host with an error indication.

iNAND 7550 will use BIT19 and BIT20 (cc_error) in the command response to indicate VDET error status to the host. the VDET error indication can be seen only if CMD13 was issued, or in the next command response.

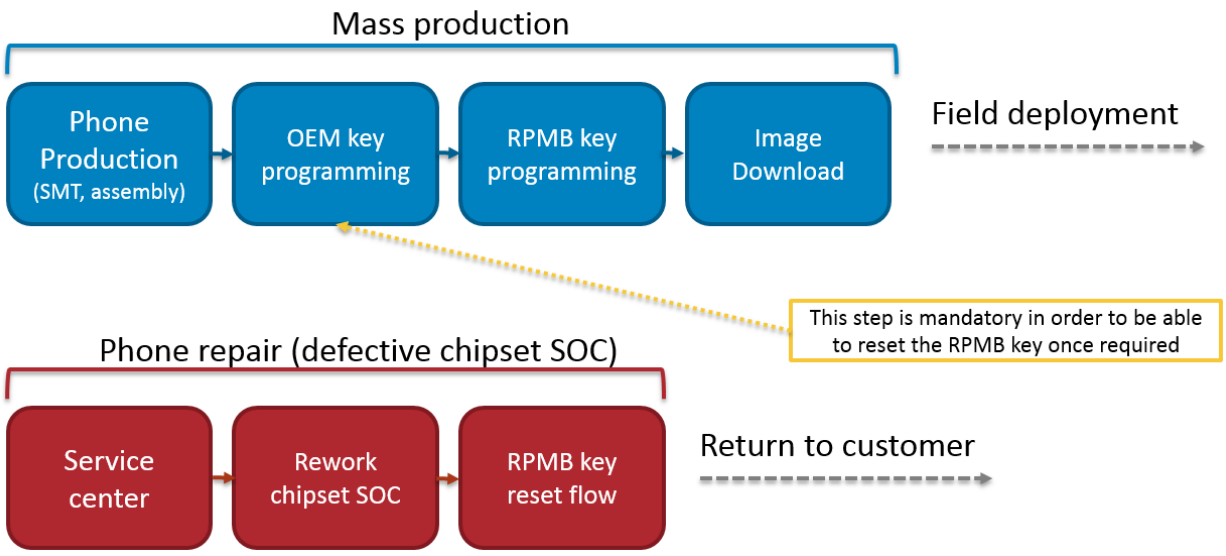
Examples:

- Open Mode (CMD25+CMD12+CMD13):
  In both cases, where the voltage droop occurs before or after CMD12:
  CMD12 response will not have BIT19 and BIT20 set.
  CMD13 will identify the error indication - BIT19 and BIT20 will be set in CMD13 response
  Note: The host may send many CMD13 and the BIT19 will be set only in first CMD13 after releasing the busy.
- Close Mode (CMD23+CMD25+CMD13):
  CMD13 will identify the error indication - BIT19 and BIT20 will be set in CMD13 response
- Single Block Mode (CMD24+CMD13):
  CMD13 will identify the error indication - BIT19 and BIT20 will be set in CMD13 response

Host shall retry latest command as long as the VDET error indication on CMD13 response (or next command response (BIT19 and BIT20 are set) is still set

7.4. RPMB Key Reset

iNAND Product line implements RPMB as specified by the eMMC specification ver. 5.1 (initially introduced in eMMC ver 4.4). RPMB is an eMMC partition – "Replay Protected Memory Block". RPMB is used by the host to store data for security purposes.
The host programs a key to the eMMC in a secure environment and uses this key to access the RPMB.
Writing to this partition can only be done by the host who programmed the RPMB key. Anyone can read the data but only the host with the key can write to it. Pairing between host and eMMC (programming the key) is done in a secure environment such as production line.
In cases where a phone is returned back to the OEM for repair and the host chipset is found defective, it would require replacement of both the host SOC and the eMMC chip
This is due to the fact that there is a unique key per SOC which is created by the SOC itself, so no one else besides the defective SOC knows what the key is.
Without a method to reset RPMB, the only way to repair a broken phone is highly expensive operation since it requires physical replacement of the memory with a new one (along with the chipset).
The new RPMB Key feature would be added to iNAND 7550 and that would offer a solution for the problem described above which will enable the OEM to reset the key once required. The feature obligates the OEM to program a unique OEM key which would later enable the use of the RPMB reset key function.



In case the OEM key is not programmed prior to the RPMB key, the Reset key function cannot be used.
The secure protocol relies on CMD62, CMD63 which are vendor specific, as well as CMD24.
The device holds a 512 bytes' status register which is updated on every command. The register contains the status of the last command as well as a counter that is needed for the protocol operation. The host may read this register at any time.

8. MARKING

First row: Simplified SanDisk Logo
Second row: Sales item P/N
Third row: Country of origin i.e. 'TAIWAN' or 'CHINA'
* No ES marking for product in mass production.
Fourth row: Y- Last digit of year
WW- Work week
D- A day within the week.
MTLLLXXX – Internal use
2D barcode: Store the 12 Digital unique ID information as reflected in the fourth row.

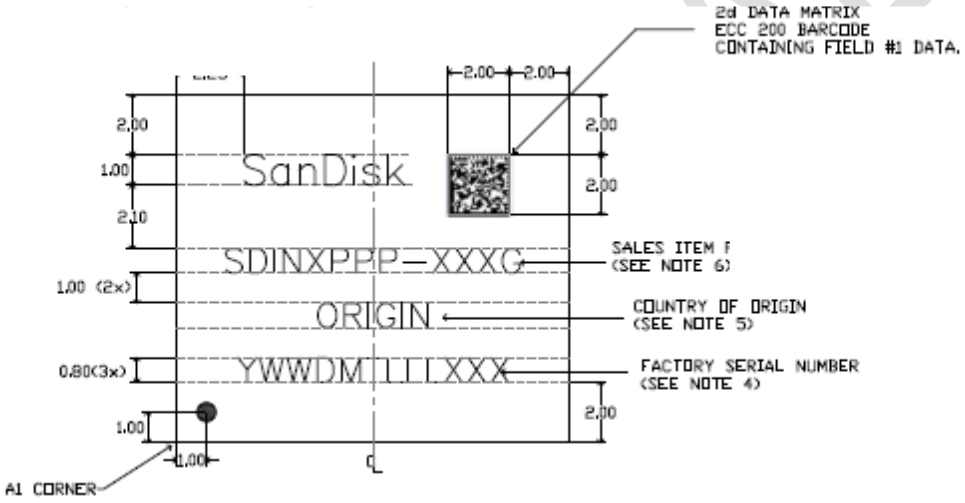


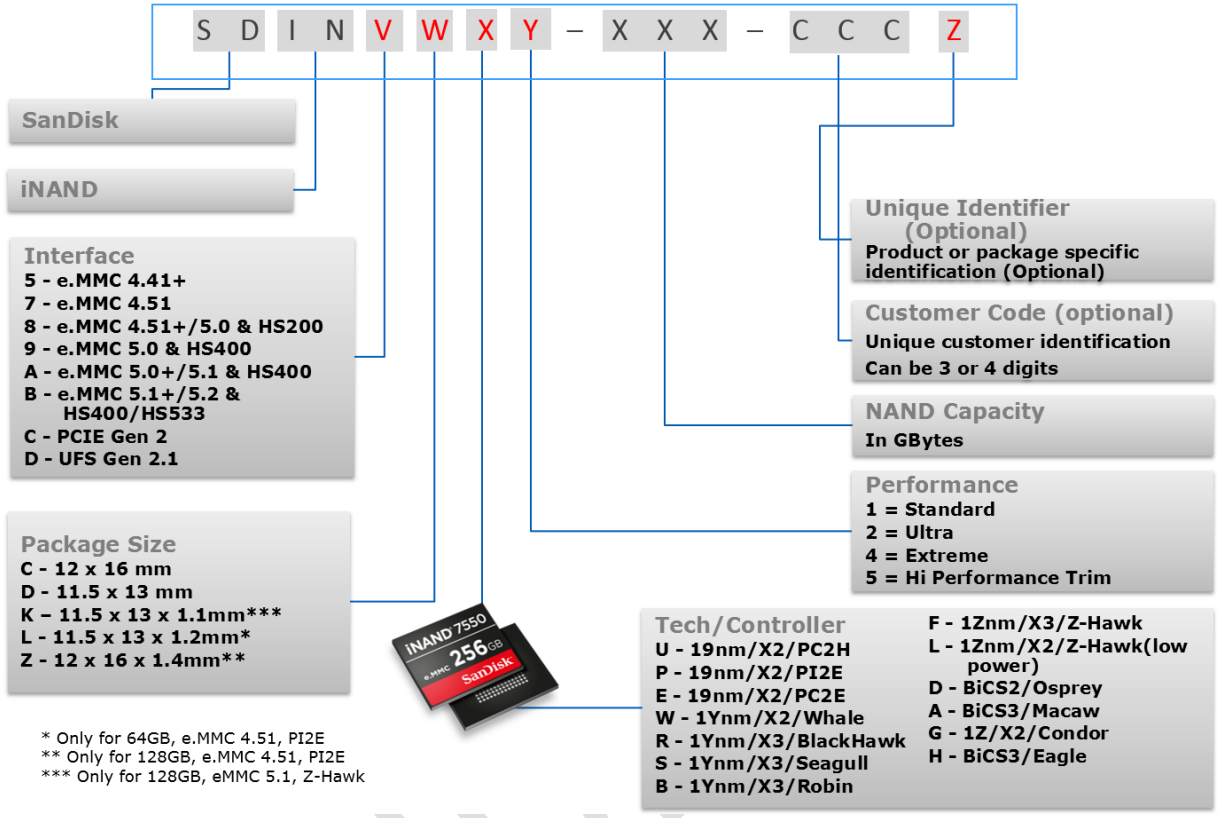
Figure 7 - Product marking 64G-256GB

9. ORDERING INFORMATION

Table 19 – Ordering Information

Capacity	Technology	Part Number	Package	e.MMC
32GB	3D-64L-X3	SDINBDA4-32G	11.5x13x1.0mm	5.1
64GB	3D-64L-X3	SDINBDA4-64G	11.5x13x1.0mm	5.1
128GB	3D-64L-X3	SDINBDA4-128G	11.5x13x1.0mm	5.1
256GB	3D-64L-X3	SDINBDA4-256G	11.5x13x1.0mm	5.1
32GB	3D-64L-X3	SDINBDA4-32-V	11.5x13x1.0mm	5.1
64GB	3D-64L-X3	SDINBDA4-64-V	11.5x13x1.0mm	5.1
128GB	3D-64L-X3	SDINBDA4-128-V	11.5x13x1.0mm	5.1
256GB	3D-64L-X3	SDINBDA4-256-V	11.5x13x1.0mm	5.1

iNAND Discrete Part Number Convention



Note1: **Customer Code** (optional) will be added at the end of the part number. The Customer Code can be 3 or 4 digits. Example:

Customer	Customer Code	Customer Part Number
Customer A	326	SDINBDA4-256-326
Customer B	473	SDINBDA4-64-473
Customer C	1243	SDINBDA4-128-1243

Note2: **Unique Identifier** (optional) is a single character identifier specifying certain FW/HW version. For example, the unique identifier (in this case, K) in SDINBDA4-128G-K specifies a certain FW version, while different unique identifier (in this case, N) in SDINBDA4-128G-N can specify a different FW version

HOW TO CONTACT US

Western Digital Technologies, Inc.
951 SanDisk Dr.
Milpitas, CA 95035-7933
Phone: +1-408-801-1000
OEMProducts@SanDisk.com

Please refer to SanDisk's web site for contact information:
www.sandisk.com