LMK00301 Evaluation Board User Guide

National Semiconductor Corporation
User Guide
20 September 2011

General Description

This user guide describes how to set up and operate the LMK00301 evaluation board kit (EVK). The LMK00301 is a 3-GHz, 10-output differential fanout buffer intended for high-frequency, low-additive jitter clock/data distribution and level translation. The EVK enables the user to verify the functionality and performance specifications of the device. Refer to the LMK00301 datasheet for the functional description and specifications of the device.

Features

- Low-noise clock fan-out via two banks of five differential outputs and one LVCMOS output
- Selectable differential output type (LVPECL, LVDS, HCSL, or Hi-Z)
- 3:1 input multiplexer with two universal input buffers and one crystal oscillator interface
- DIP switch control of device configuration
- Single 3.3 V or dual 3.3 V/2.5 V operation using onboard LDO regulators or direct supply inputs
- Flexible input and output interface with controlled-impedance traces and edge SMA connectors

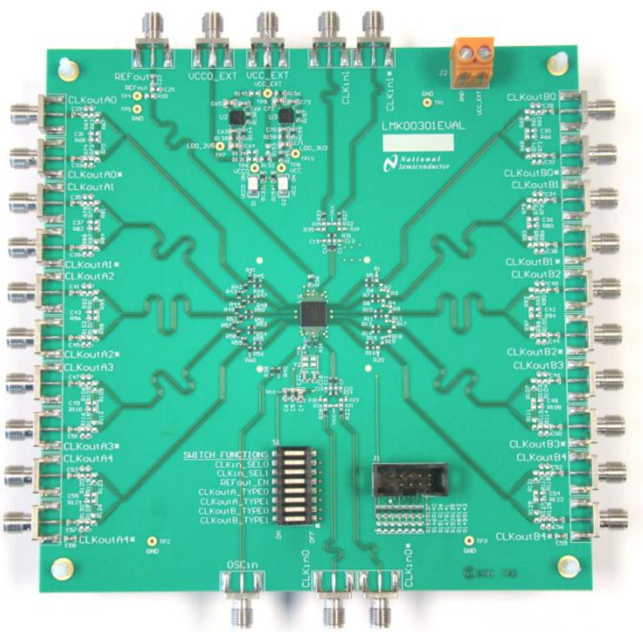

Figure 1. LMK00301 Evaluation Board Photo

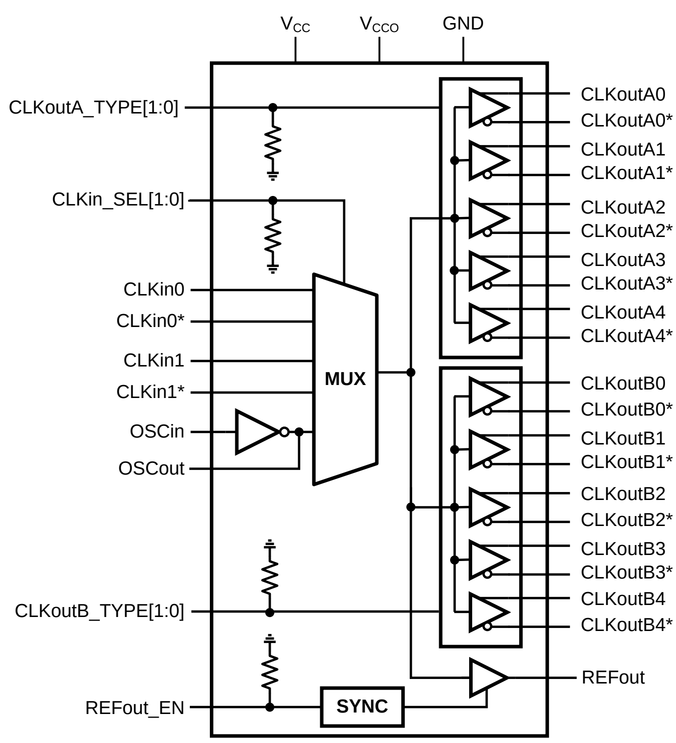

Figure 2. LMK00301 Functional Block Diagram

Contents

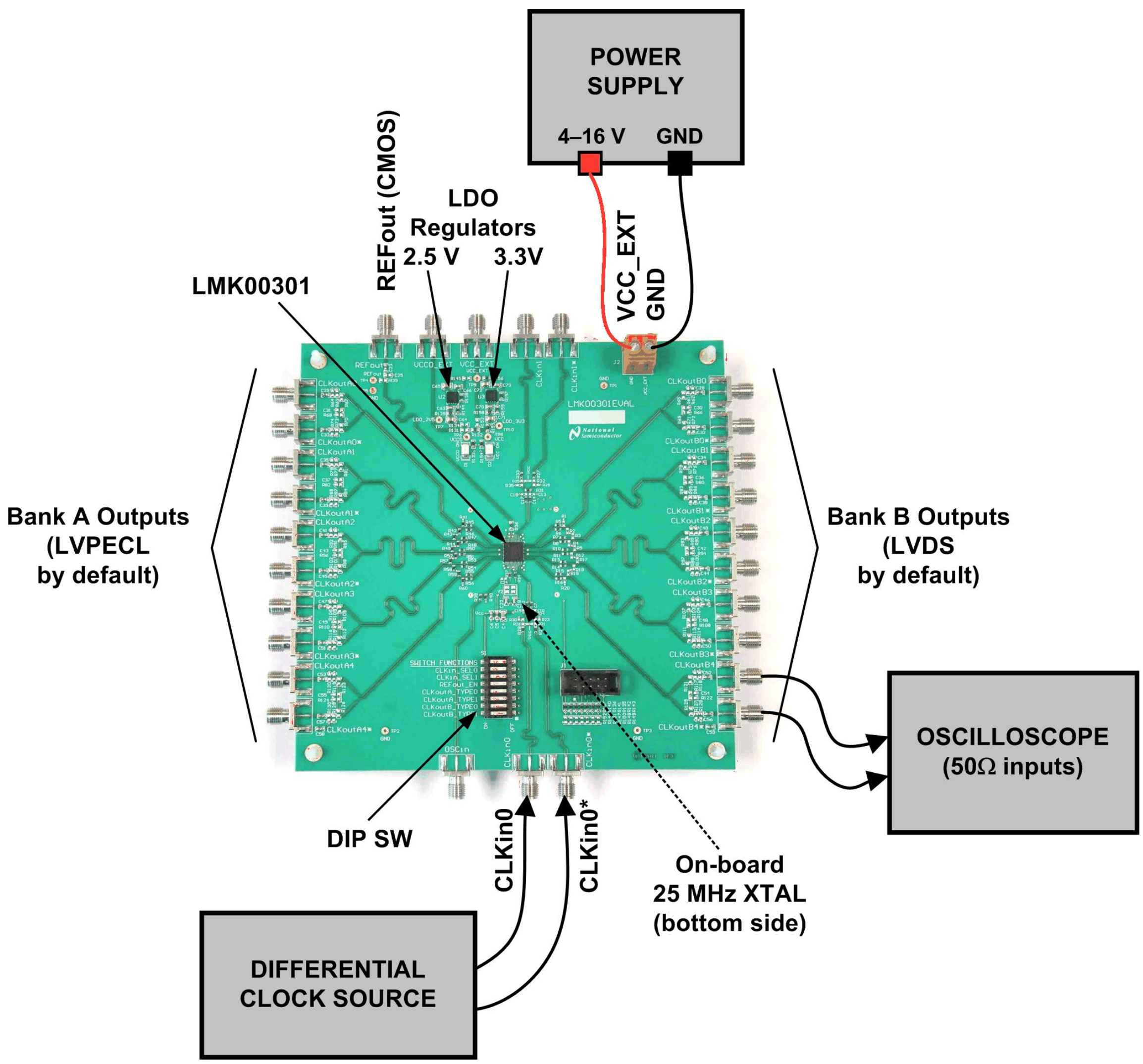

Figure 3. LMK00301 Evaluation Board Quick Start Setup

Evaluation Board Quick Start

To quickly set up and operate the board with basic equipment, refer to the quick start procedure below and test setup shown in Figure 2.

1. Verify the output mode control switches, S1[1:5], match the states shown in Table 1 to reflect the default output clock interfaces configured on the EVK.

Table 1. Default Clock Output Modes / Interfaces

SW Position/Name	SW State	Default Clock Output Modes
S1[1] / CLKoutB_Type1	0 (OFF)	Bank B outputs are LVDS
S1[2] / CLKoutB_Type0	1 (ON)	
S1[3] / CLKoutA_Type1	0 (OFF)	Bank A outputs are LVPECL
S1[4] / CLKoutA_Type0	0 (OFF)	
S1[5] / REFout_EN	1 (ON)	REFout enabled

2. Connect the VCC_EXT and GND leads from the board to a 4 V - 16 V source. This powers an onboard LDO regulator that provides 3.3 V to VCC and VCCO supplies of the IC. Both VCC & VCCO status LED should be lit green when ON.
3. Set the desired clock input using the input selection control switches, S1[6:7], per Table 2. The onboard 25 MHz crystal (Y1) is selected by default, so an external clock source is not required. A differential clock source can be connected to SMAs **CLKin0/0*** or **CLKin1/1***.

Table 2. Input Selection (0=SW OFF, 1=SW ON)

Selected Input	Default Input Mode	S1[6] CLKin_Sel1 State	S1[7] CLKin_Sel0 State
CLKin0/0*	Differential clock	0	0
CLKin1/1*	Differential clock	0	1
OSCin	25 MHz XTAL onboard	1	Don't care

CLKin0/0* and CLKin1/1* paths are configured by default to receive a differential clock as the input. The SMA inputs are DC coupled to the device inputs and terminated with 100 ohms differential. Refer to the Clock Inputs section to configure the EVK for a single-ended input.

4. Connect and measure any clock output SMA labeled **CLKoutX#/X#*** or **REFout** to an oscilloscope or other test instrument using SMA cable(s). The output clock will be level-translated/buffered copy of the selected clock input or crystal oscillator. Note: All output clocks are AC-coupled to the SMA connectors to ensure safe use with RF instruments.

Note: Leaving a driven output(s) without proper load termination can cause signal reflections on the board, which can couple onto nearby outputs and result in degraded signal quality and erroneous measurements. To minimize these effects, be sure to properly terminate any unused output path using an SMA load or solder termination resistors on the loading options near the edges of the board. Another option is to disconnect the unused output pin from the trace by removing the series 0-ohm resistor. An unused output bank may also be disabled using the output mode control switch.

Signal Path and Control Switches

The LMK00301 supports single-ended or differential clocks on CLKin0 and CLKin1. A third input, OSCin, has an integrated crystal oscillator interface that supports a fundamental mode, AT-cut crystal or an external single-ended clock. The three-input multiplexer is pin-controlled. To achieve the maximum operating frequency and lowest additive jitter, it is recommended to use a differential clock with high input slew rate (>3 V/ns) and DC-coupling to either CLKin0 or CLKin1 port.

The device provides up to 10 differential outputs split between Bank A and Bank B, where each bank has a pin-controlled output mode (LVPECL, LVDS, HCSL, or Hi-Z). An additional output, REFout, has a fixed LVCMOS buffer with output enable input.

All control pins are configured with the control switch, S1. The input selection logic is shown in Table 2. The Bank A and Bank B output mode selection logic are shown in Table 3 and Table 4. The REFout enable logic is shown in Table 5.

Table 3. Bank A Output Mode Selection (0=OFF, 1=ON)

Bank A Output Mode	S1[3] CLKoutA_Type1 State	S1[4] CLKoutA_Type0 State
LVPECL	0	0
LVDS	0	1
HCSL	1	0
Disabled/Hi-Z	1	1

Table 4. Bank B Output Mode Selection (0=OFF, 1=ON)

Bank B Output Mode	S1[2] CLKoutA_Type1 State	S1[1] CLKoutA_Type0 State
LVPECL	0	0
LVDS	0	1
HCSL	1	0
Disabled/Hi-Z	1	1

Table 5. REFout Enable Selection (0=OFF, 1=ON)

REFout Enable Mode	S1[5] REFout_EN State
Disabled/Hi-Z	0
Enabled	1

Power Supplies

The power supply section on the EVK provides flexibility to power the device using the onboard LDO regulator(s) or direct supply input(s). A combination of 0-ohm resistor options allows the user to modify the EVK power supply configuration, if desired.

By default, 3.3 V (VCC and VCCO) is supplied by one of the onboard LDO regulators, U1. To power the regulator, connect a 4 V – 16 V input voltage and ground from an external power source to the terminal block, J2, or SMA input labeled **VCC_EXT**.

To modify the EVK with a different power supply configuration, populate the resistor options as shown in Table 6. Then, apply the appropriate voltage(s) to the EVK power input(s).

If the EVK is configured for dual external input supplies, connect the 2.5 V input voltage and ground from another external power source to the SMA input labeled **VCCO_EXT**.

Decoupling capacitors and 0-ohm resistor footprints, which can accommodate ferrite beads, can be used to isolate the EVK power input(s) from the device power pins.

Table 6. EVK Power Supply Configuration Options

	Single LDO 3.3 V (Default)	Single Ext. Input 3.3 V	Dual LDO 3.3 V / 2.5 V	Dual Ext. Inputs 3.3 V / 2.5 V
VCC_EXT input	Apply 4 V – 16 V	Apply 3.3 V ± 5%	Apply 4 V – 16 V	Apply 3.3 V ± 5%
VCCO_EXT input	Not used	Not used	Not used	Apply 2.5 V ± 5%
U2 output (VCCO)	Not used	Not used	2.5 V	Not used
U3 output (VCC)	3.3 V (VCC & VCCO)	Not used	3.3 V	Not used
R131	DNP	DNP	DNP	0
R132	0	0	DNP	0
R134	DNP	DNP	0	DNP
R145	DNP	DNP	0	DNP
R153	DNP	0	DNP	0
R155	0	DNP	0	DNP

R156	0	DNP	0	DNP

Clock Inputs

The SMA inputs labeled **CLKin0** & **CLKin0*** and **CLKin1** & **CLKin1*** can be configured to receive a differential clock or single-ended clock. Best performance is achieved with a DC-coupled differential input clock, which is the default configuration for both CLKin ports.

Both CLKin0 and CLKin1 paths include footprint options (0603 size) to provide the user with flexibility in configuring the termination, biasing, and coupling for the device inputs.

Configuring CLKinX for a Single-Ended Input

To configure a single-ended clock input on CLKin0, follow the steps below. CLKin1 can be modified similarly.

1. Remove R24 (100 ohm differential termination).
2. Terminate CLKin0 (driven input) by installing 51 ohms on R30.
3. Bias CLKin0*(non-driven input) with a reference voltage near the common-mode voltage of the CLKin0 signal using R21 and R23 to form a voltage divider from VCC.
4. Install 0.1 uF on C10 as a bypass capacitor.

For example, if CLKin0 will be driven by single-ended LVPECL signal with a common-mode voltage of 2 V, then R21 and R23 can be 1.0 kohm and 1.5 kohm, respectively.

Crystal Oscillator Interface

The LMK00301 has an integrated crystal oscillator interface (OSCin/OSCout) that supports a fundamental mode, AT-cut crystal. If the crystal input is selected, the onboard XTAL on either footprint Y1 or Y2 will start-up and the oscillator clock can be measured on any enabled output.

By default, a 25.000 MHz XTAL is populated on Y1, which uses a HC49 footprint on the bottom side of the PCB.

Alternatively, a 3.2 x 2.5 mm XTAL can be populated on Y2, located on the top side. Only one XTAL footprint should be used at a time.

The external load capacitor values of C18 and C22 (C_{EXT}) depend on the specified load capacitance (C_L) for the crystal, as well as the device's OSCin input capacitance (C_{IN} = 1 pF typical) and the PCB stray capacitance (C_{STRAY} = 1 pF). The selected 25 MHz crystal is specified for C_L of 18 pF. Assuming equal external load capacitor values for optimum symmetry, C_{EXT} can be calculated as follows:

$$C_{EXT} = (C_L - C_{IN} - C_{STRAY}) * 2$$
$$C_{EXT} = (18\text{ pF} - 1\text{ pF} - 1\text{ pF}) * 2$$
$$C_{EXT} \sim 33\text{ pF (nearest standard value)}$$

To limit crystal power dissipation, a 1 kΩ resistor is placed between the OSCout pin and the crystal.

Configuring OSCin for a Single-Ended Input

To configure a single-ended clock input on OSCin, remove R34 and R37 to disconnect the crystal. Install 0.1 uF on C24 to provide an AC-coupled path from the SMA input labeled **OSCin** to the device input, which is biased internally. Note that the OSCin path is includes a 51-Ω termination on R40.

Clock Outputs

By default, Bank A outputs are configured for LVPECL mode and source-terminated with 240 ohm resistors and AC coupled to the SMA connectors labeled **CLKoutA#** and **CLKoutA#***. Bank B outputs are configured for LVDS mode and AC coupled to the output SMA connectors labeled **CLKoutB#** and **CLKoutB#***. REFout is a LVCMOS output and is AC coupled to its SMA connector. Footprint options (0603 size) provide flexibility to configure the output termination, biasing, and coupling to the destination. To modify the output interface for a different output mode, refer to the modifications provided in the Schematic section.

As noted earlier, all outputs should be properly terminated, or else disconnected via the 0-ohm resistor or disabled using the output control switch.

LVPECL and LVCMOS Outputs at 2.5 V VCCO

The LVPECL and LVCMOS output levels depend on the VCCO voltage, as specified in the datasheet.

When VCCO is 2.5 V and an output (bank) is configured for LVPECL mode, it is suggested to use a lower-valued source-termination resistor to ground, such as 91 Ω, to maintain proper DC bias current on each output.

Schematics

See the following pages.

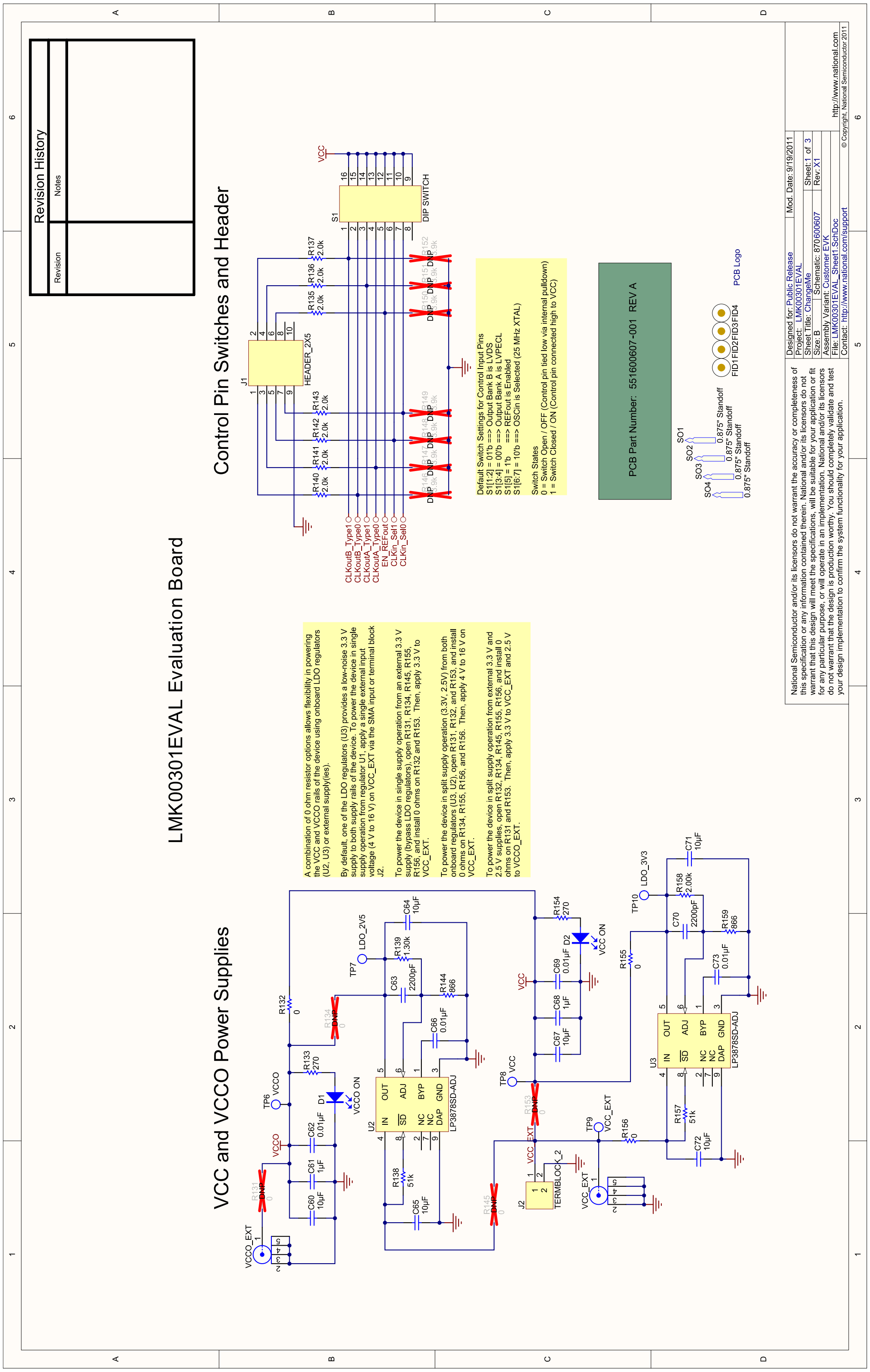

Figure 4. Schematic Sheet #1

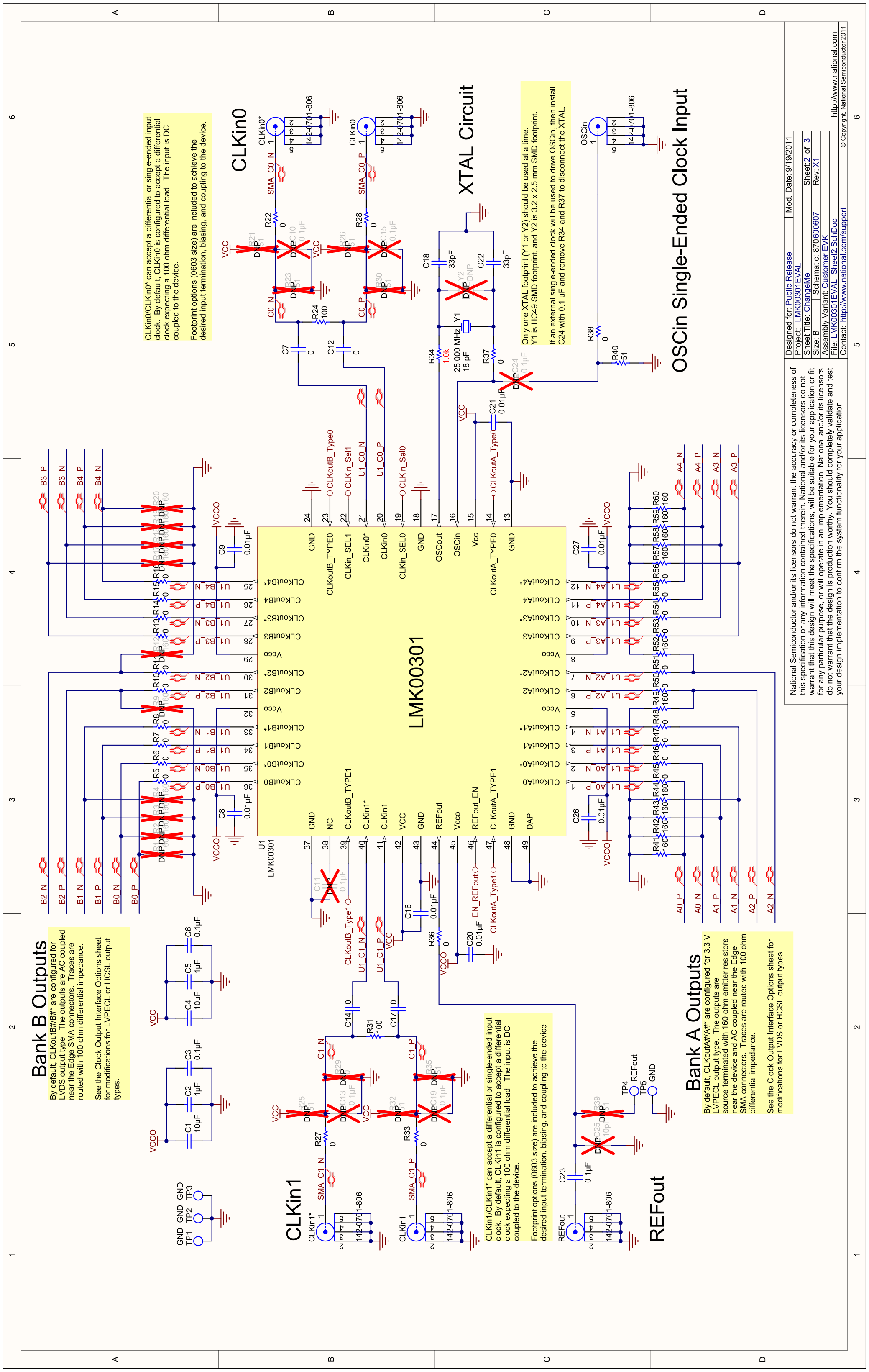

Figure 5. Schematic Sheet #2

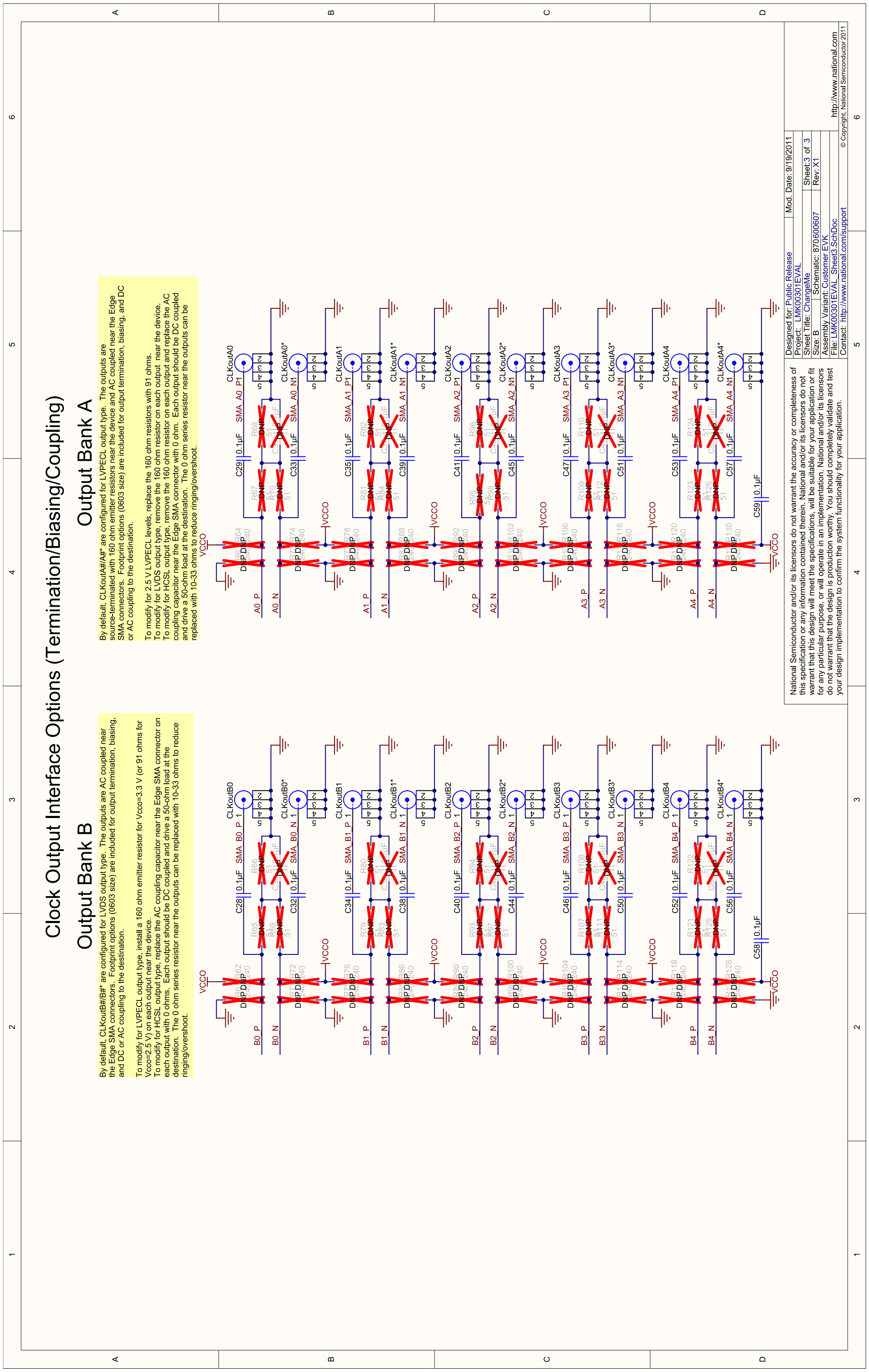

Figure 6. Schematic Sheet #3

PCB Layout

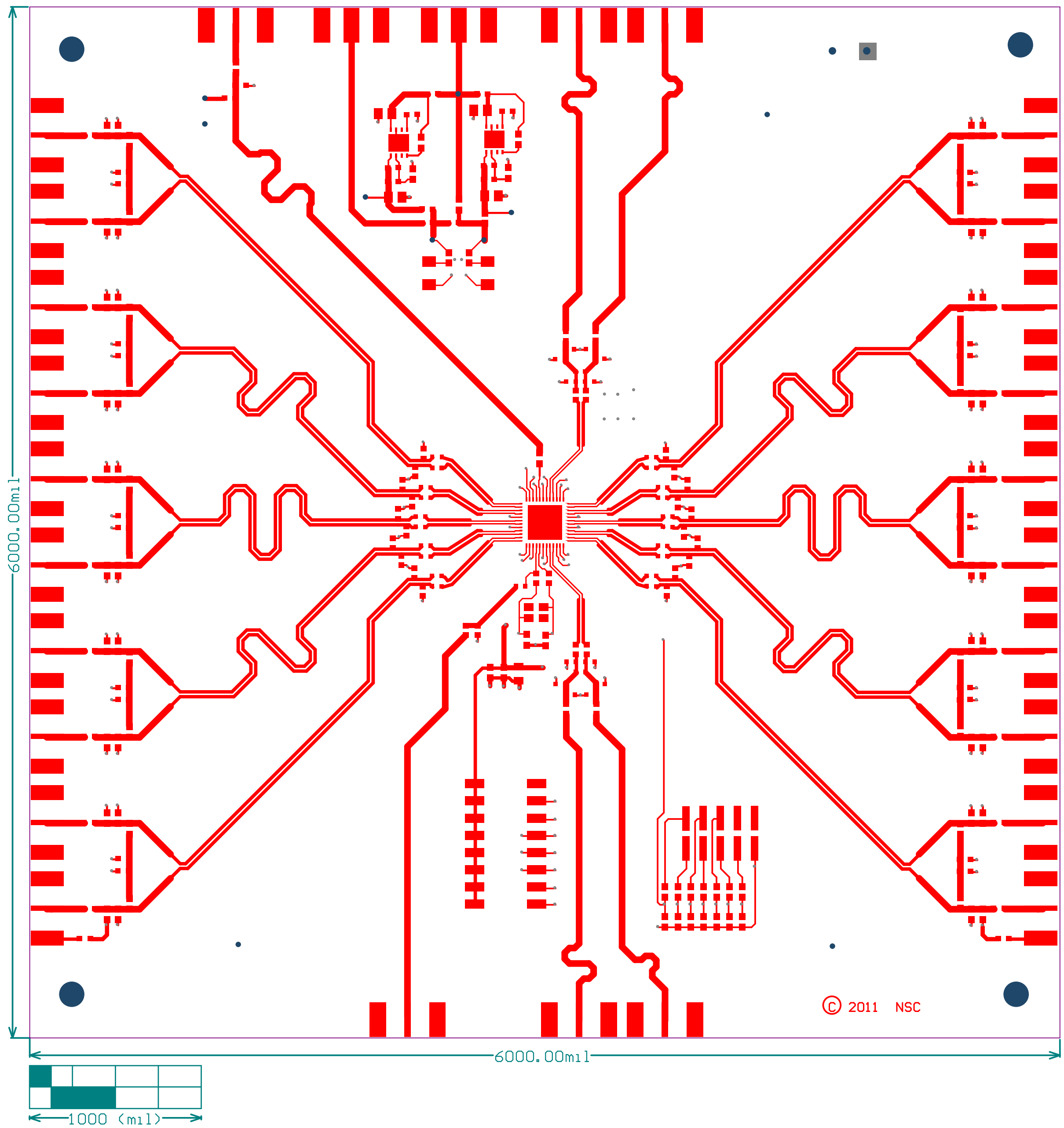

Figure 7. Top Side, Layer #1 (Not to scale)

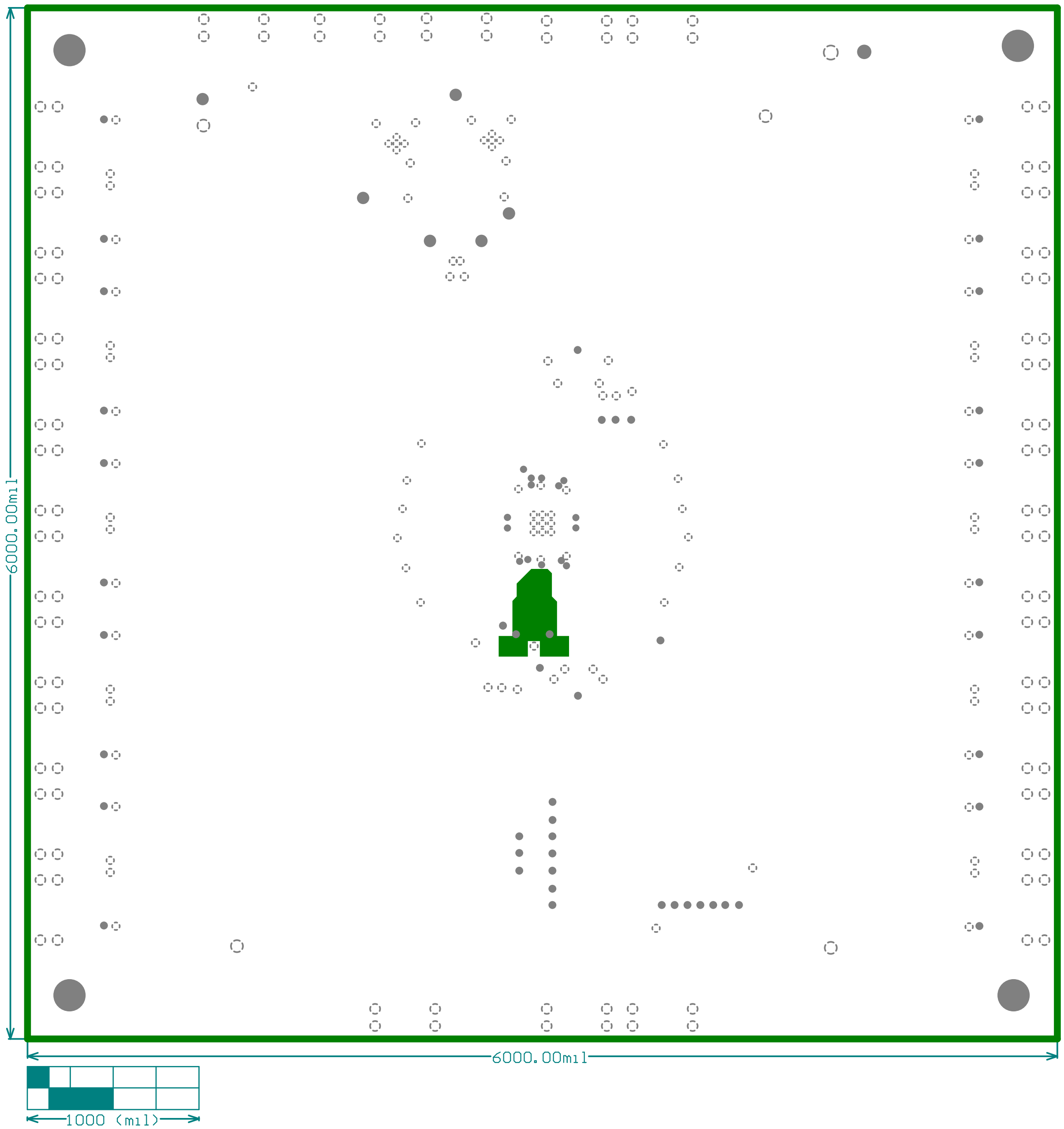

Figure 8. Internal Ground Plane, Layer #2 (Layer Inverted, Not to scale)

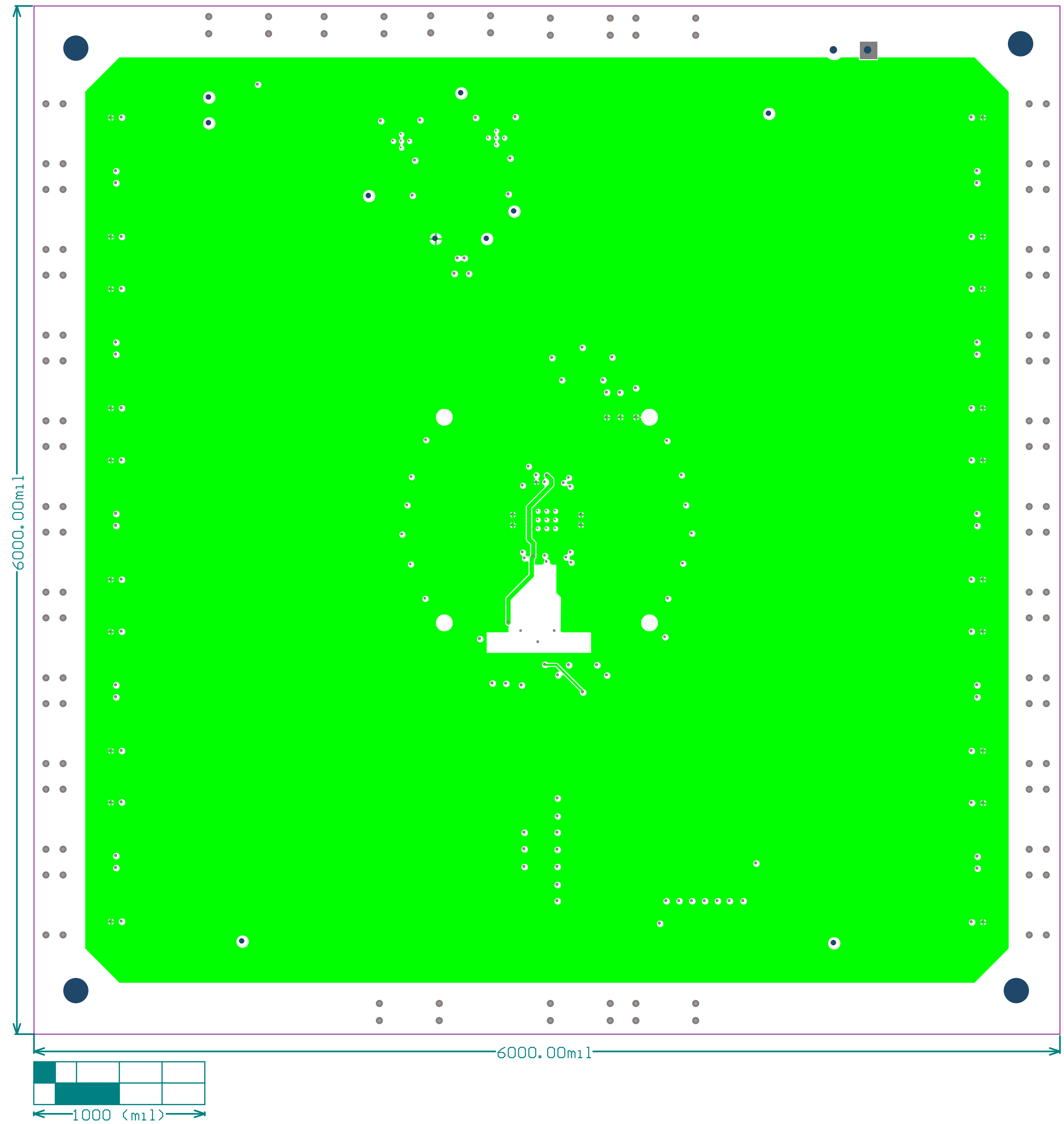

Figure 9. Internal Power Plane, Layer #3 (Not to scale)

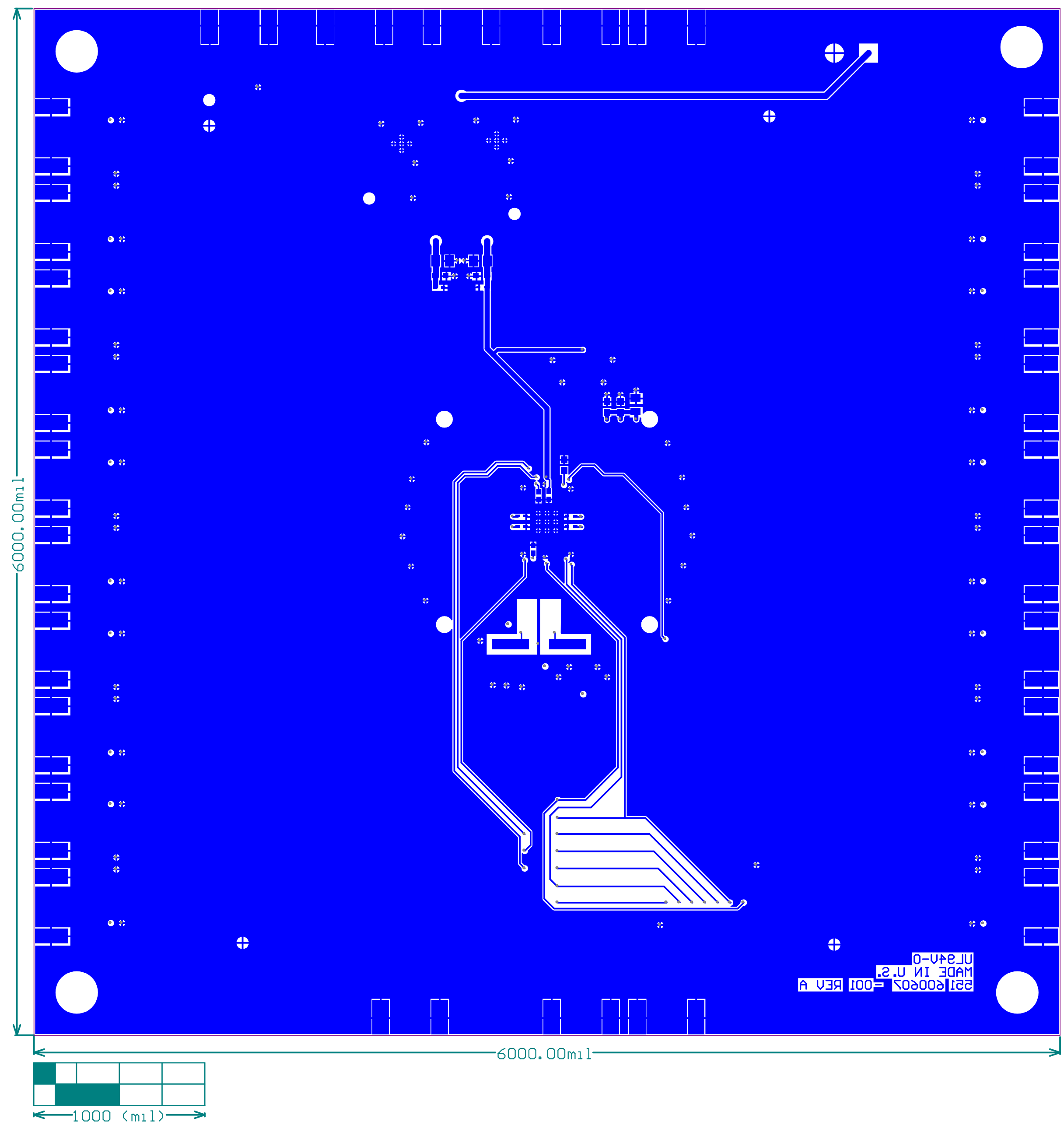

Figure 10. Bottom Side, Layer #4 (Top view, Not to scale)

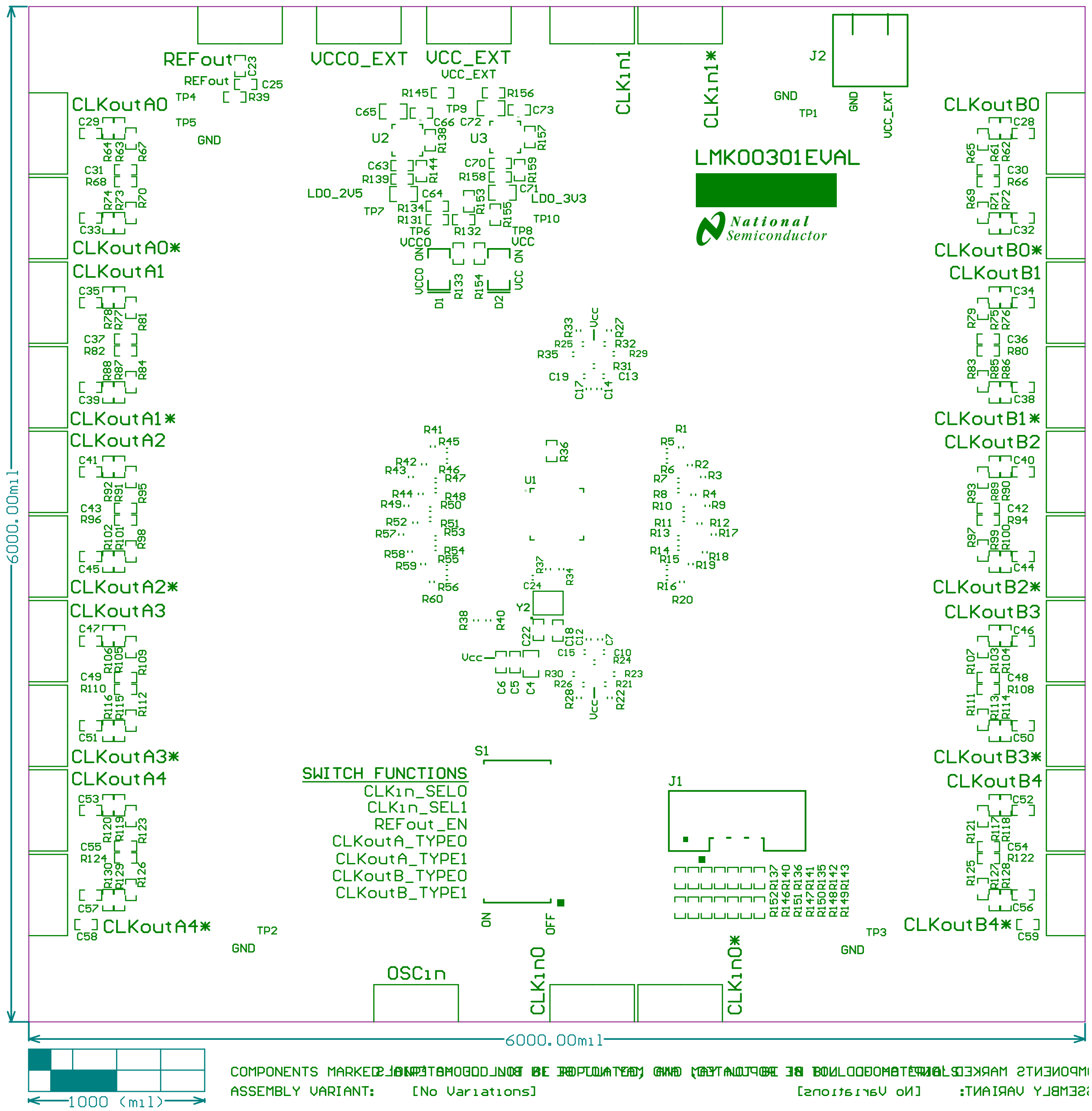

Figure 11. Top Silkscreen (Not to scale)

Figure 12. Bottom Silkscreen (Top view, Not to scale)

Bill of Materials

Item	Designator	Description	Manufacturer	Part Number	Qty
1	AA1	Printed Circuit Board		LMK00301EVAL	1
2	C1, C4, C60, C64, C65, C67, C71, C72	CAP, CERM, 10uF, 10V, +/-10%, X5R, 0805	MuRata	GRM21BR61A106KE19L	8
3	C2, C5, C61, C68	CAP, CERM, 1uF, 16V, +/-10%, X7R, 0603	TDK	C1608X7R1C105K	4
4	C3, C6, C23, C28, C29, C32, C33, C34, C35, C38, C39, C40, C41, C44, C45, C46, C47, C50, C51, C52, C53, C56, C57, C58, C59	CAP, CERM, 0.1uF, 16V, +/-10%, X7R, 0603	TDK	C1608X7R1C104K	25
5	C7, C12, C14, C17, R5, R6, R7, R8, R10, R11, R13, R14, R15, R16, R22, R27, R28, R33, R36, R37, R38, R45, R46, R47, R48, R50, R51, R53, R54, R55, R56, R132, R155, R156	RES, 0 ohm, 5%, 0.1W, 0603	Vishay-Dale	CRCW06030000Z0EA	34
6	C8, C9, C16, C20, C21, C26, C27, C62, C69	CAP, CERM, 0.01uF, 16V, +/-10%, X7R, 0402	TDK	C1005X7R1C103K	9
7	C18, C22	CAP, CERM, 33pF, 50V, +/-5%, C0G/NP0, 0603	MuRata	GRM1885C1H330JA01D	2
8	C63, C70	CAP, CERM, 2200pF, 100V, +/-5%, X7R, 0603	AVX	06031C222JAT2A	2
9	C66, C73	CAP, CERM, 0.01uF, 25V, +/-5%, C0G/NP0, 0603	TDK	C1608C0G1E103J	2

10	CLKin0, CLKin0*, CLKin1, CLKin1*, CLKoutA0, CLKoutA0*, CLKoutA1, CLKoutA1*, CLKoutA2, CLKoutA2*, CLKoutA3, CLKoutA3*, CLKoutA4, CLKoutA4*, CLKoutB0, CLKoutB0*, CLKoutB1, CLKoutB1*, CLKoutB2, CLKoutB2*, CLKoutB3, CLKoutB3*, CLKoutB4, CLKoutB4*, OSCin, REFout, VCC_EXT, VCCO_EXT	Connector, SMT, End launch SMA 50 ohm	Emerson Network Power	142-0701-806	28
11	D1, D2	LED 2.8X3.2MM 565NM GRN CLR SMD	Lumex Opto/Components Inc.	SML-LX2832GC	2
12	FID1, FID2, FID3, FID4	Fiducial mark. There is nothing to buy or mount.	N/A	N/A	4
13	J1	Low Profile Vertical Header 2x5 0.100"	FCI	52601-G10-8LF	1
14	J2	CONN TERM BLK PCB 5.08MM 2POS OR	Weidmuller	1594540000	1
15	R24, R31	RES, 100 ohm, 5%, 0.1W, 0603	Vishay-Dale	CRCW0603100RJNEA	2
16	R34	RES, 1.0k ohm, 5%, 0.1W, 0603	Vishay-Dale	CRCW06031K00JNEA	1
17	R40	RES, 51 ohm, 5%, 0.1W, 0603	Vishay-Dale	CRCW060351R0JNEA	1
18	R41, R42, R43, R44, R49, R52, R57, R58, R59, R60	RES, 160 ohm, 5%, 0.1W, 0603	Vishay-Dale	CRCW0603160RJNEA	10
19	R133, R154	RES, 270 ohm, 5%, 0.1W, 0603	Vishay-Dale	CRCW0603270RJNEA	2
20	R135, R136, R137, R140, R141, R142, R143	RES, 2.0k ohm, 5%, 0.1W, 0603	Vishay-Dale	CRCW06032K00JNEA	7
21	R138, R157	RES, 51k ohm, 5%, 0.1W, 0603	Vishay-Dale	CRCW060351K0JNEA	2
22	R139	RES, 1.30k ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW06031K30FKEA	1

23	R144, R159	RES, 866 ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW0603866RFKEA	2
24	R158	RES, 2.00k ohm, 1%, 0.1W, 0603	Vishay-Dale	CRCW06032K00FKEA	1
25	S1	SWITCH DIP ROCKER 8POS SMD	Tyco	GDR08S04	1
26	SO1, SO2, SO3, SO4	0.875" Standoff	VOLTREX	SPCS-14	4
27	U1	High-Performance Differential Fanout Buffer	National Semiconductor	LMK00301	1
28	U2, U3	Micropower 800mA Low Noise 'Ceramic Stable' Adjustable Voltage Regulator for 1V to 5V Applications, 8-pin LLP	National Semiconductor	LP3878SD-ADJ	2
29	Y1	CRYSTAL 25.000 MHZ 18PF SMD	Abracon Corporation	ABLS-25.000MHZ-B4-F-T	1
30	C10, C11, C13, C15, C19, C24, C30, C31, C36, C37, C42, C43, C48, C49, C54, C55	DNP			0
31	C25	DNP			0
32	R1, R2, R3, R4, R9, R12, R17, R18, R19, R20	DNP			0
33	R21, R23, R25, R26, R30, R32, R35, R39, R65, R66, R67, R68, R69, R70, R79, R80, R81, R82, R83, R84, R93, R94, R95, R96, R97, R98, R107, R108, R109, R110, R111, R112, R121, R122, R123, R124, R125, R126	DNP			0
34	R29, R131, R134, R145, R153	DNP			0

35	R61, R62, R63, R64, R71, R72, R73, R74, R75, R76, R77, R78, R85, R86, R87, R88, R89, R90, R91, R92, R99, R100, R101, R102, R103, R104, R105, R106, R113, R114, R115, R116, R117, R118, R119, R120, R127, R128, R129, R130	DNP			0
36	R146, R147, R148, R149, R150, R151, R152	DNP			0
37	Y2	DNP			0
38	VCC_EXT	Banana plug, Red	Emerson	108-0302-001	1
39	GND	Banana plug, Black	Emerson	108-0303-001	1

IMPORTANT NOTICE

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Wireless Connectivity	www.ti.com/wirelessconnectivity		
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