Application Note AN-49
LinkSwitch™-PH Family

Design Guide

Introduction

The LinkSwitch-PH family of devices are highly integrated monolithic switching ICs optimized to provide an isolated, dimmable (up 1000:1), high power factor (PF), constant current driver for LED lighting applications at output powers of up to 50 W. LinkSwitch-PH reduces circuit complexity by integrating the MOSFET and controller plus eliminating the optocoupler and all secondary side feedback components.

Each member of the family has a high-voltage power MOSFET and its controller integrated onto the same die. The continuous conduction mode (CCM), variable duty cycle, constant frequency operation provides both high power factor (>0.9), compliance to IEC 6100-3-2 Class C and D harmonic current limits, high efficiency and reduced EMI filtering requirements. Primary side switching current is internally sensed eliminating external current sense resistors. Internal start-up bias current is drawn from a high-voltage current source connected to the DRAIN pin, eliminating the need for external start-up components. The internal oscillator is frequency modulated (jitter) to reduce EMI. In addition, the ICs have integrated functions that provide system-level protection. The auto-restart function limits dissipation in the device, the transformer and the output diode during overload, output short-circuit and open-loop conditions, while the auto-recovering hysteretic thermal shutdown function disables MOSFET switching during a thermal fault.

Basic Circuit Configuration

The circuit in Figure 1 shows the basic configuration of a standard AC TRIAC dimmable LED driver using LinkSwitch-PH. The circuit uses the flyback topology and with the high level integration of LinkSwitch-PH devices, far fewer design issues are left to be addressed externally, resulting in one common circuit configuration for all output specifications. For example, different output power levels may require different values for some circuit components, but the circuit configuration stays unchanged.

Scope

This application note is intended for engineers designing an isolated AC-DC LED driver using the LinkSwitch-PH family of devices. It provides guidelines to enable an engineer to quickly select key components and also complete a suitable transformer design. To simplify the task, this application note refers directly to the PIXIs design spreadsheet that is part of the PI Expert™ design software suite.

In addition to this application note the reader may also find the product Reference Design Kits (RDKs) useful. These contain a prototype board, a link to an engineering report that contains complete design information and test data and product samples. Further details on downloading PI Expert, RDKs and updates to this document can be found at www.powerint.com.

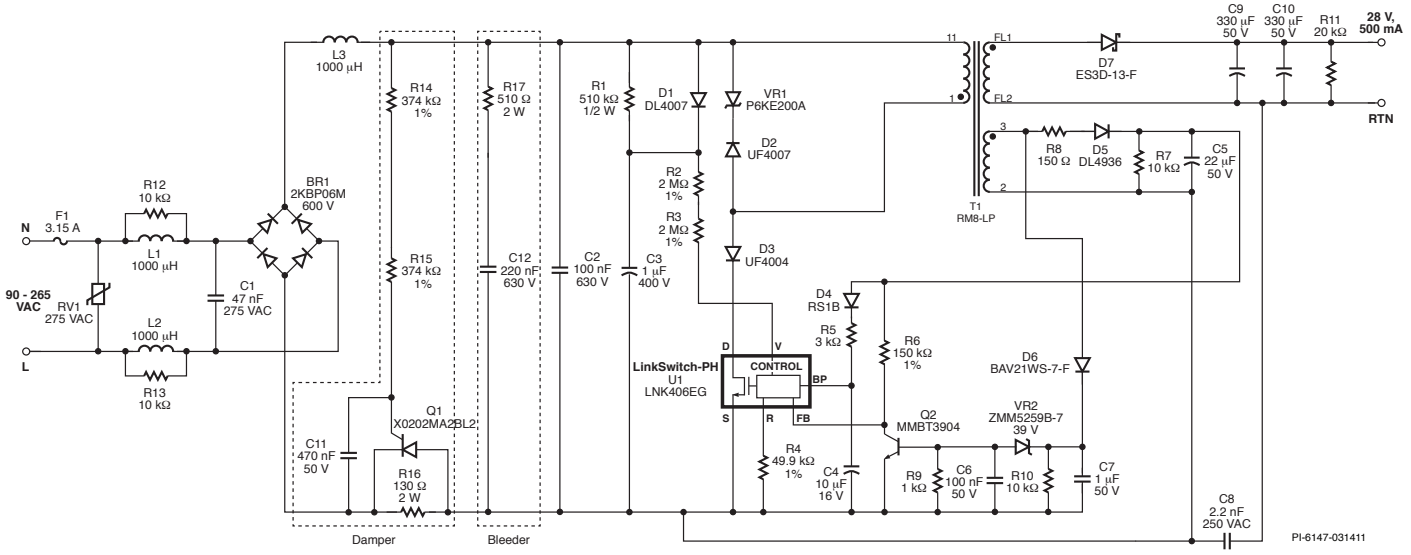


Figure 1. Typical Circuit Example (RD-195) for a Dimmable LED Driver using a LinkSwitch-PH Device.

Quick Start

Readers who want to start immediately can use the following information to quickly design the transformer and select the components for a first prototype. Only the information described below needs to be entered into the PIXIs spreadsheet, other parameters will be automatically selected based on a typical design. References to spreadsheet cell locations are provided in square brackets [cell reference].

- Select either TRIAC dimming (YES) or non-dimming/PMW dimming (NO) configuration [B3]. For TRIAC dimming the value of the R pin resistor (R4 in Figure 1) is 49.9 kΩ, 1% and for non-dimming 24.9 kΩ, 1%.
- Enter AC input voltage range VAC_{MIN}, VAC_{MAX} and minimum line frequency f_L [B4, B5, B6] based on Table 1.
- Enter nominal output (LED string) voltage V_O [B7], maximum output voltage $V_{O(MAX)}$ [B8] and minimum output voltage $V_{O(MIN)}$ [B9]. Ratio of $V_{O(MAX)}/V_{O(MIN)}$ should be less than ≤ 1.66 (V_O ±25%).
- Enter the nominal output (LED string) current I_O [B11].
- Enter efficiency estimate η [B13] based on Table 2.
- Select LinkSwitch-PH device from the drop down list or enter directly [B18]. Use Table 3 for guidance based on input voltage and output power. Where a choice between two devices exists it is recommended to select the larger device and operate in reduced current limit mode for higher efficiency.
- Select the device Current Limit Mode operating mode that will be used. Enter [B20] either reduced (RED) or full (FULL). Reduced is recommended for maximum efficiency (smallest enclosure size and heat sinking) e.g. A19 retro-fit lamp applications.
- Enter V_D [B32], the forward voltage of the expected output diode. Use 0.5 V for Schottky barrier types and 0.8 V for PN types.
- Enter the desired core type from the drop down menu or directly [B46]. Entering Auto will select a core size suitable for the specified output power. If the desired core is not listed, then you may enter a core's characteristics A_E, L_E and A_L ([B48], [B49], [B50]). Enter in the bobbin width BW [B51].
- If margin tape is required (non triple insulated wire, isolated output design), then enter the margin tape width in [B52]. Note: This will reduce the winding width by two times the margin tape width entered. For 230 VAC applications a value of 3.2 mm is typical and for 100 VAC / 115 VAC use 2 mm. In practice triple insulated wire is used in most isolated designs to minimize the size of the transformer due to limited space.
- Verify that the core's gap L_G [D78], the wire gauge AWG [D83] and the primary's winding current density CMA [D85] are within acceptable limits. Follow the guidance provided in column F to achieve this.
- Once all warning and errors have been addressed click on the Transformer Parameter and Transformer Construction tabs to obtain detailed transformer specification and construction details. These can be used to either construct the transformer in house or send to an external magnetic vendor.
- Using PIV_S [D101] and I_O [B11] determine the proper output rectifier. Select a diode with a voltage (V_{RRM}) rating >PIV_S and current rating >I_O with a recommendation of ≥2 × I_O for higher efficiency.
- The value of I_{RIPPLE} [D92] and $V_{O(MAX)}$ [D8] should be used to select the appropriate output capacitor. The selected capacitor should have a ripple current rating >I_{RIPPLE} and voltage rating >$V_{O(MAX)}$.
- The value of the V pin resistor (R_V) and if used the second lower V pin resistor (R_{V2}) are provided in cells [D27] and [D28]. A value for R_{V2} >10 MΩ indicates that it is not required.
- The value of the R pin resistor (R4 in Figure 1) programs TRIAC dimming or non-dimming. The value for the feedback resistor (R_{FB1}) is given in cell [D30]. This is the resistor connected from the FEEDBACK pin to the bias supply and is used to sense the output voltage.
- Using I_{AVG} [E64] determine the required input filter inductor current rating.
- If necessary, the output current can be fine tuned. After the first prototype is built and running, enter the output current in cells [B111] and [B112] at line voltages [B109] and [B110], new values for R_V and R_{V2} are then calculated [B113], [B114]. With these values adjusted measure and enter values for the bias voltage V_{B1} and V_{B2} [B121], [B122] and associated output current I_{O1} and I_{O2} [B123], [B124]. An adjusted value for R_{FB1} and R_{FB2} [D125], [D126] (if needed) will be calculated.

Step-by-Step Design Procedure

Step 1. Enter Application Variables (Figure 3): Dimming, VAC_{MIN}, VAC_{MAX}, f_L, V_O, $V_{O(MAX)}$, $V_{O(MIN)}$, V_{OVP}, I_O, η, V_B

Dimming Required [B3]: YES, NO
Enter YES, if the driver is to be used with TRIAC phase angle based AC dimmers else enter NO (including for PWM dimming). This input determines the configuration of the V pin and R pin resistors. The value of the R pin resistor configures the part into either (TRIAC) dimming mode or normal mode. Dimming mode reduces the amount of input line voltage compensation to improve the dimming range obtained with TRIAC based phase angle dimmers. In this mode the output current regulation is maintained within narrow limits only over a single input voltage range (e.g. 90 VAC - 132 VAC, or 185 VAC - 265 VAC). Below this input range the output current will reduce (equivalent to reduced conduction angle of a TRIAC dimmer) and above this range the output current will increase.

The normal (non-dimming) mode provides input line voltage compensation that maintains output current regulation within narrow limits (<±10%) across universal input voltage ranges (e.g. 90 VAC – 265 VAC). This mode does not prevent the device from being used with AC phase dimmers however dimming range is reduced (10:1). Control range is also reduced as no reduction in output current occurs until the phase conduction angle reduces below 90 degrees hence as the dimmer control is adjusted little change in the output current will occur for ~50% of the knob or slider range . Figure 2 shows a summary of the expected output current regulation performance versus line voltage between the two operating modes.

Input Voltage and Line Frequency, VAC_{MIN} [B4], VAC_{MAX} [B4], f_L
Select the input voltage and line frequency from Table 1. For TRIAC dimming designs a single input voltage specification is preferred as this allows greater design optimization. For example a single input 100 VAC / 115 VAC versus a universal input

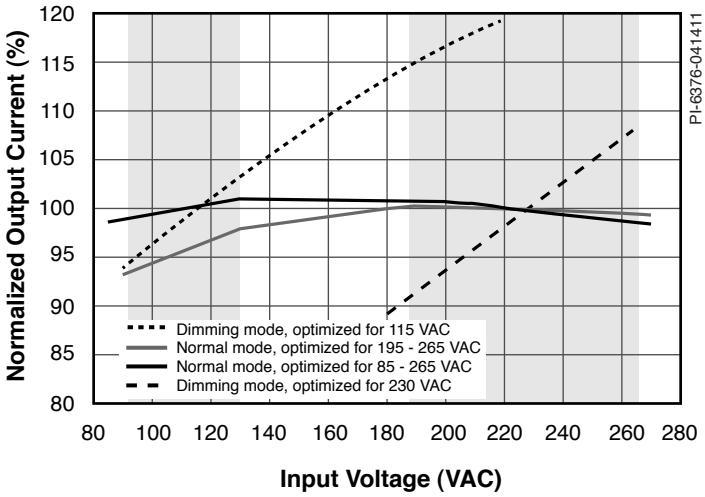


Figure 2. Comparison of Output Current Regulation in Dimming and Normal Modes Versus Line Voltage. Shaded Areas Represent Typical Single Input Voltage Operating Ranges (90-132 VAC and 195-265 VAC).

design requires lower voltage components, smaller safety spacing requirements and reduced TRIAC bleeder current. This allows the design to offer smaller size, lower cost, broader TRIAC compatibility and higher overall efficiency. For non TRIAC dimming specifications there is no efficiency benefit for a single input line voltage specification. This is due to the elimination of the damper and bleeder networks in non-dimming designs. However the component rating, size and safety spacing benefits still apply for a single low-line vs. a universal input specification.

Nominal Output Voltage [B7], V_O (V)

Enter the nominal output voltage of the LED string to be driven. LinkSwitch-PH based drivers are optimized to cover an output voltage range of 2:1. Higher output voltages result in higher overall efficiency due to a reduction in secondary diode and winding losses. Figure 4 shows an example of this effect for a non TRIAC dimmable 14 W output, 100 VAC / 115 VAC input design using an RM8 core size for the transformer.

For a TRIAC dimmable design the values would reduce by ~3% due to the losses in the TRIAC compatibility damper and bleeder circuit blocks.

Maximum Output Voltage [B8], $V_{O(MAX)}$ (V)

Enter the maximum LED string voltage to be driven including tolerance. If left blank a value of 1.1 × V_O is assumed.

Nominal Input Voltage (VAC)	Minimum Line Voltage (VAC_{MIN})	Maximum Line Voltage (VAC_{MAX})	Nominal Line Frequency ($f_{L(NOM)}$) (Hz)	Notes
100/115	85	132	50	VAC_{MIN}, $f_{L(NOM)}$: Japan VAC_{MAX}: USA
230/240	195	264	50	Europe/rest of world
208/277	177	320	60	Lighting in commercial buildings in USA, (208 VAC phase to phase)
Universal	85	264	50	VAC_{MIN}, $f_{L(NOM)}$: Japan VAC_{MAX}: Europe/rest of world

Table 1. Standard Worldwide Input Line Voltages and Line Frequencies.

Nominal Output Power (W)	Efficiency Estimate (%)			
	TRIAC Dimming		Non TRIAC Dimming	
	V_O ≤12 V	V_O >12 V	V_O ≤12 V	V_O >12 V
≤3	45	55	55	65
3-6	65	77	78	82
6-10	76	78	80	83
10-20	82	85	85	88
>20	83	86	86	89

Table 2. Initial Efficiency Estimates for a New Design.

Output Power Table

Product	R_V = 2 MΩ		R_V = 4 MΩ	
	85-132 VAC		85-308 VAC	
	Minimum Output Power	Maximum Output Power	Minimum Output Power	Maximum Output Power
LNK403/413EG	2.5 W	4.5 W	6.5 W	12 W
LNK404/414EG	2.5 W	5.5 W	6.5 W	15 W
LNK405/415EG	3.8 W	7.0 W	8.5 W	18 W
LNK406/416EG	4.5 W	8.0 W	10 W	22 W
LNK407/417EG	5.5 W	10 W	12 W	25 W
LNK408/418EG	6.8 W	13.5 W	16 W	35 W
LNK409/419EG	8.0 W	20 W	18 W	50 W

Table 3. Device Family Power Table for Initial Device Selection.

ENTER APPLICATION VARIABLES					AN49 Example
Dimming required	YES	*Info*	YES		!!! Info. When configured for dimming, best output current line regulation is achieved over a single input voltage range.
VACMIN	90		90	V	Minimum AC Input Voltage
VACMAX	265		265	V	Maximum AC input voltage
fL			50	Hz	AC Mains Frequency
VO	28			V	Typical output voltage of LED string at full load
VO_MAX			30.8	V	Maximum expected LED string Voltage.
VO_MIN			25.2	V	Minimum expected LED string Voltage.
V_OVP			33.88	V	Over-voltage protection setpoint
IO	0.5				Typical full load LED current
PO			14	W	Output Power
n			0.8		Estimated efficiency of operation
VB			25	V	Bias Voltage

Figure 3. Application Variables Section of the Design Spreadsheet.

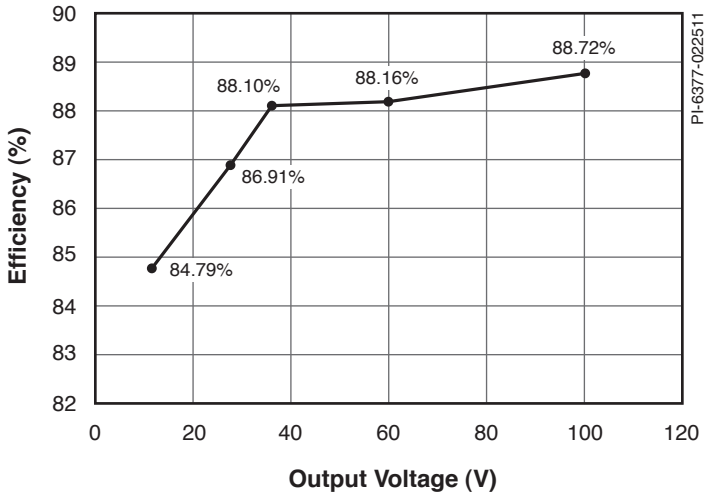


Figure 4. Effect of Output Voltage on Efficiency, Measured on 5 Designs (14 W, RM8 Core Size, Non-dimming Design Measured at 115 VAC).

Minimum Output Voltage [B9], $V_{O(MIN)}$ (V)
Enter the minimum LED string voltage. If left blank a value of $0.9 \times V_O$ is assumed.

Nominal Output Current [B11], I_O (A)
Enter the nominal output current the LED string is to be driven with.

Nominal Output Power [D12], P_O (W)
The calculated nominal output power.

Power Supply Efficiency [B13], η
Enter the estimated efficiency of the complete power supply measured at the output terminals under full load conditions and worst-case line (generally lowest input voltage). Initial values are provided in Table 2. Measure the efficiency of the first prototype-board at nominal output power and both VAC_{MIN} and VAC_{MAX} if the measured efficiency is lower than estimated then enter the measured value and refine the transformer design.

Bias Voltage, V_B (V)
This entry determines the output voltage from the bias winding. For non TRIAC dimming designs a value of 20 V is recommended and 25 V where TRIAC dimming is required. The higher voltage ensures adequate voltage to supply the IC at the minimum LED string voltage and with a TRIAC dimmer at minimum conduction angle (<30 degrees).

Step 2. Enter LinkSwitch-PH Variables (Device Size, Current Limit Mode, R Pin Resistor, V Pin Resistor (R_V), FEEDBACK Pin Current I_{FB}, Drain to Source Voltage (V_{DS}), Output Forward Voltage (V_D), and Bias Diode Forward Voltage (V_{DB})

Device Selection [B18] and Current Limit Mode [B19]
Select a LinkSwitch-PH device based on the output power using Table 3 for guidance.

For thermally challenging designs, e.g. incandescent lamp replacement, where either the ambient temperature local to the LinkSwitch-PH device is high and/or there is minimal space for heat sinking use the minimum output power column and select the reduced current limit mode by entering RED.

For open frame designs or designs where space is available for heat sinking then select from the maximum output power column and select the full current limit mode by entering FULL.

The current limit mode selection defines the value of the BYPASS pin capacitor: 10 µF for reduced and 100 µF for full current limit mode.

The recommended maximum operating device temperature under worst-case conditions (input line and external product ambient temperature) is 100 °C for the tightest output current distribution over production, and 115 °C to provide adequate design margin and ensure thermal shutdown is not triggered.

Upper V Pin Resistor Value [B27], R_V, MΩ (Entry Optional)
If left blank a default value of 4 MΩ is used for dimming designs and 3.909 MΩ for non-dimming. In conjunction with the lower V pin resistor (R_{V2}) these values provide the best output current regulation for non-dimming and without R_{V2}, the widest dimming range in dimmable applications.

ENTER LinkSwitch-PH VARIABLES					
LinkSwitch-PH	**LNK406**			Universal	115 Doubled/230V
Chosen Device		LNK406	Power Out	22.5W	22.5W
Current Limit Mode	**RED**		RED		Select "RED" for reduced Current Limit mode or "FULL" for Full current limit mode
ILIMITMIN			1.19	A	Minimum current limit
ILIMITMAX			1.36	A	Maximum current limit
fS			66000	Hz	Switching Frequency
fSmin			62000	Hz	Minimum Switching Frequency
fSmax			70000	Hz	Maximum Switching Frequency
IV			39.9	uA	V pin current
RV			4	M-ohms	Upper V pin resistor
RV2			1.00E+12	M-ohms	Lower V pin resistor
IFB			155.7	uA	FB pin current (85 uA < IFB < 210 uA)
RFB1			141.3	k-ohms	FB pin resistor
VDS			10	V	LinkSwitch-PH on-state Drain to Source Voltage
VD	0.5			V	Output Winding Diode Forward Voltage Drop (0.5 V for Schottky and 0.8 V for PN diode)
VDB	0.7			V	Bias Winding Diode Forward Voltage Drop

Figure 5. LinkSwitch-PH Variables Section of the Design Spreadsheet.

In Figure 1 R_V is made up of the series connection of R2 and R3. 1% or better tolerance should be used to obtain the narrowest output current tolerance. The voltage stress equals the peak of the AC line voltage so an equivalent rating of 500 V is recommended for high-line or universal input specifications 500 V rating is recommended, or two 250 V rated resistors in series.

Care should be taken when placing the V pin resistor(s) on the PCB to avoid noise coupling from the DRAIN node. In designs where encapsulation (potting) is used leakage currents and noise coupling may cause changes in V pin current post potting. This effect can be minimized again by careful layout and/or the addition of a 100 nF capacitor connected from the VOLTAGE pin to SOURCE pin. Place the capacitor as close to the device as possible and return directly to the SOURCE pin rather than via any other source connected nodes.

R Pin Resistor Value

This component is not included in the design spreadsheet as it is selected from one of two values. The value of the R pin resistor is determined based on whether TRIAC dimming is required. For TRIAC dimming select a value 49.9 kΩ and for non (TRIAC) dimming 24.9 kΩ. When configured for dimming the UV threshold is lowered and line compensation of output current reduced. This reduces dimmer dead band and increases the dimming range (>100:1). In the non-dimming configuration the UV threshold and the line compensation of the output current maintain tight regulation across a universal input voltage range.

FEEDBACK Pin Current, I_{FB}, μA (Optional)

If left blank a calculated value is used. The calculation depends on the value of the R pin resistor (dimming or non dimming configuration) and the value of V_{OR}. I_{FB} is used to regulate the output current and must be in the range of 85 μA to 210 μA under normal operating conditions including variation in the LED string voltage. Therefore to maximize the allowable output voltage variation and give smallest output current variation a value of 150 μA is idea allowing an LED string voltage variation of up to 2:1, ($V_{O(MAX)}$:$V_{O(MIN)}$). In practice most designs have a smaller output voltage variation and any value in the range 110 μA to 170 μA is acceptable.

Feedback Resistor Value, R_{FB1}, kΩ

This is the calculated value for the resistor connected to the FEEDBACK pin from the bias winding output to give the value of I_{FB} at the nominal output voltage (V_O).

LinkSwitch-PH Device ON-State Drain to Source Voltage, V_{DS}, V (Optional)

This parameter is the average ON state voltage developed across the DRAIN and SOURCE pins of LinkSwitch-PH. By default, if the grey override cell is left empty, a value of 10 V is assumed. Use the default value if no better data is available.

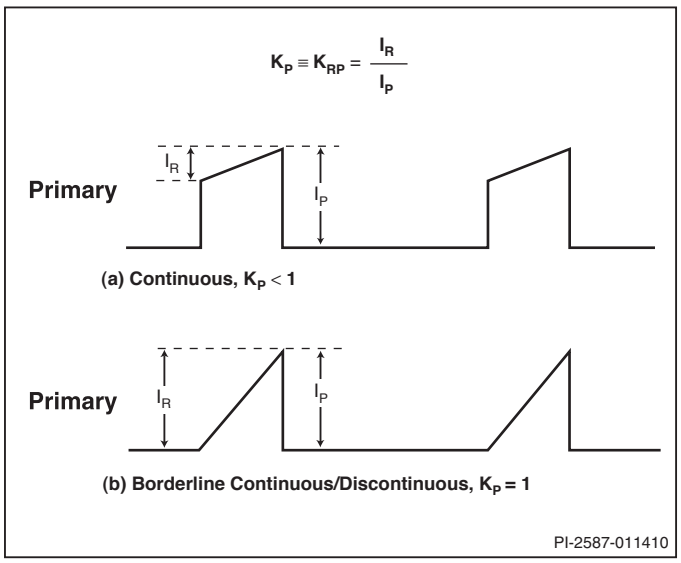


Figure 7. Continuous Conduction Mode Current Waveform (K_P<1) Showing Definition of K_P.

Output Diode Forward Voltage Drop, V_D, V

Enter the average forward drop for the output diode used. A value of 0.5 V is recommended for a Schottky diode and 0.8 V for a PN Ultrafast diode.

Bias Winding Forward Voltage Drop, V_D, V

Enter the average forward drop for the bias winding output diode. Use 0.7 V for a PN diode.

Step 3. Enter Key Design Variables: Ripple to Peak Current Ratio (K_P), Reflected Output Voltage (V_{OR})

Ripple to Peak Current Ratio (K_P)

Figure 7a shows K_P < 1, indicating continuous conduction mode, K_P is the ratio of ripple to peak primary current. LinkSwitch-PH devices require that the design operates in continuous conduction mode to achieve high power factor. The recommended range for the value of K_P is $0.4 \le K_P \le 0.9$. For reference a K_P value of <0.7 is gives a PF >0.95 and THD <20% while a design with a K_P of 0.9 gives PF >0.9 with THD <30%. Both PF and THD values are at the worst case of 230 VAC. At lower power levels higher K_P values may be used to trade smaller transformer core size against lower PF and efficiency. By default a value of 0.8 for P_O ≤25 W and 0.4 for P_O >25 W is used. For reference Figure 8 shows the measured effect of K_P on PF in a universal input, 28 V, 14 W output design.

Key Design Parameters					
KP			0.8		Ripple to Peak Current Ratio (For PF > 0.9, 0.4 < KP < 0.9)
LP			1246	uH	Primary Inductance
VOR			80	V	Reflected Output Voltage.
Expected IO (average)			0.51	A	Expected Average Output Current
KP_VACMAX			1.02		Expected ripple current ratio at VACMAX
TON_MIN			1.94	us	Minimum on time at maximum AC input voltage
PCLAMP			0.12	W	Estimated dissipation in primary clamp

Figure 6. Key Design Variables Section of the Design Spreadsheet.

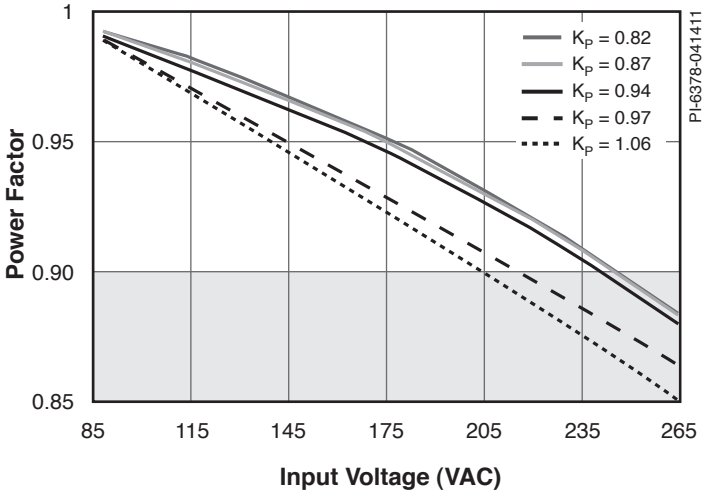


Figure 8. Illustration of the Impact of the Design Parameter K_P on PF.

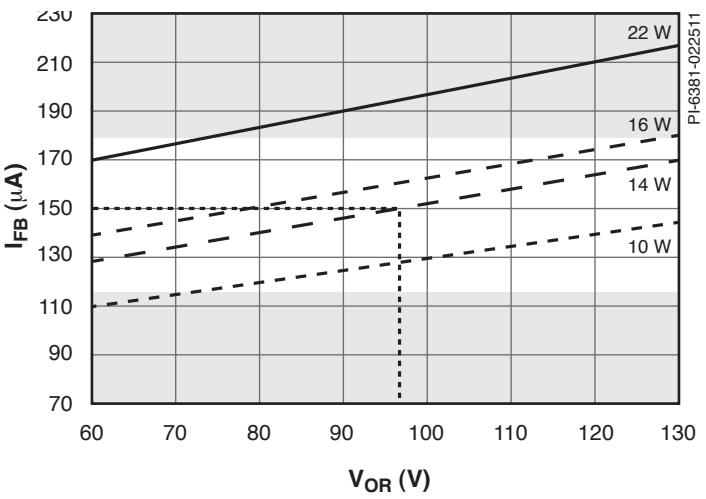


Figure 10. Example of Selecting V_{OR} for a Universal Input, 14 W Design Using LNK406EG.

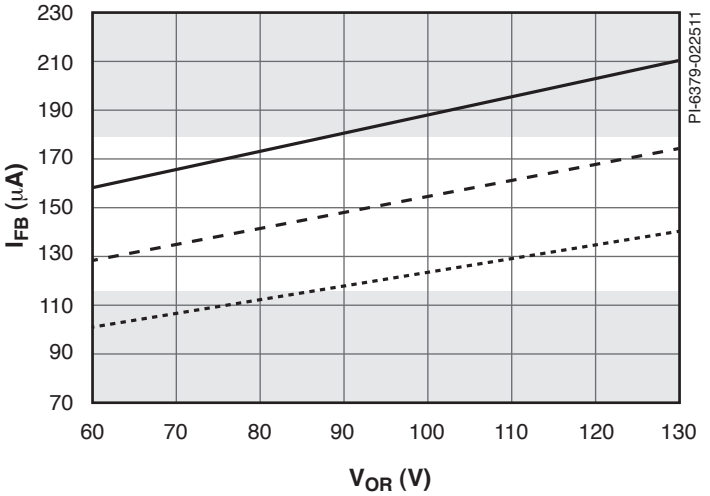
Reflected Output Voltage, V_{OR} (V)

This parameter is the secondary winding voltage during diode conduction, reflected back to the primary through the turns ratio of the transformer. Effectively V_{OR} is the parameter that sets the turns ratio of the transformer. The default value is 80 V; however the target range for V_{OR} is between 65 V and 135 V, provided that no warnings in the spreadsheet are triggered. For design optimization purposes, the following trade-offs should be considered:

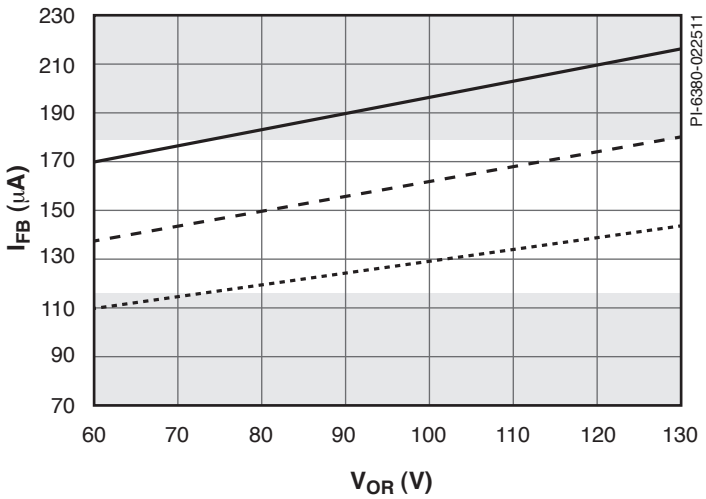
1. Higher values of V_{OR} (with low values of K_P) typically requires a larger core size due to the increased primary inductance and number of primary turns.
2. Higher values of V_{OR} reduces the output diode voltage stress. For $V_{O(MAX)}$ values below ~18 V this allows a Schottky output diode to be selected for lower losses and higher efficiency.
3. Higher values of V_{OR} reduces the maximum power capability of a given LinkSwitch-PH device.

Optimal selection of the V_{OR} value depends on the specific application and is based on a compromise between the factors mentioned above. Figure 9 may be used as a guide and provides an initial value based on the value of the V pin resistor and the output power. The upper line represents the maximum and lower line the minimum output power from the selected LinkSwitch-PH device as shown in the data sheet power table. The middle line is the mid point between these two power levels. The unshaded region is the recommended range for the feedback current I_{FB}.

An example of using these selection curves for a 14 W, universal input, LNK406EG design is shown in Figure 10. Start by labeling the upper and lower lines with the minimum and maximum power levels from the device data sheet power table. For the LNK406EG the maximum power table value in a universal or high line only design is 22 W. The minimum is 10 W. Therefore the middle line can be calculated as 16 W. Draw a parallel line between the existing lines on the chart representing the output power required, 14 W in this case. Then find the intersection between the 14 W power line and desired value of I_{FB}, with a value of 150 µA being ideal. In this example that intersection indicated a value for V_{OR} of 97 V.



(a)



(b)

Figure 9. V_{OR} Selection Curves for Designs Using a 2 MΩ (100/115 VAC) (a) and 4 MΩ (Universal or 230 VAC) (b) V Pin Resistor Values.

ENTER TRANSFORMER CORE/CONSTRUCTION VARIABLES					
Core Type	**Auto**		**EF25**		
Bobbin		*EF25_BOBBIN*		*P/N:*	*
AE			0.518	cm^2	Core Effective Cross Sectional Area
LE			5.78	cm	Core Effective Path Length
AL			2000	nH/T^2	Ungapped Core Effective Inductance
BW			15.6	mm	Bobbin Physical Winding Width
M			0	mm	Safety Margin Width (Half the Primary to Secondary Creepage Distance)
L	2		2		Number of Primary Layers
NS			28		Number of Secondary Turns

Figure 11. Transformer Variables Section of the Design Spreadsheet.

Primary Inductance, L_P (μH)
This is the calculated nominal value of primary inductance for the transformer. Designs using LinkSwitch-PH are insensitive to variations in the value of L_P in terms of output current and power delivery with the limitation being that the design maintains operation in continuous conduction mode. A tolerance of ±10% is typical when specifying the design to a transformer vendor.

Expected Average Output Current, Expected $I_{O(AVERAGE)}$ (A)
The calculated average output current, for a valid design this should match specified output current I_O.

Ripple to Peak Current Ratio at VAC_{MAX}, ($KP_{VAC(MAX)}$)
This is the calculated value of K_P at the peak of the maximum input voltage ($V_{AC(MAX)}$). This value should remain below 1.12 to ensure a PF of <0.9 at nominal AC input.

Minimum On Time at $VAC_{(MAX)}$, $t_{ON(MIN)}$ (μs)
This is the calculated minimum on time of the internal MOSFET at the peak of $V_{AC(MAX)}$. This value is should be greater than the minimum device on time of 1.5 μs.

Clamp Dissipation, P_{CLAMP} (W)
This is the calculated dissipation in the primary clamp. The calculation includes the effect of the variation in instantaneous dissipation over each AC half-cycle.

Step 4 – Select Transformer Core and Bobbin Based on Output Power and Enter A_E, L_E, A_L, BW, M, L, N_S

Core effective cross-sectional area, A_E (cm^2)
Core effective path length, L_E (cm)
Core ungapped effective inductance, A_L ($nH/turn^2$),
Bobbin width, BW: (mm)
Tape margin width equal to half the total margin, M (mm)
Primary Layers, L
Secondary Turns, N_S

Core Type
If the core type cell is left as the default of Auto, the spreadsheet will default to the smallest commonly available core suitable for the output power specified. The entire list of cores available can be selected from the drop down list in the tool bar of the PIXIs design software.

The grey override cells can be used to enter the core and bobbin parameters directly. This is useful if a core is selected that is not on the list, or the specified core or bobbin information differs from that referenced by the spreadsheet.

Note some core and bobbin types may not meet safety spacing requirements (e.g. RM or smaller EE sizes). In these cases it is common to use a triple insulated secondary winding terminated as flying leads (rather than to the bobbin pins). This allows safety creepage and clearance distances to be met and saves PCB board area by eliminating the need for a bobbin with increased spacings.

Safety Margin, M (mm)
For designs that require safety isolation between primary and secondary but do not use triple-insulated wire, the width of the safety margin to be used on each side of the bobbin should be entered here. For universal input designs, a total margin of 6.4 mm would be required, and a value of 3.2 mm would be entered into the spreadsheet. For low line only input designs (100/115/127 VAC) a total margin of 4 mm would be required and 2 mm entered into the spreadsheet. For vertical bobbins the margin may not be symmetrical. However, if a total margin of 6.2 mm were required, then 3.1 mm would still be entered even if the physical margin were only on one side of the bobbin.

For designs using triple insulated wire, it may still be necessary to enter a small margin in order to meet the required safety creepage distances.

Many bobbins exist for any core size and each will have different mechanical spacing. Refer to the bobbin data sheet or seek guidance from your safety expert or transformer vendor to determine what specific margin is required.

As the margin reduces the available area for the windings, the margin format described above may not be suitable for small core sizes. If after entering the margin, more than 3 primary layers (L) are required, it is suggested that either a larger core be selected or switch to a zero margin design approach using triple insulated wire.

Primary Layers, L
Primary layers should be in the range of 1 < L < 3, with a default value of 3. This provides a good compromise between winding losses and leakage inductance for a transformer core size appropriate for the output power. Three layers also results in lower capacitance hence improving efficiency, especially at higher input voltages. The lower limit on the value for L is set by the primary winding current density limits (circular mils per amp or CMA). CMA has a strong influence on the winding losses and therefore transformer temperature rise and efficiency. CMA values as low as 200 for designs <10 W scaling linearly to 600 at >50 W are good design targets for convection cooled designs.

For designs where the driver will be encapsulated for thermal management a lower value of CMA may be acceptable. Whether or not an encapsulant is used verification of the winding temperatures (using non ferrous T type thermocouples) is recommended. This is achieved by embedding a thermo-couple into the transformer between two of the insulation tape layers that are present between the primary and secondary windings during construction. Most designs will fall into insulation class A or class B limiting maximum winding temperatures (at maximum external ambient) to 105 °C and 130 °C respectively. Designs with more than 3 layers are possible, but the increased leakage inductance and issues associated with the physical fit of the windings should be considered. A split primary construction may be helpful for designs where leakage inductance clamp dissipation is too high and providing there is sufficient winding window. In a sandwich construction half of the primary winding is placed on either side of the secondary (and bias) windings. Sandwich construction is recommended for all design >20 W.

Secondary Turns, N_S

If the grey override cell is left blank, the minimum number of secondary turns is calculated such that the maximum operating flux density B_M is kept below the recommended maximum of 3100 Gauss (310 mT). In general, it is not necessary to enter a number in the override cell except in designs where a lower operating flux density is desired (see the explanation of B_M limits).

Step 5 – Iterate Transformer Design / Generate Prototype

Iterate the design making sure that no warnings are displayed. Any parameters outside the recommended range of values can be corrected by following the guidance given in the right hand column.

Once all warning and errors have been addressed click on the Transformer Parameter and Transformer Construction tabs to obtain detailed transformer specification and construction details. These can be used to either construct the transformer in house or send to an external magnetic vendor.

The key transformer electrical parameters are:

Primary Inductance, L_P (μH)

This is the target nominal primary inductance of the transformer.

Number of Primary Turns, N_P

TRANSFORMER PRIMARY DESIGN PARAMETERS					
LP			1246	uH	Primary Inductance
NP			79		Primary Winding Number of Turns
NB			25		Bias Winding Number of Turns
ALG			202	nH/T^2	Gapped Core Effective Inductance
BM			2845	Gauss	Maximum Flux Density at PO, VMIN (BM<3100)
BP			3442	Gauss	Peak Flux Density (BP<3700)
BAC			1138	Gauss	AC Flux Density for Core Loss Curves (0.5 X Peak to Peak)
ur			1776		Relative Permeability of Ungapped Core
LG			0.29	mm	Gap Length (Lg > 0.1 mm)
BWE			31.2	mm	Effective Bobbin Width
OD			0.4	mm	Maximum Primary Wire Diameter including insulation
INS			0.06	mm	Estimated Total Insulation Thickness (= 2 * film thickness)
DIA			0.34	mm	Bare conductor diameter
AWG			28	AWG	Primary Wire Gauge (Rounded to next smaller standard AWG value)
CM			161	Cmils	Bare conductor effective area in circular mils
CMA			524	Cmils/Amp	Primary Winding Current Capacity (200 < CMA < 600)
LP_TOL			10		Tolerance of primary inductance

Figure 12. Transformer Primary Design Parameters Section of the Design Spreadsheet.

TRANSFORMER SECONDARY DESIGN PARAMETERS (SINGLE OUTPUT EQUIVALENT)					
Lumped parameters					
ISP			2.61	A	Peak Secondary Current
ISRMS			0.98	A	Secondary RMS Current
IRIPPLE			0.85	A	Output Capacitor RMS Ripple Current
CMS			197	Cmils	Secondary Bare Conductor minimum circular mils
AWGS			27	AWG	Secondary Wire Gauge (Rounded up to next larger standard AWG value)
DIAS			0.36	mm	Secondary Minimum Bare Conductor Diameter
ODS			0.56	mm	Secondary Maximum Outside Diameter for Triple Insulated Wire

Figure 13. Transformer Secondary Design Parameters Section of the Design Spreadsheet.

VOLTAGE STRESS PARAMETERS					
VDRAIN			544	V	Estimated Maximum Drain Voltage assuming maximum LED string voltage (Includes Effect of Leakage Inductance)
PIVS			167	V	Output Rectifier Maximum Peak Inverse Voltage (calculated at VOVP, excludes leakage inductance spike)
PIVB			151	V	Bias Rectifier Maximum Peak Inverse Voltage (calculated at VOVP, excludes leakage inductance spike)

Figure 14. Voltage Stress Parameters Section of the Design Spreadsheet.

Gapped Core Effective Inductance, A_{LG} (nH/T²)
Used by the transformer vendor to specify the core center leg air gap. This is the value of inductance obtained (in nH) for the number of turns placed around the core squared.

Maximum Operating Flux Density, B_M (Gauss)
A maximum value of 3100 Gauss during normal operation is recommended. This prevents core saturation during start-up or output short-circuit

Peak Flux Density, B_P (Gauss)
A maximum value of 3700 Gauss is recommended to limit the maximum flux density under start-up and output short-circuit conditions. In these cases the output voltage is low and little reset of the transformer core occurs during the MOSFET off time. This can allow the transformer flux density to increase during the next and subsequent cycles (stair casing) until the core saturates. A value of 3700 Gauss, calculated at the maximum device current limit, together with the built-in protection features of LinkSwitch-PH devices, provides sufficient margin to prevent core saturation under start-up or output short-circuit conditions.

This calculation assumes worst-case current limit and nominal inductance values and accounts for high ambient temperatures as this reduces the saturation flux density of ferrite materials. It is important to verify that core saturation does not occur at maximum ambient temperature under start-up and overload conditions just prior to loss of regulation.

Maximum Primary Wire Diameter, OD (mm)
This is the calculated maximum wire size diameter that will allow the number of primary turns (N_P) to fit into the specified bobbin width (BW) with the specified number of layers (L).

The other factors automatically calculated by the spreadsheet include:

Estimated Total Insulation Thickness, INS (mm)
Primary wire size, DIA: (mm)
Primary wire gauge, AWG
Number of primary layers, L
Estimated core center leg gap length: L_G: (mm)
Number of secondary turns, N_S
Secondary wire size, DIAs: (mm)
Secondary wire gauge, AWG

Step 6 – Selection of LinkSwitch-PH External Components

The schematic shown in Figure 1 shows the external components for a typical LinkSwitch-PH power supply design. Each of these is dealt with in the relevant section below.

BYPASS Pin Capacitor (C4)
The BYPASS pin is both the supply rail for the IC and sets the operating mode between reduced and full power. For reduced power mode a 10 µF capacitor should be selected and for full power a 100 µF capacitor based on the selection entered into the design spreadsheet. Either ceramic or electrolytic types may be used with a voltage rating of 10 V or above and tolerance plus temperature variation of less than ±50%. Larger variation may cause the 100 µF capacitor to be incorrectly detected as a 10 µF value.

REFERENCE (R) Pin Resistor (R4)
This pin determines the operating mode between dimming and non dimming operation. For dimming operation a 49.9 kΩ 1% part and for non-dimming operation a 24.9 kΩ 1% part should be used. Resistors with 1% tolerance (or better) should be as variations in the resistor value directly impacts the supply output current and V pin thresholds for line UV and OV.

VOLTAGE MONITOR (V) Pin Resistor(s) (R_{V1} and R_{V2})
The initial value of the total resistance connected from the V pin to the DC bus is provided in the design spreadsheet as parameter R_{V1}. Resistor R_{V2} is connected from the V pin to SOURCE, typically only present in non-dimming designs to provide constant output current vs. line voltage. Both resistors should have 1% tolerance (or better) to provide unit to unit matching of both the line undervoltage threshold (to ensure parallel connected units turn on together) and dimming characteristics. A value for R_{V2} of >5 MΩ indicates that it is not required as it will be minimal. In Figure 1 R_{V1} is made up of R2 and R3 while R_{V2} is not shown as it was not required for this design.

External Bias Current (R5, D5)
Resistor R5 provides the operating current for U1 during normal operation. The inclusion of external bias is recommended even though, with the exception of the LNK403, LinkSwitch-PH devices can operate without any external bias. Providing an external bias reduces the device dissipation and allows operation to smaller conduction angles when used with phase angle dimmers. The design goal is to provide a current into the BP equal to $I_{CD1(MAX)}$ under worst case conditions. Worst-case usually occurs at $V_{O(MIN)}$ and lowest output current (due to dimming).

As an initial starting value or dimming designs the value of R5 should be selected to provide approximately 5 mA into the BYPASS pin at the nominal output voltage (V_O) according to the expression,

$$R5 = \frac{V_B - V_{BP}}{3 \times I_{CD1(MAX)}}$$

where V_B is the bias voltage from the design spreadsheet and V_{BP} is the BYPASS pin voltage (5.9 V_{TYP}) and $I_{CD1(MAX)}$ is the IC supply current from the device data sheet. The factor of 3 provides adequate margin due to variations in the bias voltage due to LED string (output) voltage, especially the reduction in the value of V_B that occurs during dimming.

For non dimming designs the factor of 3 can be omitted. Dissipation in R5 is <50 mW and tolerance is not critical (5% is acceptable).

Diode D5 can be any small signal diode with a voltage rating above 10 V (e.g. 1N4148, BAV21 etc). It is included to isolate the BP pin from the bias winding capacitor (C5) to prevent increased start-up delay and misdetection of the value of the BP capacitor.

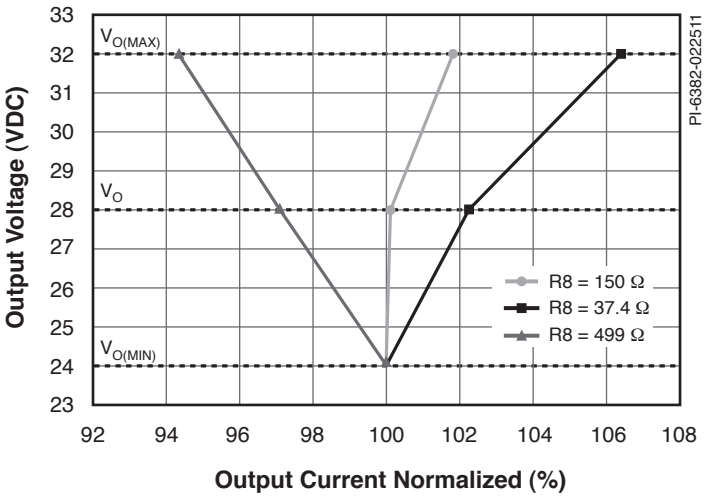


Figure 15. Effect of R8 (Bias Winding Filter Resistor) on Output Current Regulation vs. LED String Voltage (±15%).

Bias Diode (D5)

The primary referenced auxiliary winding on the transformer is rectified and filtered to create a bias supply that provides both the operating current into the BYPASS pin and feedback information into the FEEDBACK pin. The rectifier diode (D5) can be any fast or ultra fast recovery type with a voltage rating above the value given in the design spreadsheet (PIV_B), typically >200 V, and current rating >200 mA. The 1N4936 and UF4004 or SMD equivalents are good examples.

Filter Resistor (R8) and Capacitor (C5)

These two components form a low pass filter (pole). The corner frequency (1/2×π×R8×C5) should be where f_L is the minimum line frequency to prevent line frequency ripple modulating the FEEDBACK pin. A corner frequency of 50 Hz results in a power factor above 0.9 at 230 VAC input. If lower power factor is acceptable the corner frequency can be increased to allow the use of a lower value capacitor. The value of R8 should be in the range of 47 Ω to 200 Ω (5% tolerance). Making the value too high results in a reduction in the bias voltage which can reduce the minimum conduction angle at which the supply will operate. Making the value too small results in the value of C5 increasing which is undesirable due to board space constraints. Capacitor C5 should have a voltage rating above the value of $V_B \times (V_{O(MAX)} / V_O)$ and can be either an electrolytic or ceramic type.

Resistor R8 also optimizes output current regulation with changes in output voltage. Figure 15 shows the effect of changing R8 over a 10:1 range. It can be seen that a value of 150 Ω in this case gave the best output current regulation as the output voltage was varied ±15%.

Bleed Resistor (R7)

This resistor provides an addition load on the bias supply to prevent the voltage from peak charging due to the effects of transformer leaking inductance. Select the value (5% tolerance) to generate a current of ~2 mA at the bias voltage (V_B).

Feedback Resistor (R6)

For the first prototype use the value provided in the design spreadsheet (R_{FB1}). As this resistor directly impacts the output regulation it should have a 1% tolerance.

Peak Detector (D1, R1 and C3)

This network is used to provide a DC voltage from which a current is fed into the V pin of the LinkSwitch-PH device.

Diode D2 allows C3 to charge to the peak of the incoming rectified AC. Resistor R1 provides a discharge path to allow the voltage across C3 to track changes in the incoming AC. The value of C3 should be ≥100 nF for a PF of >0.9. Larger values (up to 1 μF) further increase the acheiveable PF up to 0.99. Values above 1 uF provide only incremental improvement but do provide additional filtering during differential line surges, reducing the peak drain voltage. A voltage rating of >1.41 × VAC_{MAX} is required and both film, ceramic or electrolytic types may be used. Resistor R1 should be selected such that R1 × C3 >80 ms so that the voltage across C3 is essential constant over one AC half cycle. A voltage rating of >1.41 × VAC_{MAX} is recommended. A standard 1N4007 plastic rectifier is recommended for D1.

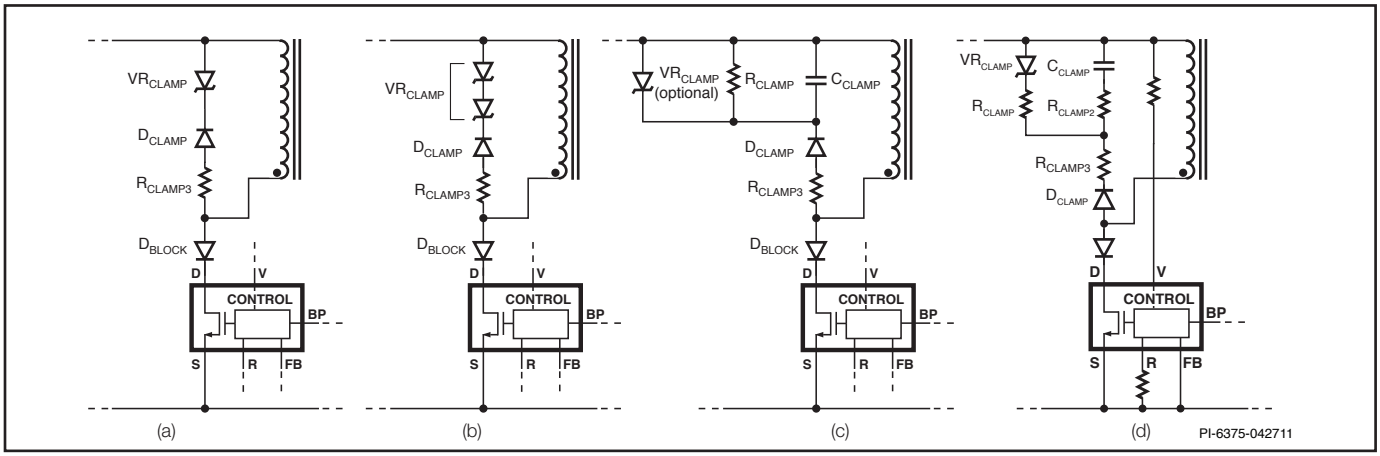


Figure 16. Recommended Clamp Configurations for LinkSwitch-PH Designs. (a) Zener Clamp, (b) Zener Clamp with Series Connected Zeners for Higher Power, (c) RCD / RCD+Z Clamp, (d) Zener Bleed Clamp.

P_O (W)	Reference Document	Configuration (Figure 10)	D_{BLOCK}	VR_{CLAMP} (V)	D_{CLAMP}	R_{CLAMP} (kΩ)	R_{CLAMP2} (Ω)	R_{CLAMP3} (Ω)	C_{CLAMP} (pF)
7	RDR-193	A	ES1D	P6KE200	UF4007	-	-	-	-
6.9	DER-269	C	US1D	-	RS1J	100	-	100	1000
8	DER-264	C	US1D	-	RS1J	50	-	100	1000
14	RDR-195	A	UF4006	P6KE200	UF4007	-	-	-	-
15	DER-256	C	MUR120	-	FR107	82	-	100	1000
15	DER-278	A	UF4004	P6KE200	UF4007	-	-	-	-

Table 4. Example Clamp Component Values for LinkSwitch-PH Designs.

Step 7 – Selection of Primary Clamp Components (D_2, D_3 and VR1)

Several different clamp configuration are shown in Figure 16. Diode D_{BLOCK} (D3 in Figure 1) prevents current flow occurring from source to drain during the period of each AC half-cycle where the rectified AC voltage is below the reflected output voltage (V_{OR}) of the design. The diode should be an ultra-fast type and have a current rating above the average drain current (I_{AVG}) and voltage rating of >1.2 × V_{OR} × ($V_{O(MAX)}$ / V_O). Good choices for this components include the UF4002 (1 A) and UF5402 (3 A).

When the internal MOSFET turns off, leakage inductance induces a voltage spike on the drain. To limit this voltage to below the 725 V BV_{DSS} rating of the internal MOSFET a clamp is required across the primary of the transformer. The clamp both limits the drain voltage and dissipates the leakage inductance energy. Clamp selection and design is similar to that of a standard flyback converter however the absence of bulk storage capacitance after the rectifier (to give high power factor) requires additional consideration.

The peak voltage on the drain is a function of the value of the input voltage, V_{OR} and the clamp voltage.

During each AC half-cycle, the primary peak current varies to provide an envelope that follows the AC voltage (giving high power factor). As the leakage energy is a function of the peak primary current this also varies during each AC half-cycle (E_{LEAK} = 0.5 × L_{LEAK} × I_P^2). Peak leakage energy occurs at the peak of the rectified input AC corresponding to the design spreadsheet value of I_P and it is at this point where the maximum peak drain voltage occurs.

The clamp must therefore be designed to provide sufficient drain voltage margin at the peak of the maximum AC input voltage (1.41 × VAC_{MAX}) and the maximum output voltage. In addition the clamp voltage must also remain significantly above the value of V_{OR} to minimize the amount of magnetizing energy (the energy that is stored in the transformer during the switch on time) being dissipated in the clamp.

The Zener or Zener Bleed configurations are preferred because the clamp voltage does not reduce below a fixed value (defined by the voltage of the Zener) irrespective of the value of E_{LEAK}. In comparison an RCD clamp has a clamping voltage that varies with the value of E_{LEAK}, reducing with the value of E_{LEAK}. As the clamp voltage reduces, towards the value of V_{OR}, proportionally more energy is dissipated in the clamp and less is delivered to the output thereby reducing efficiency.

The Zener configuration (Figure 16a) is the simplest to design, gives the highest efficiency across variations in output voltage and requires the fewest components but may have higher EMI generation due to higher dv/dt and di/dt.

The Zener Bleed configuration provides the lower EMI generation of an RCD clamp but has a defined minimum clamp voltage. The operation is similar to the RCD clamp. When the primary switch turns off, the leakage inductance energy charges C_{CLAMP} to above the voltage rating of VR_{CLAMP}. For the remainder of the switching period C_{CLAMP} is discharged via R_{CLAMP} and VR_{CLAMP} ready for the next turn-off event. The addition of VR_{CLAMP} in series with R_{CLAMP} ensures that the voltage across C_{CLAMP} cannot discharge to below the voltage rating of VR_{CLAMP}. Dissipation is shared between VR_{CLAMP} and R_{CLAMP} with the recommended voltage rating of VR_{CLAMP} being ~10% higher than the V_{OR} of the design.

The RCD configuration (Figure 16c with VR_{CLAMP} omitted) is attractive because of low EMI generation, low cost and scalability for higher power designs. The higher dissipation may be accommodated by sizing the power rating of R_{CLAMP} or using multiple resistors in parallel. However the RCD clamp requires more careful design as the clamping voltage varies with output voltage and peak drain current. This requires that the maximum clamp voltage is set at $V_{O(MAX)}$ and therefore results in lower efficiency at the nominal output voltage (V_O).

By adding a Zener to the RCD configuration (Figure 16c with VR_{CLAMP} present) to form the RCD+Z provides a good compromise between the fixed clamping voltage of a Zener and high power capability of the RCD. The Zener provides a fixed voltage clamp during transients (start-up or output short-circuit) but during normal operation the RC network clamps the peak drain voltage.

Zener diode peak current for configuration 16a and 16b is typically 0.6 to 0.8 × I_P and therefore transient suppressor diodes (TVS) are recommended. The P4KExxxA (1 W), P6KExxxA (5 W) and 1.5KExxxA (6.5 W) are good examples (where xxx represents the voltage rating and A indicates uni-directional.

For the RCD+Z and Zener Bleed configurations (Figures 16c and 16d) the peak Zener currents are significantly lower and standard 1-2 W Zener diode may be selected such as the BZY97Cxxx.

For high-power capability multiple Zener diodes may be placed in series (as shown in Figure 16b) with the overall voltage being equal to the desired clamping voltage. This is typically only required in output powers above 30 W based on Zener temperature rise.

For Figure 16 configurations (a), (b) and (c) a voltage rating of 200 V is recommended for VR_{CLAMP} but this can be lowered to provide additional drain voltage margin providing the value of VR_{CLAMP} is >1.4 × $V_{OR(MAX)}$, where $V_{OR(MAX)}$ is equal to V_{OR} × ($V_{O(MAX)}$/V_O).

Select the power rating of the clamp Zener(s) and/or resistor(s) based on the value for P_{CLAMP} given in the Key Design Parameters section of the design spreadsheet. This value represents the average energy dissipated in the clamp over one AC line cycle. Table 4 provides a good starting point for component selection based on output power.
Once a prototype is constructed verify the clamp component temperature to ensure that there is sufficient design margin when operated inside the final product enclosure (including LED) and highest ambient temperature.

D_{CLAMP} should be a fast or ultra fast type with a reverse recovery time <500 ns. Under no circumstances should a standard recovery rectifier diode be used. The high dissipation that may result during start-up or an output short-circuit can cause failure of the diode.

Step 8 – Output Overvoltage (Disconnected Load Protection – Optional) (D6, C7, R1, VR2, C5 and Q2 in Figure 1)

The purpose of this optional functional block is to limit the output voltage should the load (LED string) be disconnected. Without this protection the output voltage will rise to a high value that can cause failure of the output capacitors, the clamp components and the LinkSwitch-PH device. Even in LED retro-fit lamp applications, where disconnection of the LED load is a fault condition and represents product failure, output OVP may still be desirable to protect the supply during the manufacturing process and maintain the output voltage within SELV (safety extra low voltage) safety limits.

During unloaded operation the output voltage will rise, resulting in a proportional rise in the bias winding voltage. Once VR2 conducts and Q2 is biased on the FEEDBACK pin of U1 is pulled to source, initiating auto-restart mode. Once in auto-restart the 800 ms off time allows the output voltage to discharge via R11.

As soon as the load is reconnected normal operation resumes after the completion of the auto-restart off period.

The bias voltage is separately rectified and filtered by D6 and C7 to allow a faster response time than using the voltage across C5.

Diode D6 can be any small signal diode with a voltage rating greater that the value given in the design spreadsheet (PIV_B) and a current rating >150 mA. The value of C7 is not critical, use a 1 μF value and voltage rating above the bias voltage if no better data is available. Resistor R10 provides some load across C7 preventing peak charging. Start with a value of 10 kΩ, 5%.

Select the initial voltage rating of VR2 to be V_{OVP} + 5 V where the value of V_{OVP} is given in the Applications Variables section of the design spreadsheet. The 5 V figure compensates for the effects of peak charging and prevents false triggering under normal operation. Parts with power ratings ≤0.5 W and a tolerance of 5% are recommended.

Capacitor C6 provides noise filtering. Select any generic 100 nF, 50 V ceramic capacitor. Resistor R9 defines the current before Q3 is biased on, improving accuracy by operating the Zener closer to its data sheet test current. A value of 330 Ω to 1 kΩ, 5% is recommended, giving a Zener current of 0.5 mA to 2 mA. Transistor Q2 can be any small signal NPN transistor (collector voltage is <10 V and currents <1 mA). Once a prototype is constructed adjust the voltage of VR3 to be 5 – 10 V above the measured voltage across C7 at $V_{O(MAX)}$ (the maximum LED string voltage). This ensures that Q2 remains completely off during normal operation, preventing changing the output current.

Step 9 – Output Diode, Capacitors and Pre-load (D7, C9, C10 and R11)

Select an output diode with a current rating of ≥I_O and a voltage rating V_{RRM} >PIV_S where I_O and PIV_S are values from the design spreadsheet. A current rating of ≥ 2 × I_O results in higher efficiency and should be considered where necessary.

Ultrafast (t_{RR}<150 ns) or Schottky types should be selected. Schottky types will give higher efficiency, especially in lower output voltage designs where the diode forward voltage is a larger proportion of the secondary winding voltage.

Low or very low ESR capacitors should be used. Select the values based on allowable output (LED) current ripple with an initial value = ~1.5 μF per mA of output current for ±50% output current ripple. The capacitance value may be split across several capacitors for space reasons. When using low ESR types the ripple current rating of the capacitors is typically much higher than actual ripple current so typically this rating doesn't need to be considered.

Larger values of output capacitance reduces the output ripple and improves dimming range by maintaining feedback into the LinkSwitch-PH device even at very small TRIAC conduction angles.

Output LED ripple currents of ≤50% vs. DC have little performance impact, with negligible change in LED efficiency or color temperature.

Both electrolytic or ceramic capacitors may be used. Ceramic capacitors offer longer lifetime than electrolytic types however when used as output capacitors there is less benefit. This is due to the effect on LED operation at end life. Here the reduction in capacitance and increase in ESR results in higher LED ripple current but not outright failure of the driver. Lifetime of electrolytic capacitors is directly affected by operating temperature. However when using low ESR types with sufficient capacitance to limit output current ripple to ≤50% then capacitor self-heating is negligible and the operating temperature is equal to the ambient temperature.

Select the value of the output discharge and pre-load resistor to provide a current of 1.5 mA at the output voltage (R15 = V_O / 1.5 mA). This resistor causes the output to discharges below the LED string voltage when the AC is removed and therefore ensures the LED extinguish rather than there being a slight glow for several seconds after AC is removed.

Step 10 – TRIAC Leading Edge Dimmer Compatibility Components

Working with TRIAC Dimmers

The requirement to provide output dimming with low cost, TRIAC based, leading edge phase dimmers introduces a number of trade-offs in the design.

For correct operation incandescent phase angle dimmers typically have a specified minimum load, typically ~40 W for a 230 VAC rated unit. This is to ensure that the current through the internal TRIAC stays above its specified holding current threshold.

Due to the much lower power consumed by LED lighting the input current drawn by the lamp is below the holding current of the TRIAC within the dimmer. The input capacitance of the driver allows large inrush currents to flow when the TRIAC fires. This then generates input current ringing with the input stage and line inductance which may cause the current to fall below the TRIAC holding current. Both of these mechanisms cause undesirable behavior such as limited dimming range and/or flickering.

To overcome these issues two circuit blocks, damper and bleeder, are incorporated in dimming applications. The drawback of these circuits is increased dissipation and therefore reduced efficiency of the supply.

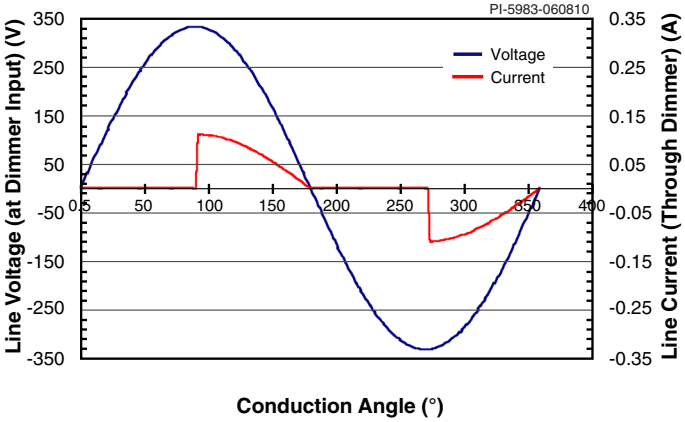


Figure 17. Ideal Input Voltage and Current Waveforms for a Leading Edge TRIAC Dimmer at 90° Conduction Angle.

Figure 17 shows the line voltage and current at the input of a leading edge TRIAC dimmer. In this example, the TRIAC conducts at 90 degrees.

Figure 18 shows the desired rectified bus voltage and current.

Figure 19 shows undesired rectified bus voltage and current with the TRIAC turning off prematurely and restarting. On the first half cycle this is due to the input current ringing below the holding current of the TRIAC, excited by the initial inrush current. The second half cycle also shows the TRIAC turning off due to the current falling below the holding current towards the end of the conduction angle. This difference in behavior on alternate half cycles is often seen due to a difference in the holding current of the TRIAC between the two operating quadrants.

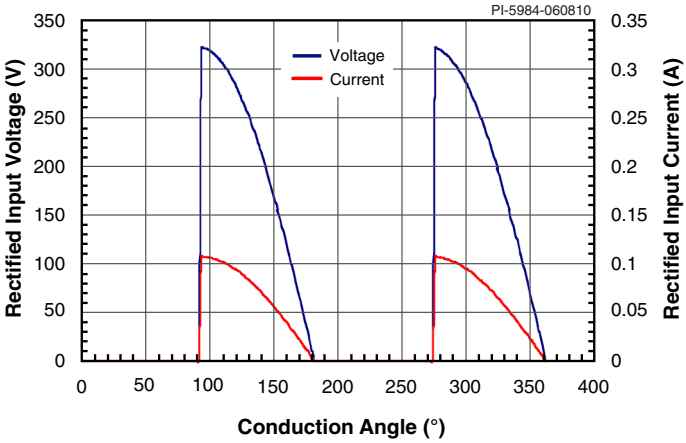


Figure 18. Resultant Waveforms Following Rectification of Ideal TRIAC Dimmer Output.

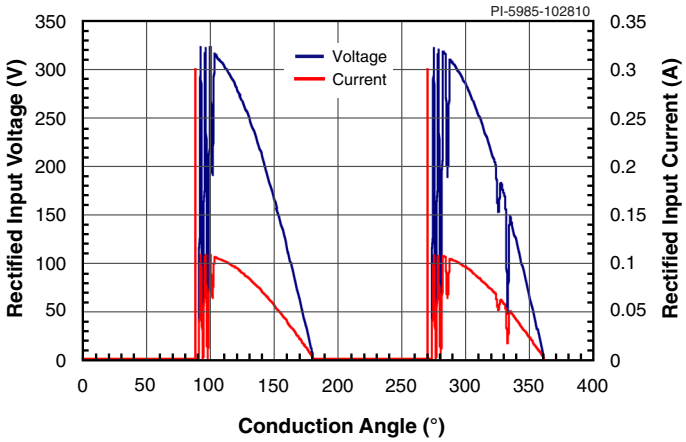


Figure 19. Example of Phase Angle Dimmer Showing Erratic Firing.

If the TRIAC is turning off before the end of the half cycle or rapidly turning on and off then a bleeder and damper circuit are required.

In general as power dissipated in the bleeder and damper circuits increases, so does dimmer compatibility.

Initially install a bleeder network across the rectified power bus (R7 and C12 in Figure 1) with initial values of 0.22 µF and a total resistance of 510 Ω and power rating of 2 W.

Reduce the capacitance value to find the minimum acceptable value. Reducing the capacitance value reduces power dissipation and therefore increases efficiency.

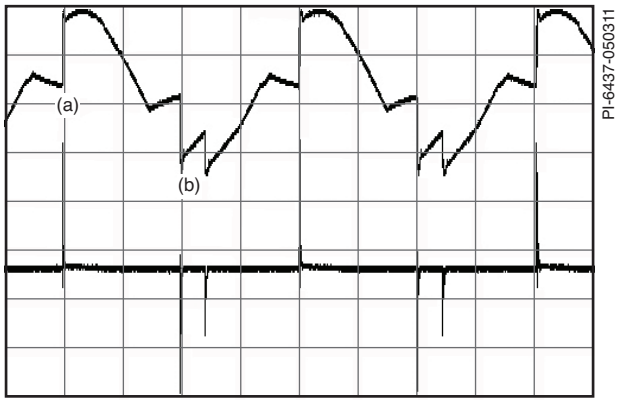


Figure 20. Example of TRIAC Dimmer Output Voltage and Current Showing Half-Cycle Dissymmetry Upper: AC Voltage (200 V / div.), Lower: AC Current (1 A / div.)

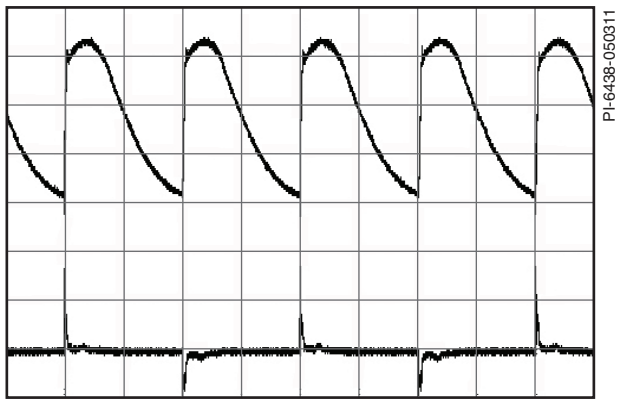


Figure 21. Example Waveforms Showing Correct TRIAC Operation at Minimum Conduction Angle. Upper: Rectified AC Input Voltage (100 V / div.), Lower: AC Input Current (1 A / div.)

If the bleeder circuit does not maintain conduction in the TRIAC on both AC half-cycles, then add a damper. Figure 20 shows a typical waveform where the bleeder circuit alone is not sufficient to maintain correct TRIAC conduction on both AC half-cycles. On positive half-cycles (a) the TRIAC conducts for the full conduction angle but on the negative half-cycle (b) the TRIAC fires twice. In this case a damper is required. The purpose of the damper is to limit the inrush current that flows through the input stage and line inductances as the input capacitance charges. Without limiting this current the input capacitor (C2 in Figure 1) voltage can reach significantly above the peak of the incoming AC voltage which causes the TRIAC current to fall to zero and therefore turn off. This cycle then repeats causing flicker.

For designs with an output power of less than 6 W, a passive damper may be used. Here a simple resistor in series with the AC input. Values in the range of 10 Ω – 100 Ω are typical with the upper range being limited by the allowed dissipation / temperature rise and reduction in efficiency. Values below 10 Ω may also be used but are less effective especially in high AC line input designs.

For higher power designs or if the passive damper is insufficient to prevent incorrect TRIAC operation then an active damper is required. This is typical in high-line applications due to the much larger inrush current that flows when the TRIAC turns on. A low cost active damper circuit is formed by R14, R15, C11, and Q1 in Figure 1. Resistor R16 limits the inrush current and can be a much higher value than the passive case as they are in circuit for only a fraction of the line cycle. Silicon controlled rectifier (SCR) Q1 shorts R16 after a delay defined by R14, R15 and C3. The delay is adjusted to give the shortest time that provides acceptable dimmer performance to minimize the dissipation in R16. Figure 21 shows the effect of adding the damper compared to the waveform in Figure 20. Here the TRIAC correctly conducts once each half-cycle. The SCR required is a low current, low cost device available with very low gate current requirements. The gate drive requirement of the selected SCR together with the minimum specified line voltage defines the maximum value of R14 and R15. SCRs with low gate trigger currents are recommended (Table 5). Maximum dissipation in the resistors of the damper and bleeder occurs at 90 degree TRIAC conduction and therefore thermal testing should be performed under this condition to verify component temperatures. For high-line designs it may be necessary to use a wirewound construction for the active damper resistor to prevent failure. This is due to the high instantaneous power dissipated when AC is first applied. In this case a single resistor is acceptable, for example the CRF series from Vitrohm.

It's common for different dimmers to behave differently across manufacturers and power ratings. For example a 300 W dimmer requires less dampening and requires less power loss in the bleeder than a 600 W or 1000 W dimmer due to the use

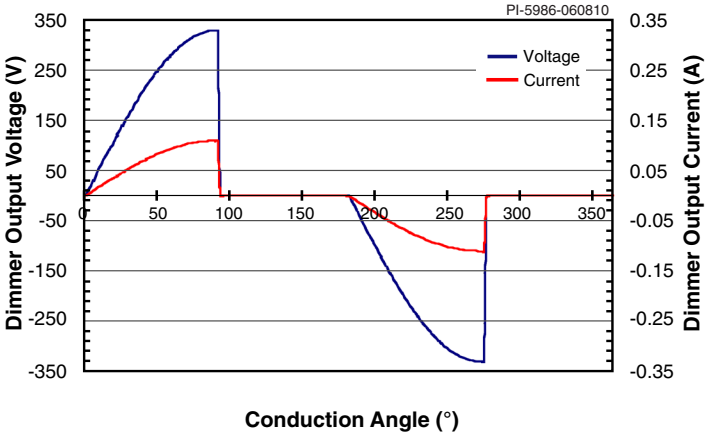


Figure 22. Ideal Dimmer Output Voltage and Current Waveforms for a Trailing Edge Dimmer at 90° Conduction Angle.

Part Number	Supplier	Specification
MCRZZ-6	On Semi	1.5 A, 400 V, TO-92, 200 µA
P0118DA	ST	0.8 A, 400 V, TO-92, 5 µA

Table 5. Example of SCRs Suitable for use in an Active Damper.

of a lower current rating TRIAC which typically have lower holding currents. Line impedance differences can also cause variation in behavior so during development the use of an AC source is recommended for consistency however testing using AC building power should also be performed.

Electronic Trailing Edge Dimmers

Figure 22 shows the line voltage and current at the input of the power supply with a trailing edge electronic dimmer. In this example, the dimmer conducts at 90 degrees. This type of dimmer typically uses a power MOSFET or IGBT to provide the switching function and therefore no holding current is necessary. Also since the conduction begins at the zero crossing, high current surges and line ringing are not an issue. Use of these types of dimmers typically does not require damper and bleeder circuits.

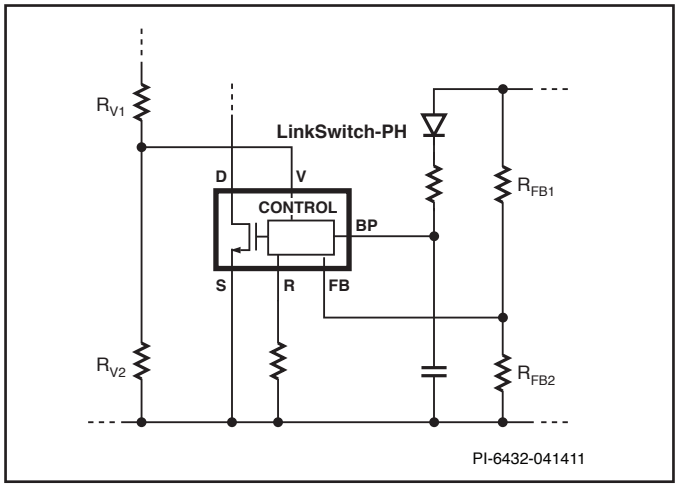


Figure 23. Partial Schematic Defining the Location of Resistors R_{V1}, R_{V2}, R_{FB1} and R_{FB2} Used During Output Fine Tuning.

Step 11 – Fine Tuning

Once a prototype has been built it may be necessary to adjust the values of the V and FEEDBACK pin resistors. This adjustment compensates for the actual bias voltage in operation (tracking between bias winding and secondary) the actual nominal output voltage (LED string voltage) and any voltage drops in the input stage. A two step procedure is required as both the V pin and feedback resistors change the output current. The V pin resistors optimize line voltage regulation whereas the FEEDBACK pin resistors primarily center the output current. Typically one or two iterations are required.

Start by adjusting the V pin resistor values before moving onto the FEEDBACK pin resistors. Figure 23 shows the location of both the V pin and FEEDBACK pin resistors.

Enter the actual values of R_{V1} and R_{V2} (if fitted) into the V pin Resistor Fine Tuning section of the design spreadsheet. If left blank then the original spreadsheet values are assumed. For non-dimming designs measure the output current at the nominal line voltages of the input specification e.g. 115 VAC and 230 VAC for a universal input specification. For designs that will operate with phase angle TRIAC dimmers measure at the minimum and maximum input voltage of the specified single line input voltage range e.g. for 230 VAC nominal measure at 195 VAC and 265 VAC.

Once entered the spreadsheet will provide new values ($R_{V1(NEW)}$, $R_{V2(NEW)}$). Values for $R_{V2(NEW)}$ above 10 MΩ can be ignored and $R_{V2(NEW)}$ omitted. As the new values will also modify the line undervoltage and line overvoltage values these are shown for reference. Change the resistor values on the prototype and re-measure the output current and move to FEEDBACK pin resistor adjustment.

Enter the actual values of R_{FB1} and R_{FB2} (if fitted) into the FEEDBACK pin resistor Fine Tuning section of the design spreadsheet. If left blank then the original spreadsheet values are assumed.

For non-dimming designs measure the bias voltage and output current at the nominal line voltages of the input specification. For example for a universal input voltage specification measure the bias voltage and output current at 115 VAC (V_{B1}, I_{O1}) and 230 VAC (V_{B2}, I_{O2}). For designs that will operate with phase

FINE TUNING (Enter measured values from prototype)					
V pin Resistor Fine Tuning					
RV1			4	M-ohms	Upper V Pin Resistor Value
RV2			1E+12	M-ohms	Lower V Pin Resistor Value
VAC1			115	V	Test Input Voltage Condition1
VAC2			230	V	Test Input Voltage Condition2
IO_VAC1			0.5	A	Measured Output Current at VAC1
IO_VAC2			0.5	A	Measured Output Current at VAC2
RV1 (new)			4	M-ohms	New RV1
RV2 (new)			20911.63	M-ohms	New RV2
V_OV			319.6	V	Typical AC input voltage at which OV shutdown will be triggered
V_UV			66.3	V	Typical AC input voltage beyond which power supply can startup
FB pin resistor Fine Tuning					
RFB1			141	k-ohms	Upper FB Pin Resistor Value
RFB2			1.00E+12	k-ohms	Lower FB Pin Resistor Value
VB1			22.5	V	Test Bias Voltage Condition1
VB2			27.5	V	Test Bias Voltage Condition2
IO1			0.5	A	Measured Output Current at Vb1
IO2			0.5	A	Measured Output Current at Vb2
RFB1 (new)			141.3	k-ohms	New RFB1
RFB2(new)			1.00E+12	k-ohms	New RFB2

Figure 24. Fine Tuning Section of the Design Spreadsheet.

angle TRIAC dimmers measure at the minimum and maximum input voltage of the specified single line input range. For example a design with a nominal input voltage of 115 VAC should be measured at 85 VAC (V_{B1}, I_{O1}) and 132 VAC (V_{B2}, I_{O2}). Once these values have been entered the spreadsheet with calculate new values for the FEEDBACK pin resistors ($R_{FB1(NEW)}$, $R_{FB2(NEW)}$). Values for R_{FB2} >4 MΩ can be ignored and R_{FB2} omitted.

Replace the existing resistors in the prototype with new values and measure the output current. If the output current is centered and line voltage regulation acceptable then no further adjustment is required. However if further improvement is desired complete a second iteration, entering the updated values for R_{FB1}, R_{FB2}, R_{V1} and R_{V2} into the relevant cells in the Fine Tuning section of the spreadsheet.

Tips and Tricks

Accurately Measuring Output Power

When measuring the efficiency of a LinkSwitch-PH design it is critical to accurately measure the output power. The normal practice of using a digital multimeter to measure the output current and voltage can cause significant errors if the line frequency output ripple is significant. For example a design with 100% output ripple compared to a design of the same output power but 10% ripple measured with DVMs will result in an efficiency measurement error of -3%. To avoid the error in design with output current ripple >~30% either use a power meter to directly measure the output power (for example the Yokogawa WT2xx series measures accurately to DC) or temporarily connect a large additional output capacitance during measurement (2200 μF). Once the output current and voltage are close to a DC level the measurement error when using DVMs becomes negligible.

PWM Dimming

Figure 25 shows a circuit configuration for implementing PWM dimming which converts the digital signal into an analog current which adjusts the FEEDBPACK (FB) pin current and therefore the output current. The dimming range achievable is 16:1.

The PWM signal is injected via Q1. This may be either a small signal NPN transistor or for isolation the transistor side of an optocoupler. With no PWM signal the value of IFB (the current into the FEEDBACK pin) is unchanged and the output is regulated as normal. As the PWM signal duty cycle increases the current into the FEEDBACK pin is lowered, lowering output current. At 100% duty cycle the FEEDBACK pin current is at a minimum giving the lowest output current.

With the value as shown R4 provides a bias from the BYPASS pin into the FEEDBACK pin which prevents the FEEDBACK pin current falling below the auto-restart threshold current of 20 μA when Q1 is fed with a 100% duty cycle signal. This will also disable auto-restart during a fault condition such as output short-circuits. This can be avoided if the maximum PMW duty cycle is limited or the value of R2 is adjusted to limit the maximum current through the optocoupler such that IFB is always >20 μA

The value for R_{FB} provided by the PIXIs design spreadsheet is split between R1 and R3 but must be increased to account for the 20 μA provided via R4. The expression for R1 is shown in the Figure. The value of R3 is not critical but should be a 1% type to give output current matching unit to unit.

The calculation for R2 is designed to limit the minimum voltage at the output of the resistor divider formed by R2 and R3 to be equal to 2.5 V when the PWM signal duty cycle is 100% duty cycle. For this example R2 would be 11 k.

The value of C1 is selected such that the time constant formed by C1 and R2 is >5 times the period of the PWM signal.

PWM frequencies above the eye's response (>100 Hz) are recommended to greatly reduce the likelihood of perceiving shimmer in the output.

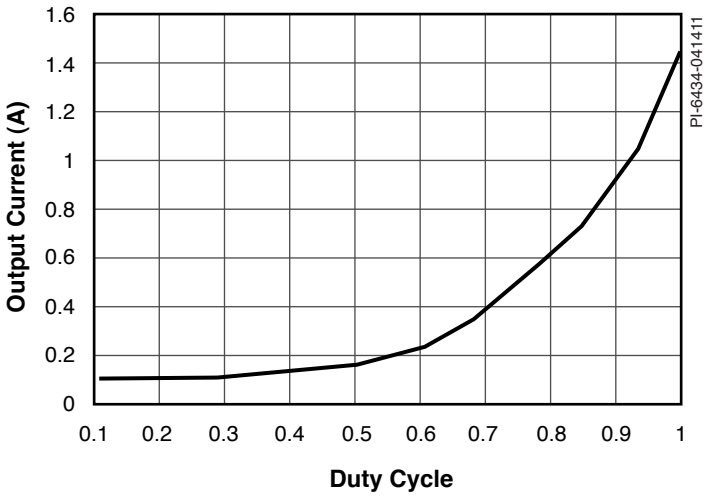
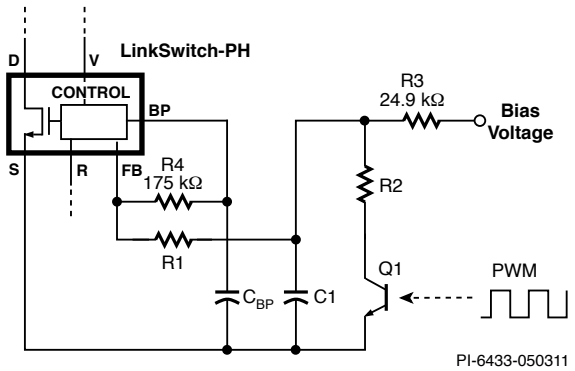


Figure 26. Duty Cycle to Output Current Characteristic for the PWM Dimming Circuit Shown in Figure 25.



$R_1 = ((V_{BIAS}-V_{FB}) / (I_{FB} - 20\ \mu A)) - R_3$

Where:
V_{BIAS} = Bias voltage
I_{FB} = FEEDBACK pin (from PIXIs)
V_{FB} = FEEDBACK pin voltage (2.4 V_{TYP})
20 μA is the current through R4

$C_1 \geq 5/(f_{PWM} \times R2)$

Where:
f_{PWM} = PWM frequency

$$R2 = \frac{2.5 \times R3}{V_{BIAS(FD)} - 2.5}$$

Where:
V_{BIAS} = Bias voltage at full dimming, assume $V_{BIAS}/3$

Figure 25. Circuit Configuration for PWM Dimming.

Revision	Notes	Date
A	Initial Release	05/11

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