

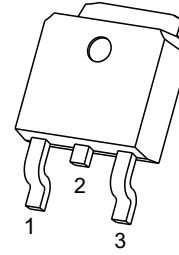
Description

- The Power MOSFET is fabricated using the advanced planer VDMOS technology. The resulting device has low conduction resistance, superior switching performance and high avalanche energy.

General Features

- RDS(ON) < 1.4 Ω @VGS = 10 V
- Ultra low gate charge
- Low reverse transfer Capacitance
- Fast switching capability
- Avalanche energy tested
- Improved dv/dt capability, high ruggedness

TO-252

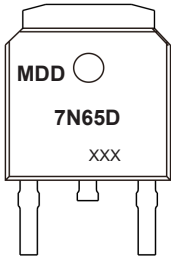


1. Gate
2. Drain
3. Source

Application

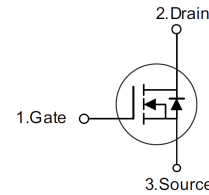
- High efficiency switch mode power supplies
- Electronic lamp ballasts based on half bridge
- LED power supplies

Marking



XXX: Date Code

Equivalent Circuit



Absolute Maximum Ratings (T_A=25°C unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V _{DS}	650	V
Gate-Source Voltage	V _{GS}	±30	V
Avalanche Current (Note 2)	I _{AR}	7	A
Continuous Drain Current	I _D	7	A
Pulsed Drain Current (Note 2)	I _{DM}	29.6	A
Avalanche Energy Single Pulsed (Note 3)	E _{AS}	530	mJ
Avalanche Energy Repetitive (Note 2)	E _{AR}	14.2	mJ
Peak Diode Recovery dv/dt (Note 4)	dv/dt	4.5	V/ns
Power Dissipation	P _D	120	W
Junction Temperature	T _J	150	°C
Storage Temperature	T _{stg}	-55 ~+150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature

3. L = 19.5mH, I_{AS} = 7.0A, V_{DD} = 50V, R_G = 25 Ω Starting T_J = 25°C

4. I_{SD} ≤ 7.0A, di/dt ≤ 200A/μs, V_{DD} ≤ BV_{DSS}, Starting T_J = 25°C



Ta = 25°C unless otherwise specified

Symbol	Parameter	Condition	Min	Typ	Max	Unit	
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	650	--	--	V	
I_{GSS}	Gate-Source Leakage Current	Forward	$V_{GS}=30V, V_{DS}=0V$	--	--	100	nA
		Reverse	$V_{GS}=-30V, V_{DS}=0V$	--	--	-100	nA
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=650V, V_{GS}=0V$	--	--	1	uA	
$V_{GS(TH)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	2.0	--	4.0	V	
$R_{DS(ON)}$	Drain-Source On-State Resistance	$V_{GS}=10V, I_D=3.5A$	--	1.2	1.4	Ω	
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D=250\mu A$	--	0.67	--	V/C	

Dynamic Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
C_{iss}	Input Capacitance	$V_{DS}=25V$ $V_{GS}=0V$ $f=1MHz$	--	--	1400	pF
C_{oss}	Output Capacitance		--	--	180	pF
C_{rss}	Reverse Transfer Capacitance		--	16	21	pF
Q_g	Total Gate Charge	$V_{DS}=520V,$ $V_{GS}=10V,$ $I_D=7.0A$ (Note1,2)	--	29	38	nC
Q_{gs}	Gate Source Charge		--	7	--	nC
Q_{gd}	Gate Drain Charge		--	14.5	--	nC

Switching Characteristics

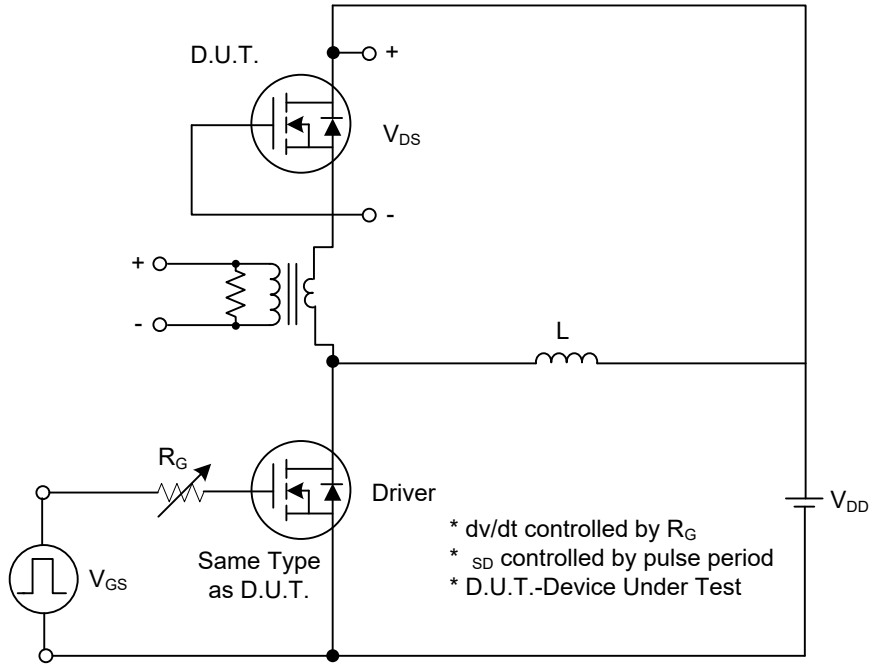
Symbol	Parameter	Condition	Min	Typ	Max	Unit
$t_{d(on)}$	Turn on Delay Time	$V_{DS}=325V,$ $I_D=7.4A,$ $R_G=25\Omega$ (Note1,2)	--	--	70	ns
t_r	Turn on Rise Time		--	--	170	ns
$t_{d(off)}$	Turn Off Delay Time		--	--	140	ns
t_f	Turn Off Fall Time		--	--	130	ns

Source Drain Diode Characteristics

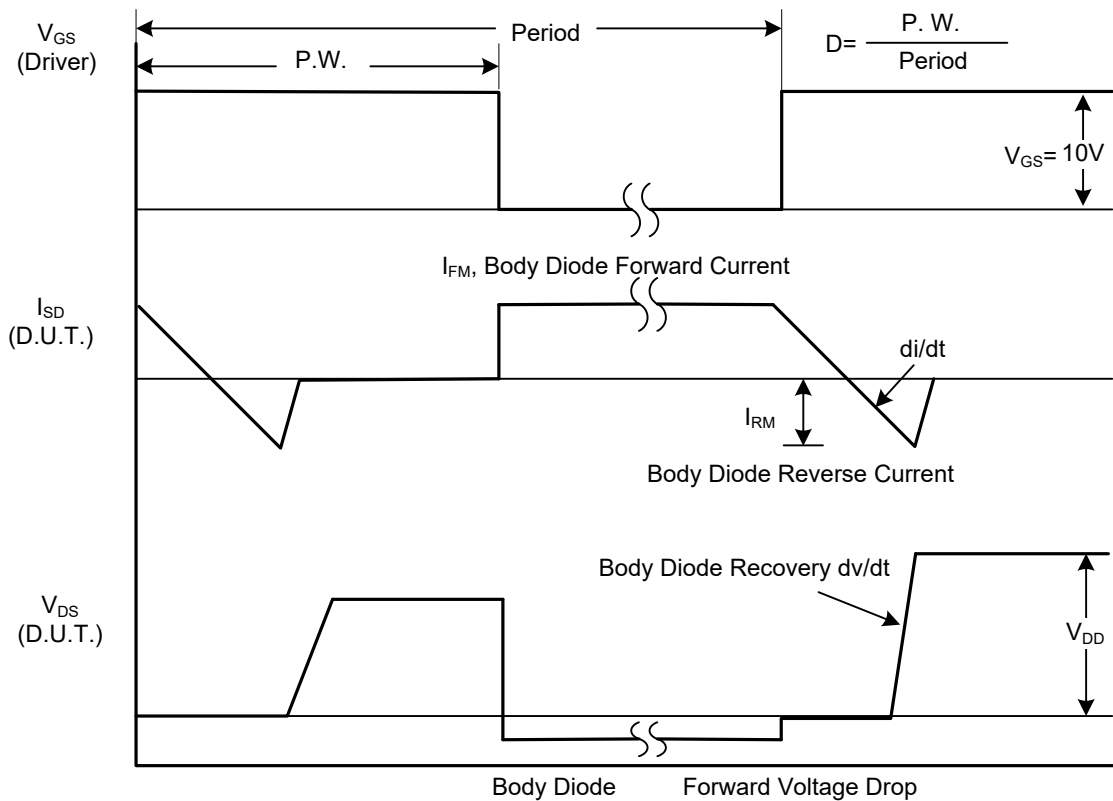
Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{SD}	Source drain current(Body Diode)		--	--	7	A
I_{SM}	Pulsed Current		--	--	29.6	A
V_{SD}	Drain-Source Diode Forward Voltage	$I_S=7A, V_{GS}=0V$	--	--	1.4	V
t_{rr}	Body Diode Reverse Recovery Time	$I_S=7A, V_{GS}=0V,$ $dI_S/dt=100A/\mu s$	--	320	--	ns
Q_{rr}	Body Diode Reverse Recovery Charge		--	2.4	--	uC

- Notes:**
1. Pulse test ; Pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$.
 2. Essentially independent of operating temperature.

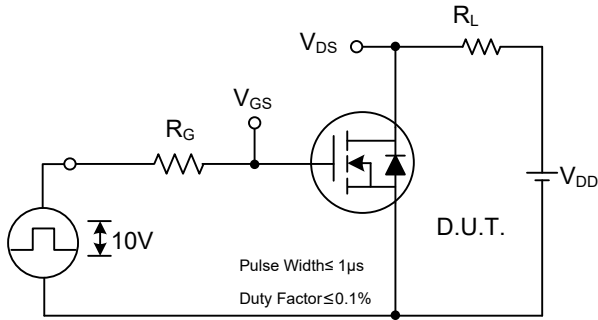
■ TEST CIRCUITS AND WAVEFORMS



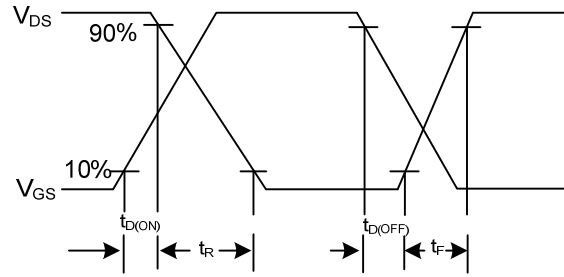
Peak Diode Recovery dv/dt Test Circuit



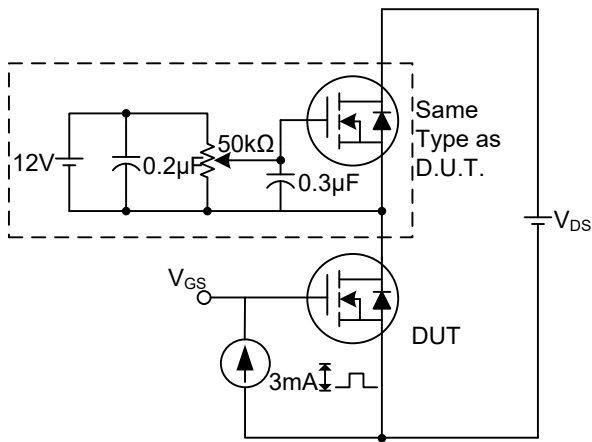
Peak Diode Recovery dv/dt Waveforms



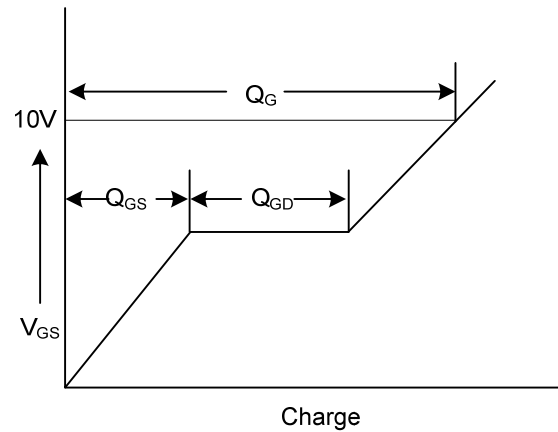
Switching Test Circuit



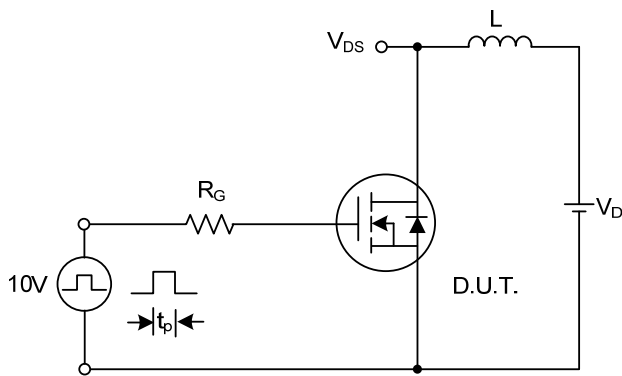
Switching Waveforms



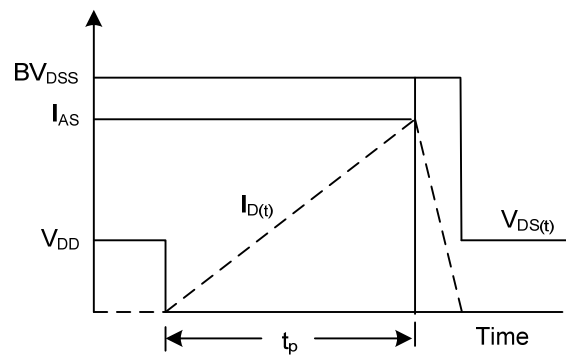
Gate Charge Test Circuit



Gate Charge Waveform



Unclamped Inductive Switching Test Circuit



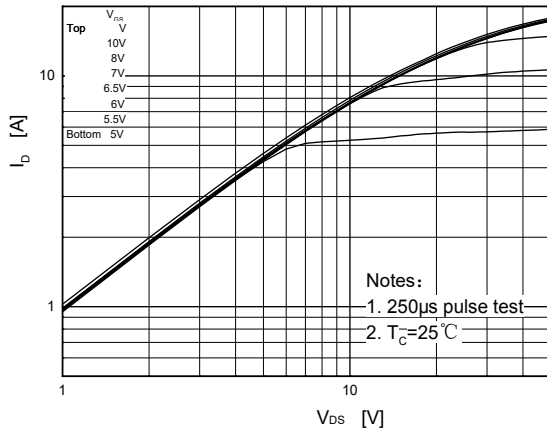
Unclamped Inductive Switching Waveforms

The curve above is for reference only.

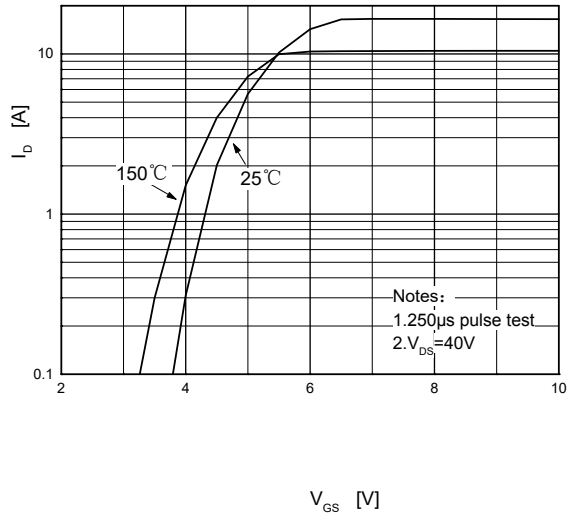


ELECTRICAL CHARACTERISTICS

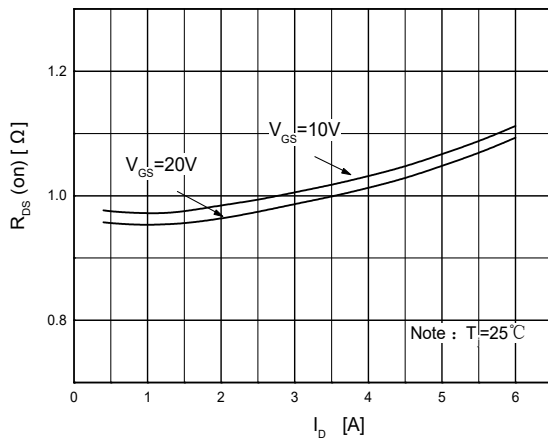
On-Region Characteristics



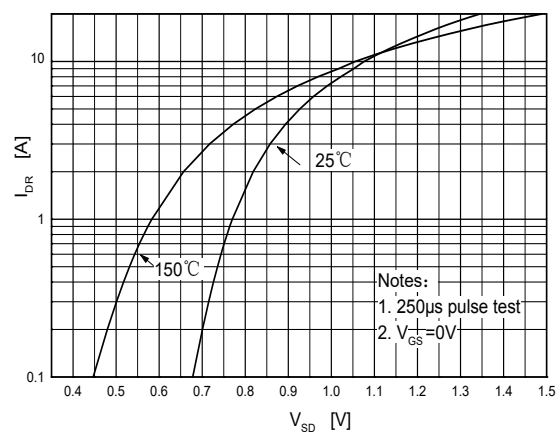
Transfer Characteristics



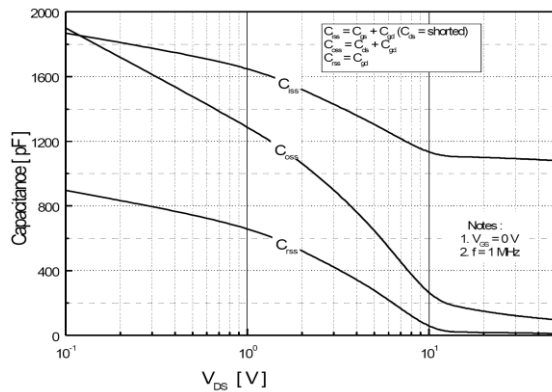
On-Resistance Variation vs. Drain Current and Gate Voltage



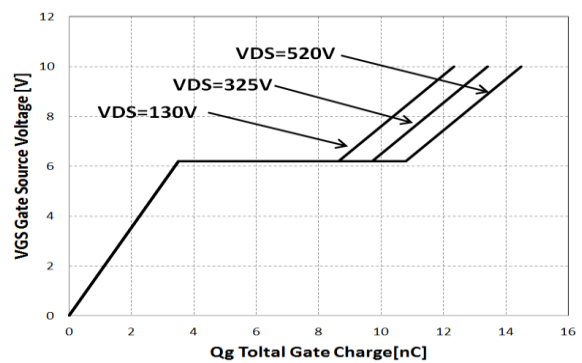
Body Diode Forward Voltage Variation vs. Source Current and Temperature



Capacitance Characteristics



Gate Charge Characteristics

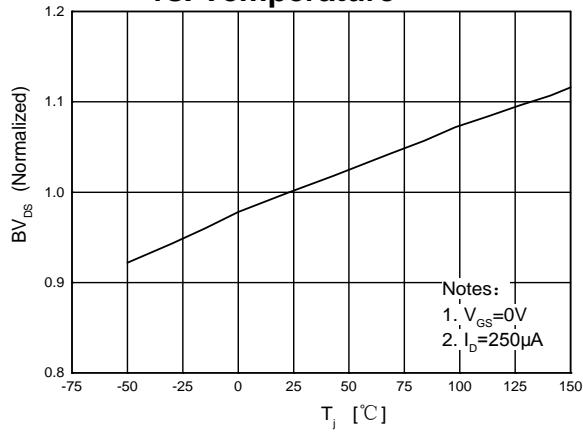




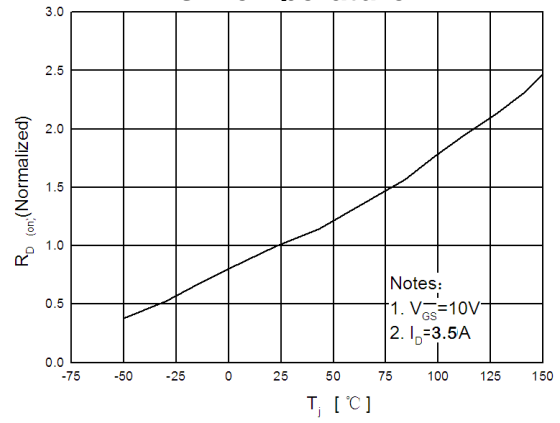
MDD7N65D

650V N-Channel Enhancement Mode MOSFET

Breakdown Voltage Variation vs. Temperature



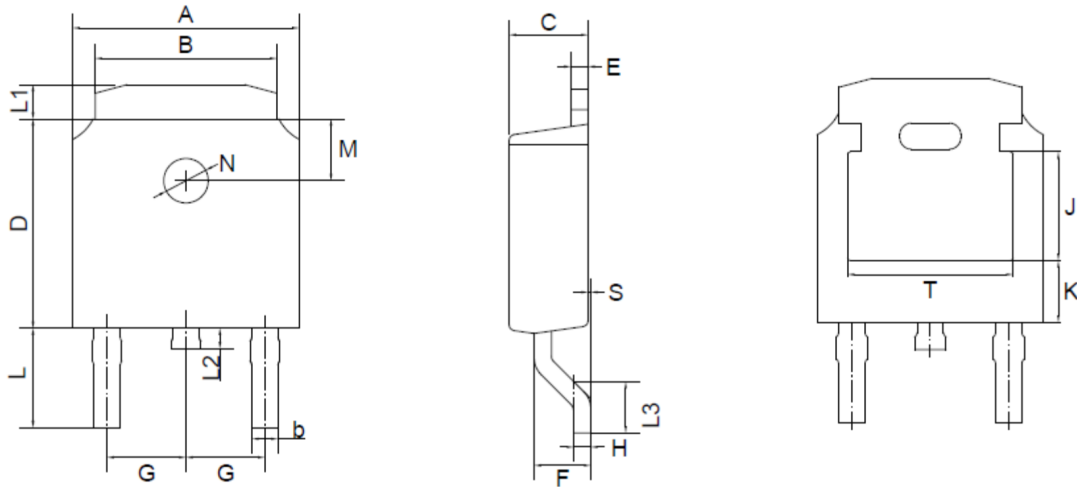
On-Resistance Variation vs. Temperature



The curve above is for reference only.

Outline Drawing

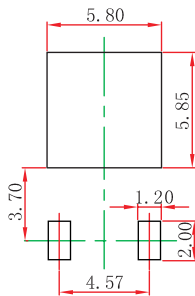
TO-252 Package Outline Dimensions



TO-252(D-PAK) mechanical data

UNIT		A	B	b	C	D	E	F	G	H	L	L1	L2	L3	S	M	N	J	K	T
mm	max	6.7	5.5	0.8	2.5	6.3	0.6	1.8	2.29 TYPICAL	0.55	3.1	1.2	1.0	1.75	0.1	1.8 TYPICAL	1.3 TYPICAL	3.16 ref.	1.80 ref.	4.83 ref.
	min	6.3	5.1	0.3	2.1	5.9	0.4	1.3		0.45	2.7	0.8	0.6	1.40	0.0					
mil	max	264	217	31	98	248	24	71	90 TYPICAL	22	122	47	39	69	4	71 TYPICAL	51 TYPICAL	124 ref.	71 ref.	190 ref.
	min	248	201	12	83	232	16	51		18	106	31	24	55	0					

Suggested Pad Layout



Note:

1. Controlling dimension: in/millimeters.
2. General tolerance: $\pm 0.05\text{mm}$.
3. The pad layout is for reference purposes only.

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