

SERIES: PYB30-U | DESCRIPTION: DC-DC CONVERTER
FEATURES

- up to 30 W isolated output
- industry standard pinout
- 4:1 input range (9~36 Vdc, 18~75 Vdc)
- smaller package
- single/dual/triple regulated outputs
- 1,500 Vdc isolation
- continuous short circuit, over current protection, over voltage protection
- temperature range (-40~85°C)
- six-sided metal shielding
- efficiency up to 90%



MODEL	input voltage		output voltage (Vdc)	output current		output power max (W)	ripple and noise ¹ max (mVp-p)	efficiency typ (%)
	typ (Vdc)	range (Vdc)		min (mA)	max (mA)			
PYB30-Q24-S5-U	24	9~36	5	300	6000	30	100	88
PYB30-Q24-S12-U	24	9~36	12	125	2500	30	100	88
PYB30-Q24-S15-U	24	9~36	15	100	2000	30	100	90
PYB30-Q24-D5-U	24	9~36	±5	±150	±3000	30	100	86
PYB30-Q24-D12-U	24	9~36	±12	±63	±1250	30	100	89
PYB30-Q24-D15-U	24	9~36	±15	±50	±1000	30	100	90
PYB30-Q24-T312-U	24	9~36	3.3 ±12	175 ±31	3500 ±625	26.5	100	85
PYB30-Q24-T315-U	24	9~36	3.3 ±15	175 ±25	3500 ±500	26.5	100	86
PYB30-Q24-T512-U	24	9~36	5 ±12	150 ±31	3000 ±625	30	100	88
PYB30-Q24-T515-U	24	9~36	5 ±15	150 ±25	3000 ±500	30	100	88
PYB30-Q48-S5-U	48	18~75	5	300	6000	30	100	88
PYB30-Q48-S12-U	48	18~75	12	125	2500	30	100	88
PYB30-Q48-S15-U	48	18~75	15	100	2000	30	100	89
PYB30-Q48-D5-U	48	18~75	±5	±150	±3000	30	100	86
PYB30-Q48-D12-U	48	18~75	±12	±63	±1250	30	100	87
PYB30-Q48-D15-U	48	18~75	±15	±50	±1000	30	100	87
PYB30-Q48-T312-U	48	18~75	3.3 ±12	175 ±31	3500 ±625	26.5	100	85
PYB30-Q48-T315-U	48	18~75	3.3 ±15	175 ±25	3500 ±500	26.5	100	85
PYB30-Q48-T512-U	48	18~75	5 ±12	150 ±31	3000 ±625	30	100	88
PYB30-Q48-T515-U	48	18~75	5 ±15	150 ±25	3000 ±500	30	100	87

Notes: 1. Ripple and noise are measured at 20 MHz BW by "parallel cable" method with 1 µF ceramic and 10 µF electrolytic capacitors on the output.

PROTECTIONS

parameter	conditions/description	min	typ	max	units
short circuit protection	hiccup, continuous, automatic recovery				
over current protection			150		%
over voltage protection	3.3 Vdc output models		3.9		Vdc
	5 Vdc output models		6.2		Vdc
	12 Vdc output models		15		Vdc
	15 Vdc output models		18		Vdc

SAFETY AND COMPLIANCE

parameter	conditions/description	min	typ	max	units
isolation voltage	for 1 minute at 1 mA max.	1,500			Vdc
isolation resistance	at 500 Vdc	1,000			MΩ
conducted emissions	CISPR22/EN55022, class A, class B (external circuit required, see Figure 1-b)				
radiated emissions	CISPR22/EN55022, class A, class B (external circuit required, see Figure 1-b)				
ESD	IEC/EN61000-4-2, class B, contact ± 4kV				
radiated immunity	IEC/EN61000-4-3, class A, 10V/m				
EFT/burst	IEC/EN61000-4-4, class B, ± 2kV (external circuit required, see Figure 1-a)				
surge	IEC/EN61000-4-5, class B, ± 2kV (external circuit required, see Figure 1-a)				
conducted immunity	IEC/EN61000-4-6, class A, 3 Vr.m.s				
voltage dips & interruptions	IEC/EN61000-4-29, class B, 0%-70%				
MTBF	as per MIL-HDBK-217F @ 25°C	1,000,000			hours
RoHS	2011/65/EU				

ENVIRONMENTAL

parameter	conditions/description	min	typ	max	units
operating temperature	see derating curve	-40		85	°C
storage temperature		-55		125	°C
storage humidity	non-condensing	5		95	%
case temperature	at full load, Ta=71°C			105	°C

MECHANICAL

parameter	conditions/description	min	typ	max	units
dimensions	67.5 x 54.99 x 19.05				mm
case material	aluminum alloy				
weight			58		g

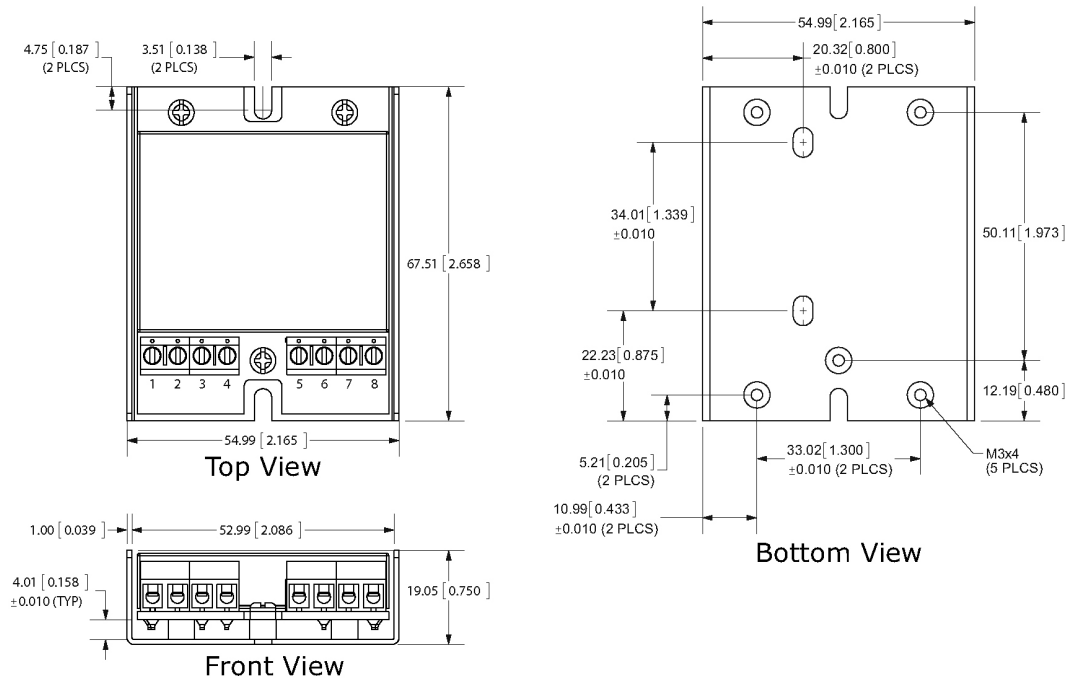
MECHANICAL DRAWING

U-FRAME

units: mm[inch]
tolerance: $\pm 0.5[\pm 0.020]$

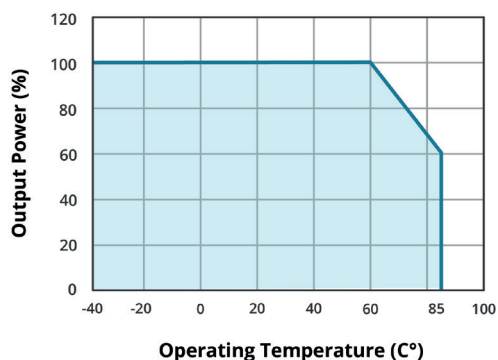
Wire range: 22~14 AWG
DIN rail mounting kit available
(part# STK-DIN)

PIN CONNECTIONS			
PIN	Single Output	Dual Output	Triple Output
1	Vin	Vin	Vin
2	GND	GND	GND
3	CTRL	CTRL	CTRL
4	Case	Case	Case
5	NC	Trim	-Vo2
6	Trim	-Vo	0V
7	0V	0V	+Vo1
8	+Vo	+Vo	+Vo2



DERATING CURVES

TEMPERATURE DERATING CURVE



EMC RECOMMENDED CIRCUIT

Figure 1

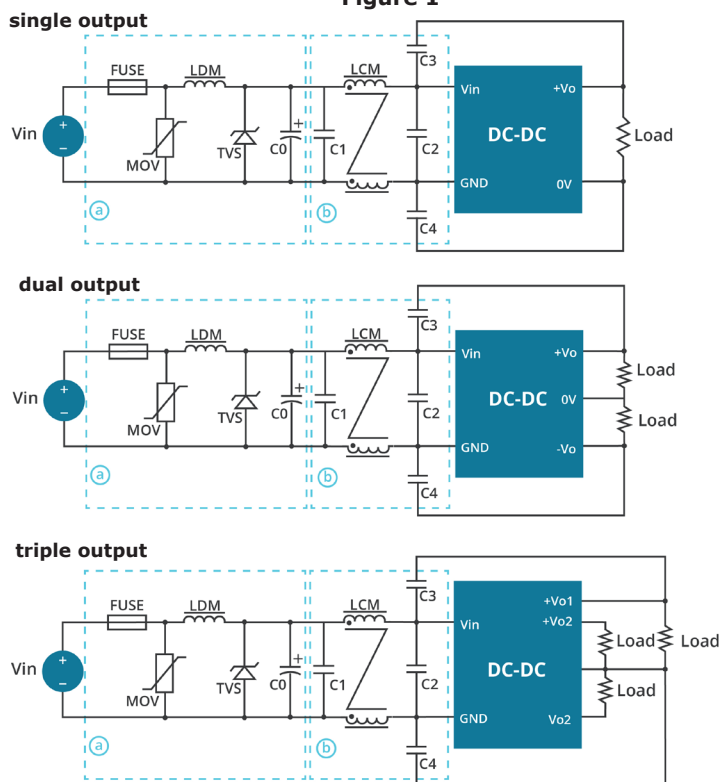


Table 1

Recommended external circuit components		
Vin (Vdc)	24	48
FUSE	Choose according to input current	
MOV	10D560K	10D101K
LDM	56μH	56μH
TVS	SMCJ48A	SMCJ90A
C0	120μF/50V	120μF/100V
C1	4.7μF/50V	2.2μF/100V
LCM	2.2mH	2.2mH
C2	4.7μF/50V	2.2μF/100V
C3*	1nF/2kV	1nF/2kV
C4*	1nF/2kV	1nF/2kV

Note: *2nF/2kV capacitors for triple output, 48 Vdc input models.

TEST CONFIGURATION

Figure 2

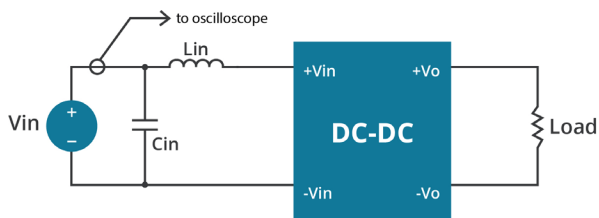


Table 2

External components	
Lin	4.7μH
Cin	220μF, ESR < 1.0Ω at 100 kHz

Note: Input reflected-ripple current is measured with an inductor Lin and Capacitor Cin to simulate source impedance.

APPLICATION NOTES

1. Recommended circuit

This series has been tested according to the following recommended testing circuit before leaving the factory. This series should be tested under load (see Figure 3). If you want to further decrease the input/output ripple, you can increase the capacitance accordingly or choose capacitors with low ESR (see Table 3). However, the capacitance of the output filter capacitor must be appropriate. If the capacitance is too high, a startup problem might arise. For every channel of the output, to ensure safe and reliable operation, the maximum capacitance must be less than the maximum capacitive load (see Table 4).

Figure 3

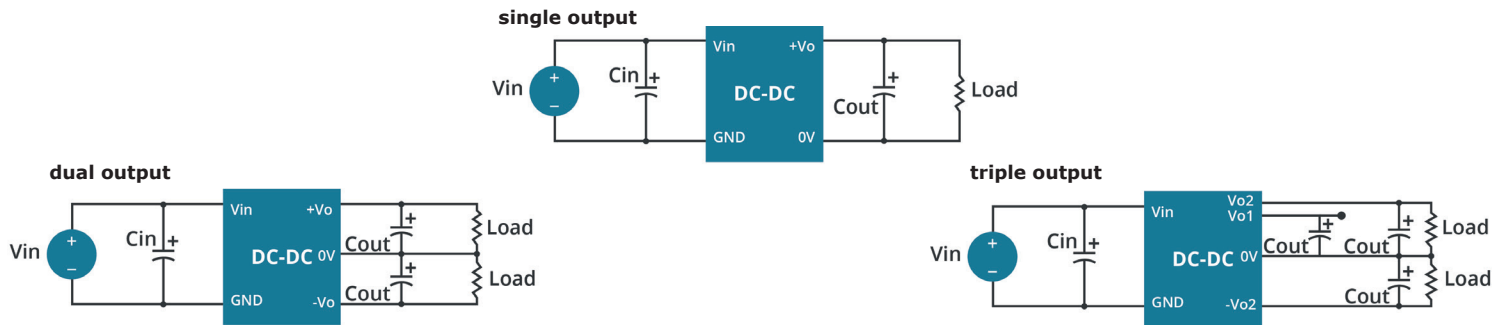


Table 3

Single Vout (Vdc)	Cin (μF)	Cout (μF)	Dual Vout (Vdc)	Cin (μF)	Cout ¹ (μF)	Triple Vout (Vdc)	Cin (μF)	Cout ¹ (μF)
--	--	--	--	--	--	3.3	10	10
5	10	10	±5	10	10	5	10	10
12	10	4.7	±12	10	4.7	±12	10	4.7
15	10	4.7	±15	10	4.7	±15	10	4.7

Note: 1. For each output.

Table 4

Single Vout (Vdc)	Max. Capacitive Load (μF)	Dual Vout (Vdc)	Max. Capacitive Load ¹ (μF)	Triple Vout (Vdc)	Max. Capacitive Load ¹ (μF)
--	--	--	--	3.3/±12	4700/300
5	6000	5	2000	3.3/±15	4700/220
12	2500	12	1250	5/±12	4700/300
15	1100	15	680	5/±15	4700/220

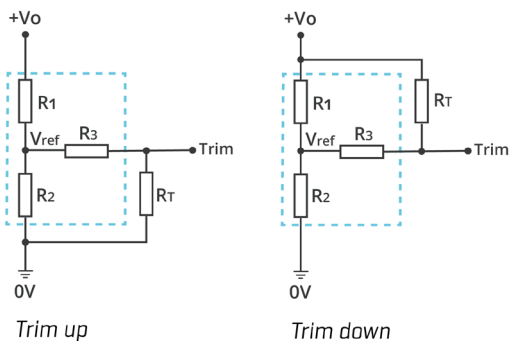
Note: 1. For each output.

2. Output voltage trimming

Leave open if not used.

Figure 4

Application Circuit for Trim pin
(part in broken line is the interior of models)



Formula for Trim Resistor

$$\begin{aligned} \text{up: } R_T &= \frac{aR_2}{R_2-a} - R_3 & a &= \frac{V_{ref}}{V_o' - V_{ref}} \cdot R_1 \\ \text{down: } R_T &= \frac{aR_1}{R_1-a} - R_3 & a &= \frac{V_o' - V_{ref}}{V_{ref}} \cdot R_2 \end{aligned}$$

Note: Value for R1, R2, R3, and Vref refer to Table 5
R_T: Trim Resistor
a: User-defined parameter, no actual meanings
V_{o'}: The trim up/down voltage

Table 5

Vout (Vdc)	R1 (kΩ)	R2 (kΩ)	R3 (kΩ)	Vref (V)
5	2.883	2.864	10	2.5
12	10.971	2.864	17.8	2.5
15	14.497	2.864	17.8	2.5

Note: 1. Minimum load shouldn't be less than 5%, otherwise ripple may increase dramatically. Operation under minimum load will not damage the converter, however, they may not meet all specifications listed.
2. Maximum capacitive load is tested at input voltage range and full load.
3. All specifications are measured at Ta=25°C, humidity<75%, nominal input voltage and rated output load unless otherwise specified.

REVISION HISTORY

rev.	description	date
1.0	initial release	06/26/2013
1.01	updated spec	08/16/2013
1.02	updated spec	08/18/2014
1.03	discontinued heat sink versions	06/21/2019
1.04	company logo updated	02/16/2021
1.05	removed heat sink versions, derating curve updated	03/15/2021
1.06	circuit figures updated	08/30/2021

The revision history provided is for informational purposes only and is believed to be accurate.



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