

### Description

The DL0504S2-T6B0 is an ultra low capacitance TVS array, utilizing leading monolithic silicon technology to provide fast response time and low ESD clamping voltage, making this device an ideal solution for protecting voltage sensitive high-speed data lines. The DL0504S2-T6B0 has an ultra-low capacitance with a typical value at 0.3pF, and complies with the IEC 61000-4-2 (ESD) standard with ±15kV air and ±8kV contact discharge. It is assembled into a 6-pin lead-free SOT23-6 package. The low capacitance array make it ideal for four high speed data and transmission line. This device is optimized for ESD protection of portable electronics.

### Features

- ◆ Ultra low capacitance: 0.3pF typical (I/O to I/O)
- ◆ Ultra low leakage: nA level
- ◆ Low operating voltage: 5V
- ◆ Low clamping voltage
- ◆ Up to 4 data lines and one power line protects
- ◆ Complies with following standards:
  - IEC 61000-4-2 (ESD) immunity test  
Air discharge: ±15kV  
Contact discharge: ±8kV
  - IEC61000-4-4 (EFT) 40A (5/50ns)
  - IEC61000-4-5 (Lightning) : 4A(8/20µs)
- ◆ ROHS Compliant

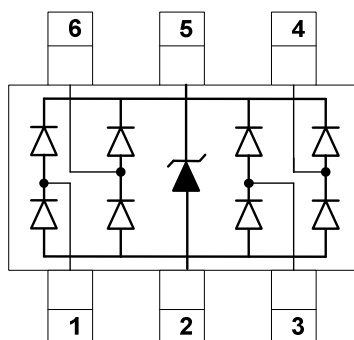
### Mechanical Characteristics

- ◆ Package: SOT23-6
- ◆ Lead Finish: Matte Tin
- ◆ UL Flammability Classification Rating 94V-0
- ◆ Case Material: “Green” Molding Compound
- ◆ Moisture Sensitivity: Level 3 per J-STD-020
- ◆ Terminal Connections: See Diagram Below
- ◆ Marking Information: See Below

### Applications

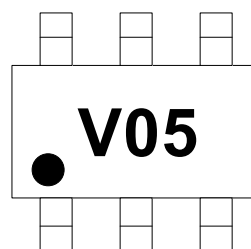
- ◆ USB 2.0 and USB 3.0 Ports
- ◆ USB OTG
- ◆ Digital video interface(DVI)
- ◆ Monitor and Flat Panel Displays
- ◆ PCI Express and Serial SATA Ports
- ◆ Gigabit Ethernet
- ◆ IEEE 1394 firewire ports
- ◆ Consumer products (STB, DVD, DSC, DVC...)

### Dimensions and Pin Configuration



Circuit and Pin Schematic

### Marking Information



V05 = Device Marking Code  
Dot denotes Pin1

### Ordering Information

Part Number	Marking	Packaging	Reel Size
DL0504S2-T6B0	V05	3000/Tape & Reel	7 inch

### **Absolute Maximum Ratings ( $T_A=25^{\circ}\text{C}$ unless otherwise specified)**

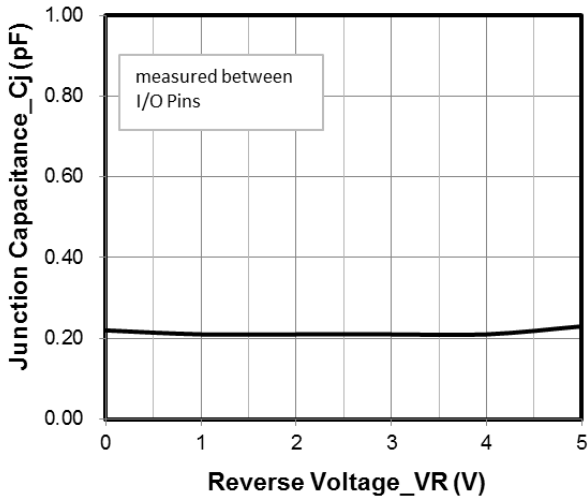
Parameter	Symbol	Value	Unit
Peak Pulse Power (tp=8/20μs)	PPP	60	W
Peak Pulse Current (tp=8/20μs)	I <sub>PP</sub>	4	A
ESD per IEC 61000-4-2 (Air)	V <sub>ESD</sub>	±15	kV
ESD per IEC 61000-4-2 (Contact)		±8	
Operating Temperature Range	T <sub>J</sub>	-55 to +125	°C
Storage Temperature Range	T <sub>stg</sub>	-55 to +150	°C

### **Electrical Characteristics ( $T_A=25^{\circ}\text{C}$ unless otherwise specified)**

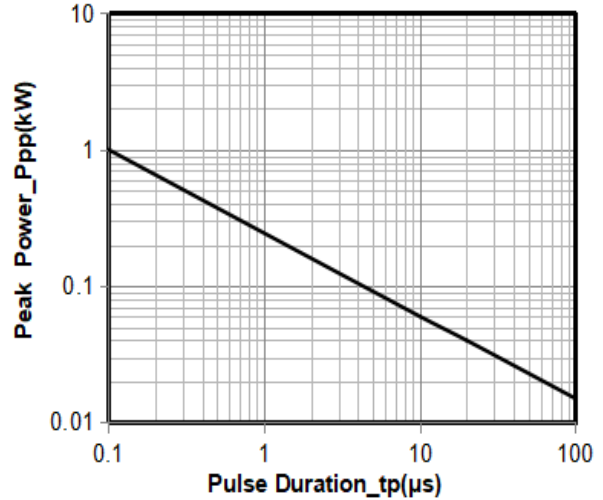
Parameter	Symbol	Min	Typ	Max	Unit	Test Condition
Reverse Working Voltage	V <sub>RWM</sub>			5	V	Any I/O pin to ground
Breakdown Voltage	V <sub>BR</sub>	6			V	I <sub>T</sub> = 1mA, any I/O pin to ground
Reverse Leakage Current	I <sub>R</sub>			0.5	μA	V <sub>RWM</sub> = 5V, any I/O pin to ground
Clamping Voltage	V <sub>C</sub>			11	V	I <sub>PP</sub> = 1A (8 x 20μs pulse) any I/O pin to ground
Clamping Voltage	V <sub>C</sub>			15	V	I <sub>PP</sub> = 4A (8 x 20μs pulse) any I/O pin to ground
Junction Capacitance	C <sub>J</sub>		0.3	0.4	pF	V <sub>R</sub> = 0V, f = 1MHz, between I/O pins
Junction Capacitance	C <sub>J</sub>			0.8	pF	V <sub>R</sub> = 0V, f = 1MHz, any I/O pin to ground

Note 1: I/O pins are Pin 1, 3, 4 and 6

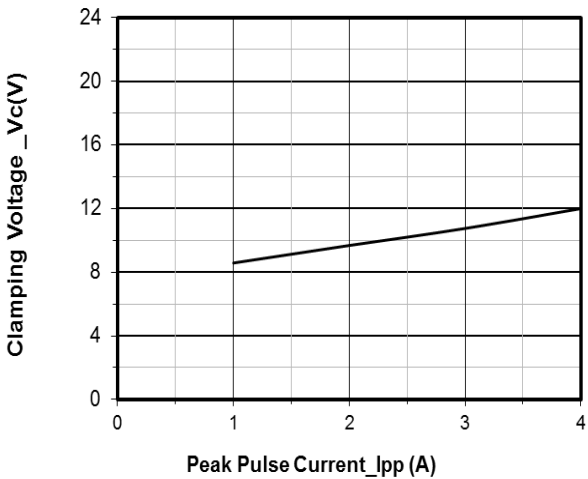
**Typical Performance Characteristics (TA=25°C unless otherwise Specified)**



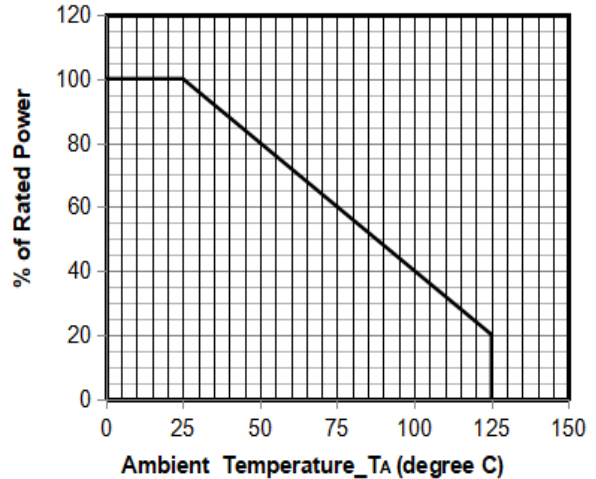
**Junction Capacitance vs. Reverse Voltage**



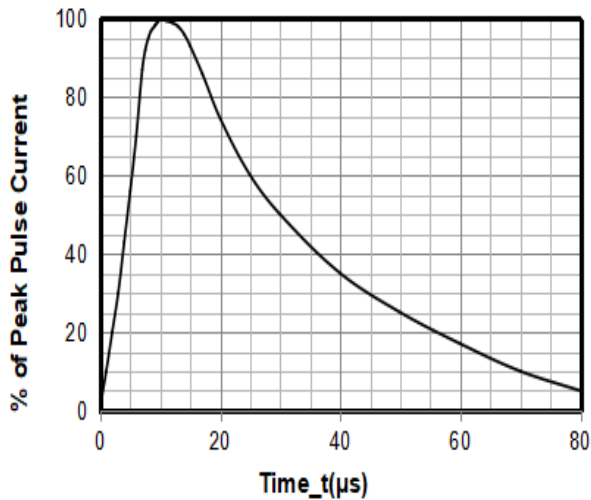
**Peak Pulse Power vs. Pulse Time**



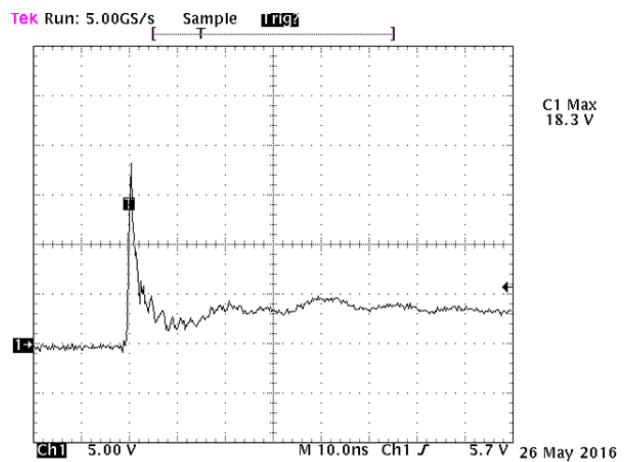
**Clamping Voltage vs. Peak Pulse Current**



**Power Derating Curve**



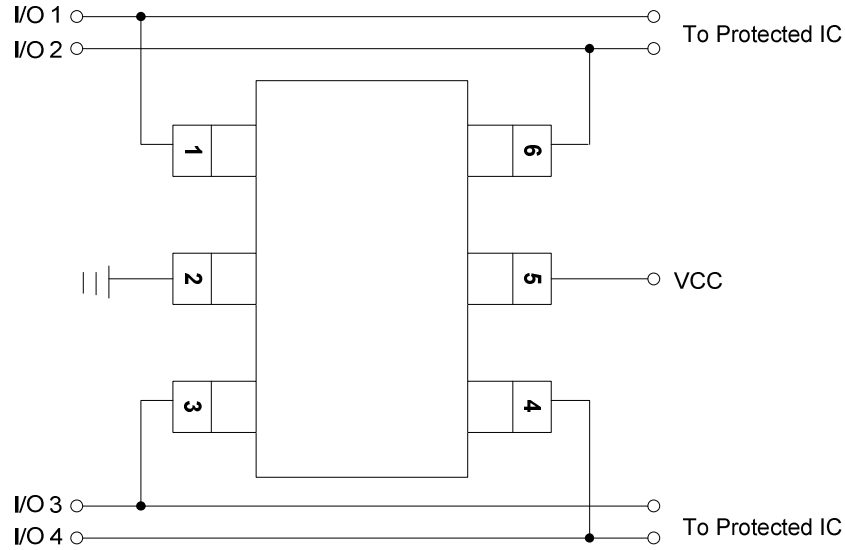
**8 X 20μs Pulse Waveform**



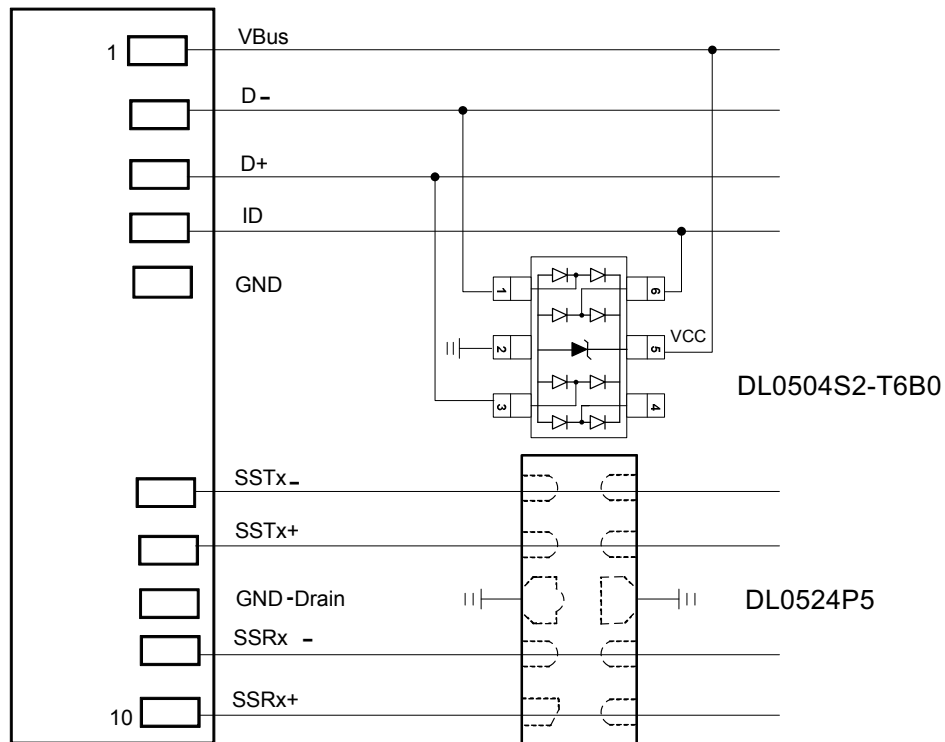
**Note: Data is taken with a 10x attenuator  
Contact discharge current waveform  
per IEC61000-4-2**

## Typical Application

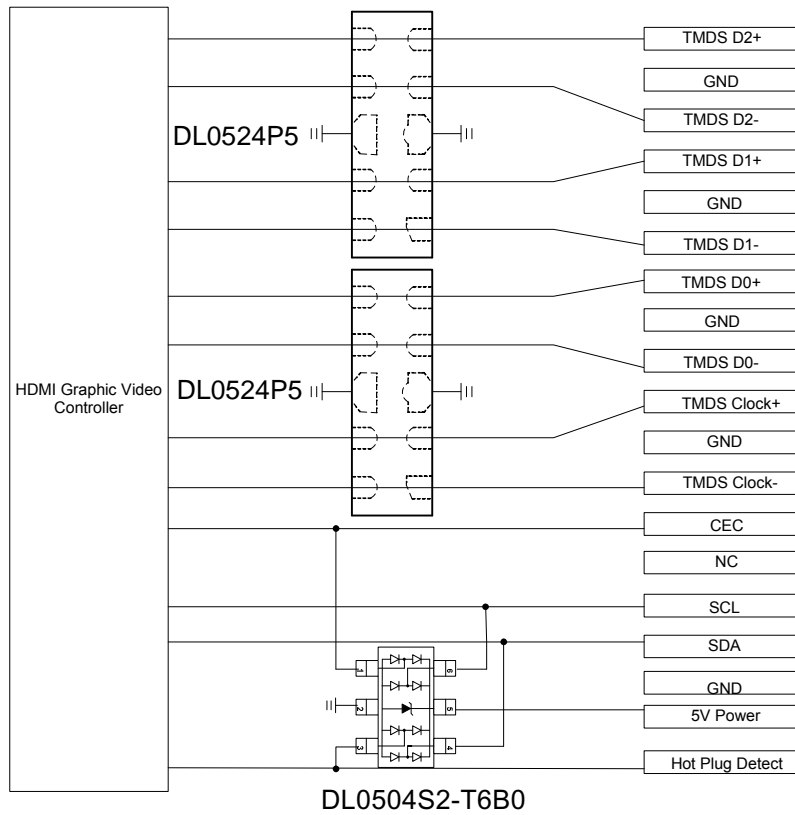
The DL0504S2-T6B0 is designed to protect four data lines from transient over-voltages by clamping them to fixed reference. When the voltage on the protected line exceeds the reference voltage (plus diode VF) the steering diodes are forward biased, conducting the transient current away from the sensitive circuitry. Data lines are connected at pins 1, 3, 4 and 6. The negative reference (REF1) is connected at pin 2. This pin should be connected directly to a ground plane on the board for best results. The path length is kept as short as possible to minimize parasitic inductance. The positive reference (REF2) is connected at pin 5.



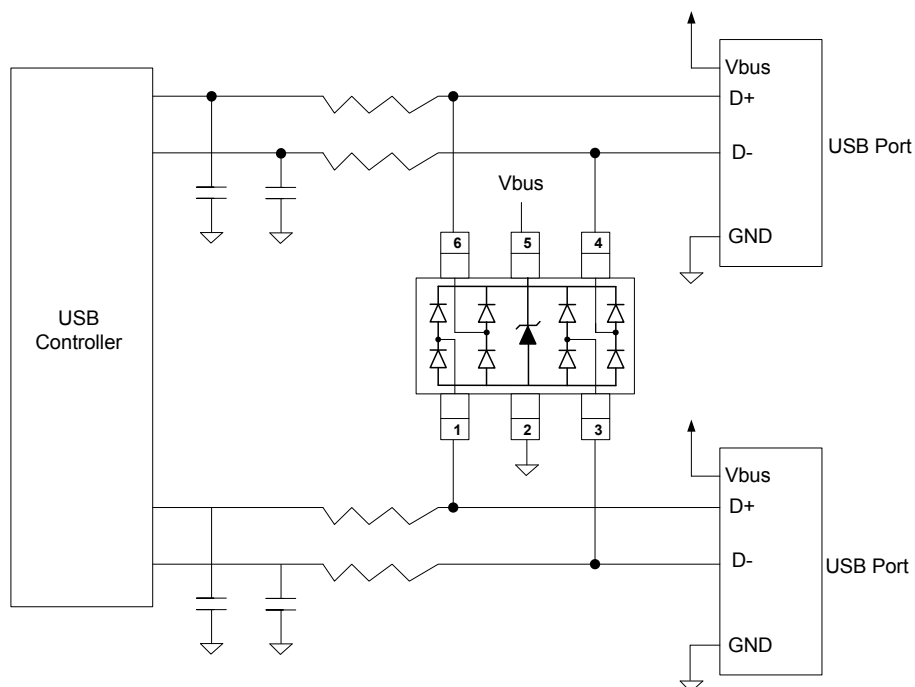
## DL0504S2-T6B0 on USB 3.0 Port Application



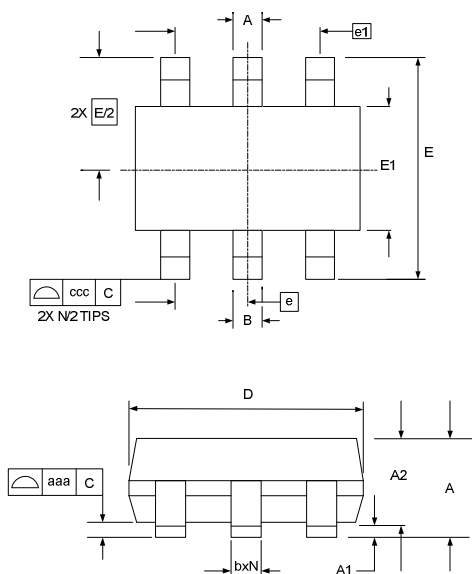
**DL0504S2-T6B0 on HDMI Port Application**



**DL0504S2-T6B0 on USB Port Application**

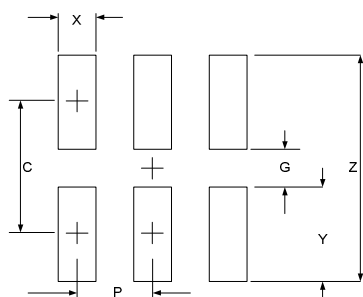


### SOT23-6 Package Outline Drawing



SYM	DIMENSIONS					
	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.90		1.45	0.035		0.057
A1	0.00		0.15	0.000		0.006
A2	0.90	1.15	1.30	0.035	0.045	0.051
b	0.25		0.50	0.010		0.020
c	0.08		0.22	0.003		0.009
D	2.80	2.90	3.10	0.110	0.114	0.122
E1	1.50	1.60	1.75	0.060	0.063	0.069
E	2.80 BSC			0.110 BSC		
e	0.95 BSC			0.037 BSC		
e1	1.90 BSC			0.075 BSC		
N	6			6		
aaa	0.10			0.004		
ccc	0.20			0.008		

### Suggested Land Pattern



SYM	DIMENSIONS	
	MILLIMETERS	INCHES
C	2.50	0.098
G	1.40	0.055
P	0.95	0.037
X	0.60	0.024
Y	1.10	0.043
Z	3.60	0.141

### Contact Information

Changzhou D-first Electronics CO.,Ltd.

www.first-electronic.com

Email: yf@first-electronic.cn

Phone: +86 (0519) -8817 1671