Preliminary

SPECIFICATION

1. Application

1)This document is applicable to the real time clock module RX-8025T that are delivered to from Seiko Epson Corp.

2)RoHS compliant

RX-8025T contains lead in high melting type solder which is exempted in RoHS directive.

3)This Product supplied (and any technical information furnished, if any) by Seiko Epson Corporation shall not be used for the development and manufacture of weapon of mass destruction or for other military purposes. Making available such products and technology to any third party who may use such products or technologies for the said purposes are also prohibited.

4)This product listed here is designed as components or parts for electronics equipment in general consumer use. We do not expect that any of these products would be incorporated or otherwise used as a component or part for the equipment, which requires an systems, and medical equipment, the functional purpose of which is to keep extra high reliability, such as satellite, rocket and other space life.

2. Product No. / Model

The product No. of this Real Time Clock Module is X1B0002810005.
The model is RX – 8025T VerD

3. Packing

It is subject to the packing standard of Seiko Epson Corp.

4. Warranty

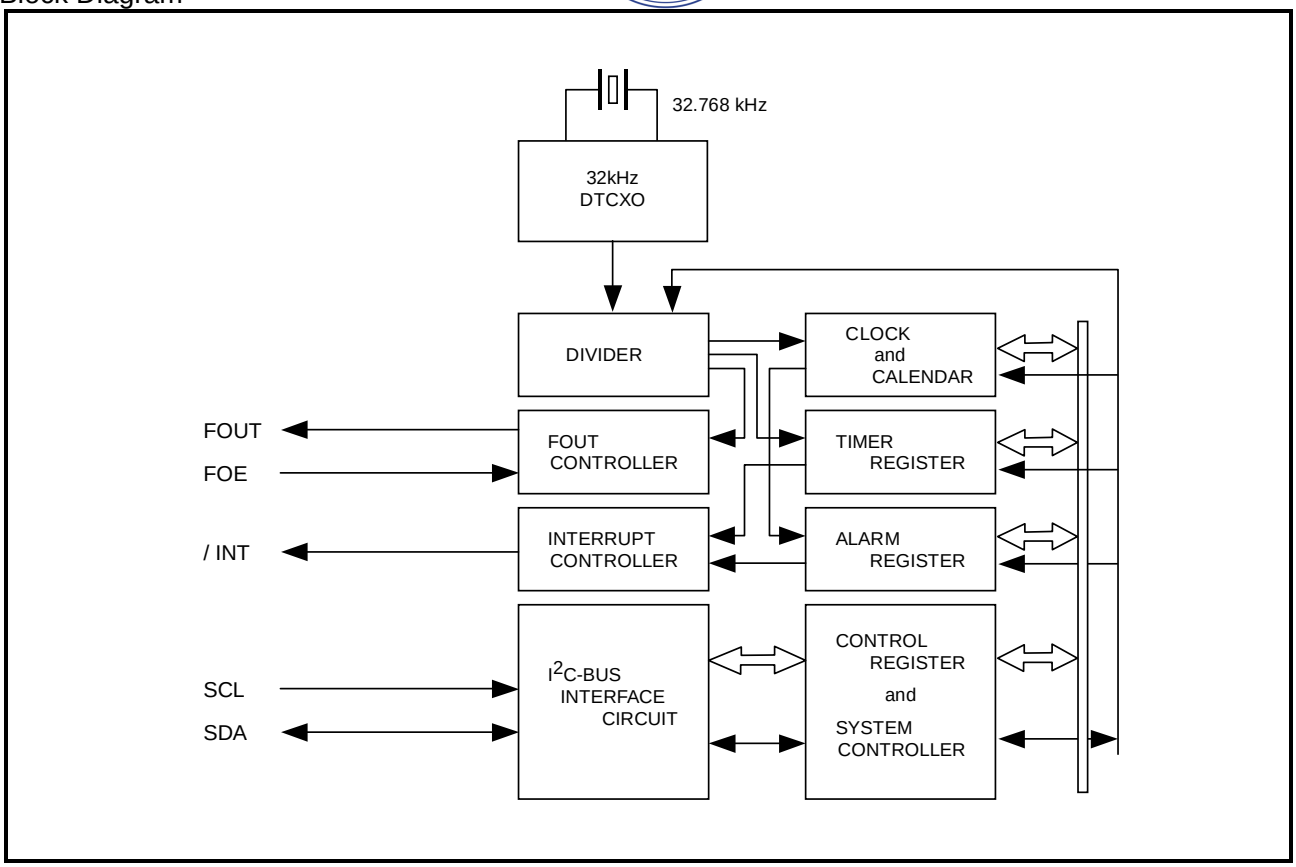
Defective parts which are originated by us are replaced free of charge in case defects are found within 12 months after delivery.

5. Amendment and abolishment

Amendment and/or abolishment of this specification are subject to the agreement of both parties.

6. Contents

1. Block Diagram

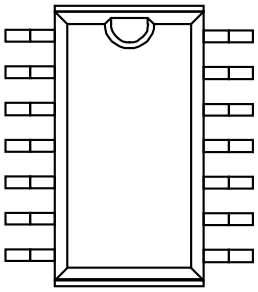


Preliminary

2. Terminal description

2.1. Terminal connections

RX – 8025T



SOP – 14pin

2.2. Pin Functions

Signal name	I/O	Function
T1	Input	* Use by the manufacture for testing. (Do not connect externally.)
SCL	Input	This is the serial clock input pin for I^2C Bus communications.
FOUT	Output	This is the C-MOS output pin with output control provided via the FOE pin. When FOE = "H" (high level), this pin outputs a 32.768 kHz signal. When output is stopped, the FOUT pin = "Hi-Z"(high impedance).
TEST	Input	* Use by the manufacture for testing. (Do not connect externally.)
VDD	–	This pin is connected to a positive power supply.
FOE	Input	This is an input pin used to control the output mode of the FOUT pin. When this pin's level is high, the FOUT pin is in output mode. When it is low, output via the FOUT pin is stopped.
/ INT	Output	This pins is used to output alarm signals, timer signals, time update signals, and other signals. This pin is an open drain pin.
GND	–	This pin is connected to a ground.
T2	–	* Use by the manufacture for testing. (Do not connect externally.)
SDA	I / O	This pin's signal is used for input and output of address, data, and ACK bits, synchronized with the serial clock used for I^2C communications. Since the SDA pin is an N-ch open drain pin during output, be sure to connect a suitable pull-up resistance relative to the signal line capacity.
N.C.	–	This pin is not connected to the internal IC. Leave N.C. pins open or connect them to GND or VDD.

Note: Be sure to connect a bypass capacitor rated at least 0.1 μF between VDD and GND.

3. Absolute Maximum Ratings

GND = 0 V

Item	Symbol	Condition	Rating	Unit
Supply voltage	V_{DD}	Between V_{DD} and GND	–0.3 to +6.5	V
Input voltage (1)	V_{IN1}	FOE pin	GND–0.3 to V_{DD}+0.3	V
Input voltage (2)	V_{IN2}	SCL and SDA pins	GND–0.3 to +6.5	V
Output voltage (1)	V_{OUT1}	FOUT pin	GND–0.3 to V_{DD}+0.3	V
Output voltage (2)	V_{OUT2}	SDA and /INT pins	GND–0.3 to +6.5	V
Storage temperature	T_{STG}	When stored separately, without packaging	–55 to +125	°C

4. Recommended Operating Conditions

GND = 0 V

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating supply voltage	V_{DD}	Interface voltage	1.6	3.0	5.5	V
Temp. compensation voltage	V_{TEM}	Temperature compensation voltage	2.2	3.0	5.5	V
Clock supply voltage	V_{CLK}	–	1.6	3.0	5.5	V
Operating temperature	T_{OPR}	No condensation	–40	+25	+85	°C

5. Frequency Characteristics

GND = 0 V

Item	Symbol	Condition		Rating	Unit
Frequency tolerance	Δf /f	UC	Ta = 0 to +50 ºC, V_{DD} = 3.0 V Ta = –30 to +70 ºC, V_{DD} = 3.0 V	± 3.8 (*1) ± 5.0 (*2)	× 10^{-6}
Frequency/voltage characteristics	f /V	Ta = +25 °C, V_{DD} = 2.2 V to 5.5 V		± 1.0 Max.	× 10^{-6} /V
Oscillation start time	tSTA	Ta = +25 °C, V_{DD} = 1.6 V Ta = –40 to +85 ºC, V_{DD} = 1.6 V to 5.5 V		1.0 Max. 3.0 Max.	s
Aging	fa	Ta = +25 °C, V_{DD} = 3.0 V, first year		± 3 Max.	× 10^{-6} / year

*1) Equivalent to 10 seconds of month deviation. *2) Equivalent to 13 seconds of month deviation.

6. Electrical Characteristics

6.1. DC Characteristics

*Unless otherwise specified, GND = 0 V, V_{DD} = 1.6 V to 5.5 V, Ta = –40 °C to +85 °C

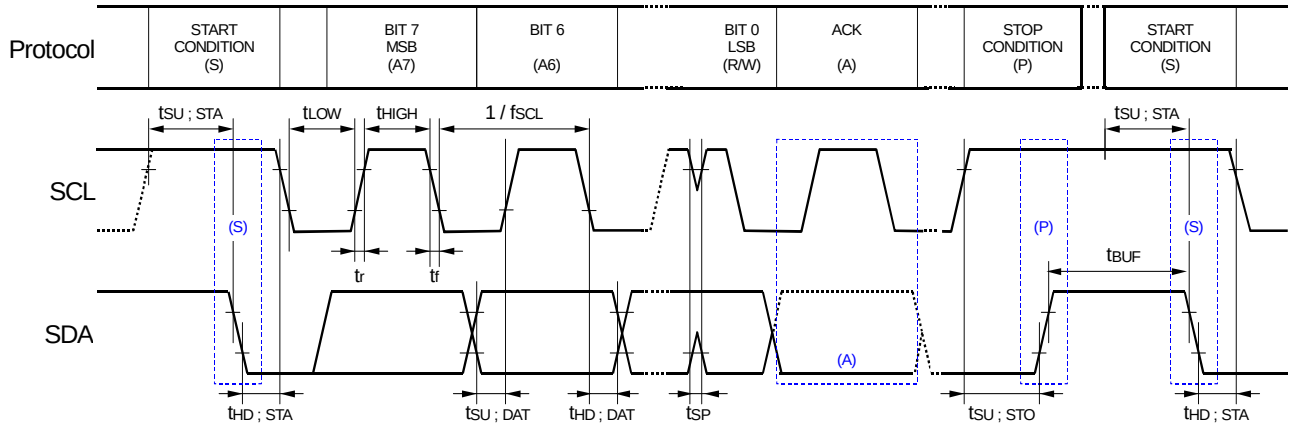
Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Current consumption (1)	I_{DD1}	f_{SCL} = 0 Hz, / INT = V_{DD} FOE = GND FOUT : output OFF (High Z) Compensation interval 2.0 s	V_{DD} = 5 V		1.2	3.4	µA
Current consumption (2)	I_{DD2}		V_{DD} = 3 V		0.8	2.1	
Current consumption (3)	I_{DD3}	f_{SCL} = 0 Hz, / INT = V_{DD} FOE = GND FOUT :32.768 kHz, CL =0pF Compensation interval 2.0 s	V_{DD} = 5 V		3.0	7.5	µA
Current consumption (4)	I_{DD4}		V_{DD} = 3 V		2.0	5.0	
Current consumption (5)	I_{DD5}	f_{SCL} = 0 Hz, / INT = V_{DD} FOE = GND FOUT :32.768 kHz, CL =30pF Compensation interval 2.0 s	V_{DD} = 5 V		8.0	20.0	µA
Current consumption (6)	I_{DD6}		V_{DD} = 3 V		5.0	12.0	
Current consumption (7)	I_{DD7}	f_{SCL} = 0 Hz, / INT = V_{DD} FOE = GND FOUT : output OFF (High Z) Compensation OFF	V_{DD} = 5 V		1.15	2.95	µA
Current consumption (8)	I_{DD8}		V_{DD} = 3 V		0.72	1.85	
Current consumption (9)	I_{DD9}	f_{SCL} = 0 Hz, / INT = V_{DD} FOE = GND FOUT : output OFF (High Z) Compensation ON (peak)	V_{DD} = 5 V		430	900	µA
Current consumption (10)	I_{DD10}		V_{DD} = 3 V		180	350	
High-level input voltage	V_{IH}	FOE pin		0.8 × V_{DD}		V_{DD} + 0.3	V
		SCL and SDA pins		0.7 × V_{DD}		5.5	
Low-level input voltage	V_{IL}	FOE pin		GND – 0.3		0.2 × V_{DD}	V
		SCL and SDA pins		GND – 0.3		0.3 × V_{DD}	
High-level output voltage	V_{OH1}	FOUT pin	V_{DD}=5 V, I_{OH}=–1 mA	4.5		5.0	V
	V_{OH2}		V_{DD}=3 V, I_{OH}=–1 mA	2.2		3.0	
	V_{OH3}		V_{DD}=3 V, I_{OH}=–100 µA	2.9		3.0	
Low-level output voltage	V_{OL1}	FOUT pin	V_{DD}=5 V, I_{OL}=1 mA	GND		GND+0.5	V
	V_{OL2}		V_{DD}=3 V, I_{OL}=1 mA	GND		GND+0.8	
	V_{OL3}		V_{DD}=3 V, I_{OL}=100 µA	GND		GND+0.1	
	V_{OL4}	/ INT pin	V_{DD}=5 V, I_{OL}=1 mA	GND		GND+0.25	V
	V_{OL5}		V_{DD}=3 V, I_{OL}=1 mA	GND		GND+0.4	
	V_{OL6}	SDA pin	V_{DD} ≥2 V, I_{OL}=3 mA	GND		GND+0.4	V
Input leakage current	I_{LK}	FOE, SCL, SDA pins , V_{IN} = V_{DD} or GND		–0.5		0.5	µA
Output leakage current	I_{OZ}	/ INT, SDA, FOUT pins, V_{OUT} = V_{DD} or GND		–0.5		0.5	µA

6.2. AC Characteristics

* Unless otherwise specified,
GND = 0 V , V_{DD} = 1.8 V to 5.5 V , Ta = –40 °C to +85 °C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
SCL clock frequency	f_{SCL}				400	kHz
Start condition setup time	$t_{SU;STA}$		0.6			µs
Start condition hold time	$t_{HD;STA}$		0.6			µs
Data setup time	$t_{SU;DAT}$		100			ns
Data hold time	$t_{HD;DAT}$		0		900	ns
Stop condition setup time	$t_{SU;STO}$		0.6			µs
Bus idle time between start condition and stop condition	t_{BUF}		1.3			µs
Time when SCL = "L"	t_{LOW}		1.3			µs
Time when SCL = "H"	t_{HIGH}		0.6			µs
Rise time for SCL and SDA	t_r				0.3	µs
Fall time for SCL and SDA	t_f				0.3	µs
Allowable spike time on bus	t_{SP}				50	ns
FOUT duty	t_W /t	50% of V_{DD} level	40	50	60	%

Timing chart



Caution: When accessing this device, all communication from transmitting the start condition to transmitting the stop condition after access **should be completed within 0.95 seconds**.
If such communication requires **0.95 seconds** or longer, the I^2C bus interface is reset by the internal bus timeout function.

7. Register table

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Remark
0	SEC	○	40	20	10	8	4	2	1	∗3
1	MIN	○	40	20	10	8	4	2	1	∗3
2	HOUR	○	○	20	10	8	4	2	1	∗3
3	WEEK	○	6	5	4	3	2	1	0	∗3
4	DAY	○	○	20	10	8	4	2	1	∗3
5	MONTH	○	○	○	10	8	4	2	1	∗3
6	YEAR	80	40	20	10	8	4	2	1	–
7	RAM	•	•	•	•	•	•	•	•	∗4
8	MIN Alarm	AE	40	20	10	8	4	2	1	–
9	HOUR Alarm	AE	•	20	10	8	4	2	1	∗4
A	WEEK Alarm	AE	6	5	4	3	2	1	0	∗4
	DAY Alarm		•	20	10	8	4	2	1	
B	Timer Counter 0	128	64	32	16	8	4	2	1	–
C	Timer Counter 1	•	•	•	•	2048	1024	512	256	∗4
D	Extension Register	TEST	WADA	USEL	TE	FSEL1	FSEL0	TSEL1	TSEL0	∗1, ∗3, ∗5
E	Flag Register	○	○	UF	TF	AF	○	VLF	VDET	∗1, ∗2, ∗3
F	Control Register	CSEL1	CSEL0	UIE	TIE	AIE	○	○	RESET	∗3

Note When after the initial power-up or when the result of read out the VLF bit is "1" , initialize all registers, before using the module.
Be sure to avoid entering incorrect date and time data, as clock operations are not guaranteed when the data or time data is incorrect.

∗1) During the initial power-up, the TEST bit is reset to "0" and the VLF bit is set to "1".
∗ At this point, all other register values are undefined, so be sure to perform a reset before using the module.

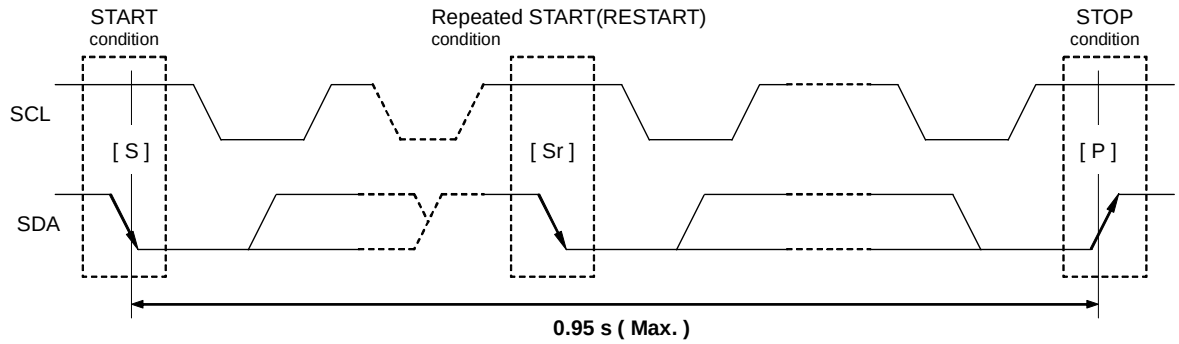
∗2) Only a "0" can be written to the UF, TF, AF, VLF, or VDET bit.

∗3) Any bit marked with "○" should be used with a value of "0" after initialization.

∗4) Any bit marked with "•"(is a RAM bit that can be used to read or write any data.

∗5) The TEST bit is used by the manufacturer for testing. Be sure to set "0" for this bit when writing.

7.1. Starting and stopping I²C bus communications



1) START condition, repeated START condition, and STOP condition

(1) START condition

- The SDA level changes from high to low while SCL is at high level.

(2) STOP condition

- This condition regulates how communications on the I²C-BUS are terminated. The SDA level changes from low to high while SCL is at high level.

(3) Repeated START condition (RESTART condition)

- In some cases, the START condition occurs between a previous START condition and the next STOP condition, in which case the second START condition is distinguished as a RESTART condition. Since the required status is the same as for the START condition, the SDA level changes from high to low while SCL is at high level.

2) Caution points

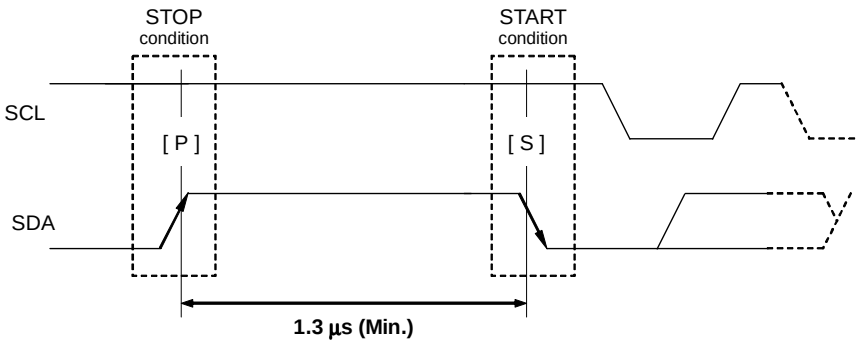
∗1) The master device always controls the START, RESTART, and STOP conditions for communications.

∗2) The master device does not impose any restrictions on the timing by which STOP conditions affect transmissions, so communications can be forcibly stopped at any time while in progress. (However, this is only when this RTC module is in receiver mode (data reception mode = SDA released).

∗3) When communicating with this RTC module, the series of operations from transmitting the START condition to transmitting the STOP condition should occur **within 0.95 seconds**. (A RESTART condition may be sent between a START condition and STOP condition, but even in such cases the series of operations from transmitting the START condition to transmitting the STOP condition should still occur **within 0.95 seconds**.)

If this series of operations requires **0.95 seconds or longer,** the I²C bus interface will be automatically cleared and set to standby mode by this RTC module's bus timeout function. Note with caution that both write and read operations are invalid for communications that occur during or after this auto clearing operation. (When the read operation is invalid, all data that is read has a value of "1").
Restarting of communications begins with transfer of the START condition again

∗4) When communicating with this RTC module, wait **at least 1.3 µs (see the tBUF rule)** between transferring a STOP condition (to stop communications) and transferring the next START condition (to start the next round of communications).



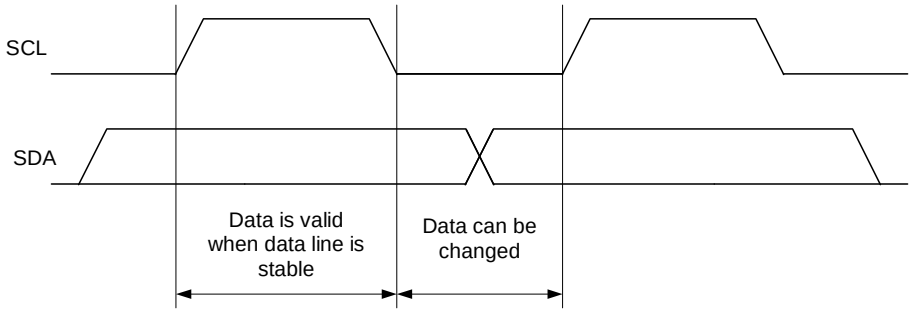
7.2. Data transfers and acknowledge responses during I²C-BUS communications

1) Data transfers

Data transfers are performed in 8-bit (1 byte) units once the START condition has occurred. There is no limit on the amount (bytes) of data that are transferred between the START condition and STOP condition.
(**However, the transfer time must be no longer than 0.95 seconds**.)

The address auto increment function operates during both write and read operations.
After address Fh, incrementation goes to address 0h.

Updating of data on the transmitter (transmitting side)'s SDA line is performed while the SCL line is at low level. The receiver (receiving side) receives data while the SCL line is at high level.

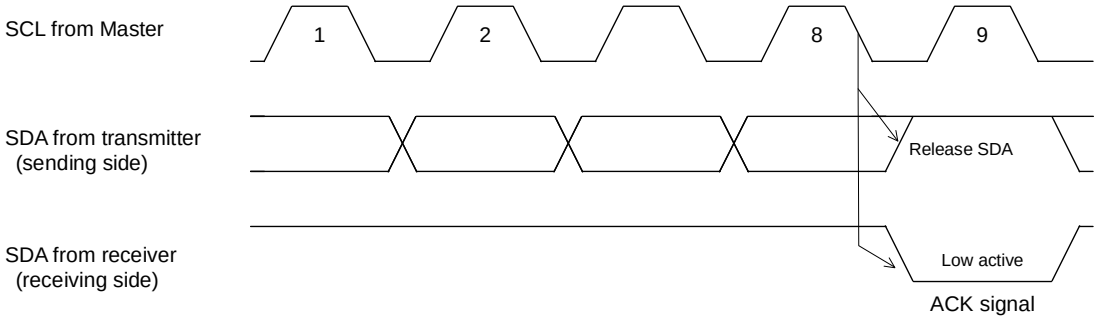


∗ Note with caution that if the SDA data is changed while the SCL line is at high level, it will be treated as a START, RESTART, or STOP condition.

2) Data acknowledge response (ACK signal)

When transferring data, the receiver generates a confirmation response (ACK signal, low active) each time an 8-bit data segment is received. If there is no ACK signal from the receiver, it indicates that normal communication has not been established. (This does not include instances where the master device intentionally does not generate an ACK signal.)

Immediately after the falling edge of the clock pulse corresponding to the 8th bit of data on the SCL line, the transmitter releases the SDA line and the receiver sets the SDA line to low (= acknowledge) level.



After transmitting the ACK signal, if the Master remains the receiver for transfer of the next byte, the SDA is released at the falling edge of the clock corresponding to the 9th bit of data on the SCL line. Data transfer resumes when the Master becomes the transmitter.
When the Master is the receiver, if the Master does not send an ACK signal in response to the last byte sent from the slave, that indicates to the transmitter that data transfer has ended. At that point, the transmitter continues to release the SDA and awaits a STOP condition from the Master.

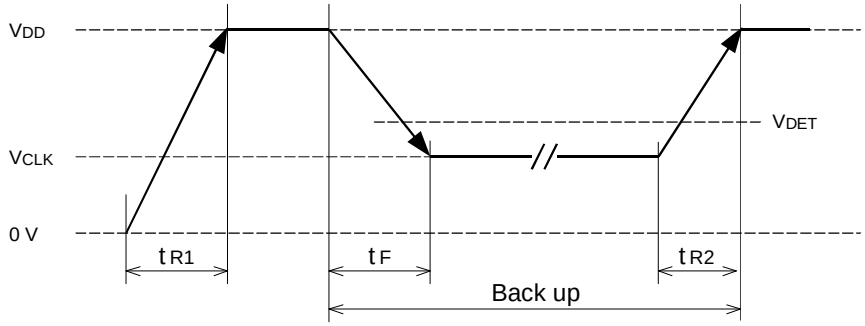
7.3. Slave address

The I²C bus device does not include a chip select pin such as is found in ordinary logic devices. Instead of using a chip select pin, slave addresses are allocated to each device.
All communications begin with transmitting the [START condition] + [slave address (+ R/W specification)]. The receiving device responds to this communication only when the specified slave address it has received matches its own slave address.

Slave addresses have a fixed length of 7 bits. This RTC's slave address is **[0110 010∗]**.
An R/W bit ("*" above) is added to each 7-bit slave address during 8-bit transfers.

	Transfer data	Slave address							R/W bit
		bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Read	**65 h**	**0**	**1**	**1**	**0**	**0**	**1**	**0**	1 (= Read)
Write	**64 h**								0 (= Write)

7.4. Backup and Recovery



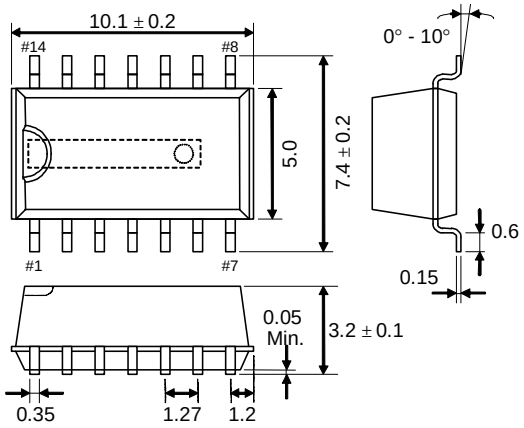
Item	Symbol	Condition	Min.	Typ.	Max.	Unit.
Power supply detection voltage (1)	V_{DET}	–			2.2	V
Power supply detection voltage (2)	V_{LOW}	–			1.6	V
Power supply drop time	t_F	–	2			µs /V
Initial power-up time	t_{R1}	–			10	ms /V
Clock maintenance power-up time	t_{R2}	1.6V → VDD ≤ 3.6V	5			µs /V
		1.6V → VDD > 3.6V	15			µs /V

8. External Dimensions / Marking Layout

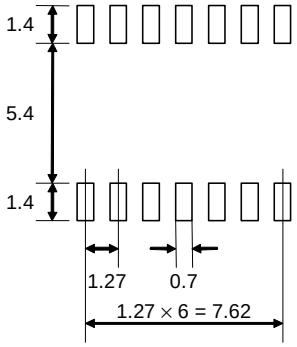
8.1. External dimensions

RX-8025T (SOP - 14 pin)

• External dimensions



• Recommended soldering

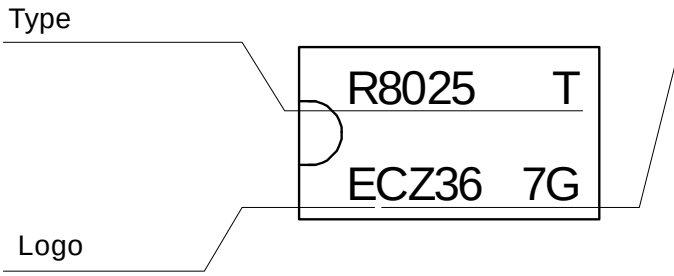


Unit : mm

∗ The crystal oscillator's metal case may be visible in the area (on top) indicated in broken lines ┈┈┈, but this has no effect on the device's characteristics.

8.2. Marking layout

RX – 8025T (SOP-14pin)



Production lot

C Z 36 7C
① ② ③ ④

① Frequency tolerance [C]:UC
Ta= 0 ~ +50 °C, V_{DD}=3.0 V
(± 3.8) × 10^{-6}
Ta=–30 ~ +70 °C, V_{DD}=3.0 V
(± 5.0) × 10^{-6}

② The last digit of the year
③ Week of the year
④ Internal ID Code

∗ Marking (year part lot No.) will be changed as follows.

Year digit	1	2	3	4	5	6	7	8	9	0
Marking (Sn plating Terminal)	M	N	R	S	T	U	V	W	X	Z
Marking (SnAg plating Terminal)	A	B	C	D	E	F	G	H	J	K

∗ Contents displayed indicate the general markings and display, but are not the standards for the fonts, sizes and positioning.

9. Environmental and mechanical characteristics

(The company evaluation condition　We evaluate it by the following examination item and examination condition.)

No.	Item	Value *1		Test Conditions
		Δ f / f [1×10^{-6}] *2	Electrical characteristics	
1	High temperature storage	*3　± 50	*4	+125 °C × 1 000 h
2	Low temperature storage	*3　± 10		-55 °C × 1 000 h
3	High temperature bias	*3　± 20		+85 °C × 5.5 V × 1 000 h
4	Low temperature bias	*3　± 10		-40 °C × 5.5 V × 1 000 h
5	Temperature humidity bias	*3　± 20		+85 °C × 85 %RH × 5.5 V × 1 000 h
6	Temperature cycle	*3　± 10		-55 °C ⇔ +125 °C 30 min at each temp. 100 cycles
7	Resistance to soldering heat	± 8		For convention reflow soldering furnace (3 times) Follow　JEDEC J-STD-020C
8	Drop	± 5		Free drop from 750 mm height on a hard wooden board for 3 times (Board is thickness more than 30 mm)
9	Vibration	± 5		10 Hz to 55 Hz amplitude 0.75 mm 55 Hz to 500 Hz　acceleration 98 m/s^2 10 Hz → 500 Hz → 10 Hz 15min./cycle 6 h (2 hours , 3 directions)
10	Flexibility of termination	No defect for wire termination		Put weight of 2.5 N on top of the termination Bending following angle :+90 ° to -90 ° to 0
11	Solderability	Termination must be 95 % covered with fresh solder		Dip termination into solder bath at +235 ℃ ± 5 ℃ for 5 s (Using Rosin Flux)
12	Solvent resistance	The marking shall be legible		Ref. JIS C 0052 or IEC 60068-2-45

< Notes >

1. *1 Each test done independently.
2. *2 Measuring 2 h to 24 h later leaving in room temperature after each test.
3. *3 Pre conditionings
   1. +125 °C × 24 h to +85 °C × 85 % × 168 h → reflow 3 times
   2. Initial value shall be after 24 h at room temperature.
4. *4 Satisfy item【5】Frequency characteristics (exclude Frequency stability and Aging) and item【6】Electrical characteristics after test

♦ Air-reflow condition (Follow JEDEC J-STD-020C)