MIC2182

High-Efficiency Synchronous Buck Controller

Features

- 4.5V to 32V Input Voltage Range
- 1.25V to 6V Output Voltage Range
- 95% Efficiency
- 300 kHz Oscillator Frequency
- Current Sense Blanking
- 5Ω Impedance MOSFET Drivers
- Drives N-channel MOSFETs
- 600 µA Typical Quiescent Current (Skip-Mode)
- Logic Controlled Micropower Shutdown (I_Q < 0.1 µA)
- Current-Mode Control
- Cycle-by-Cycle Current Limiting
- Built-In Undervoltage Protection
- Adjustable Undervoltage Lockout
- Easily Synchronizable
- Precision 1.245V Reference Output
- 0.6% Total Regulation
- 16-Lead SOIC and SSOP Packages
- Frequency Foldback Overcurrent Protection
- Sustained Short-Circuit Protection at Any Input Voltage
- 20A Output Current Capability

Applications

- DC Power Distribution Systems
- Notebook and Subnotebook Computers
- PDAs and Mobile Communicators
- Wireless Modems
- Battery-Operated Equipment

General Description

The MIC2182 is a synchronous buck (step-down) switching regulator controller. An all N-channel synchronous architecture and powerful output drivers allow up to a 20A output current capability. The PWM and skip-mode control scheme allows efficiency to exceed 95% over a wide range of load current, making it ideal for battery powered applications, as well as high current distributed power supplies.

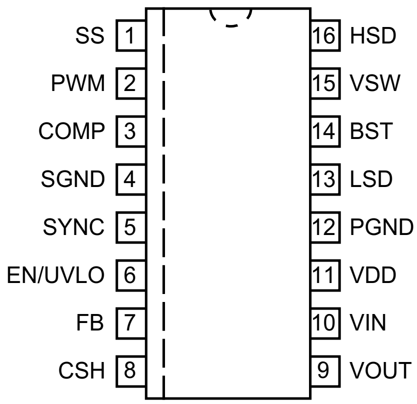
The MIC2182 operates from a 4.5V to 32V input and can operate with a maximum duty cycle of 86% for use in low- dropout conditions. It also features a shutdown mode that reduces quiescent current to 0.1 µA.

The MIC2182 achieves high efficiency over a wide output current range by automatically switching between PWM and skip mode. Skip-mode operation enables the converter to maintain high efficiency at light loads by turning off circuitry pertaining to PWM operation, reducing the no-load supply current from 1.6 mA to 600 µA. The operating mode is internally selected according to the output load conditions. Skip mode can be defeated by pulling the PWM pin low which reduces noise and RF interference.

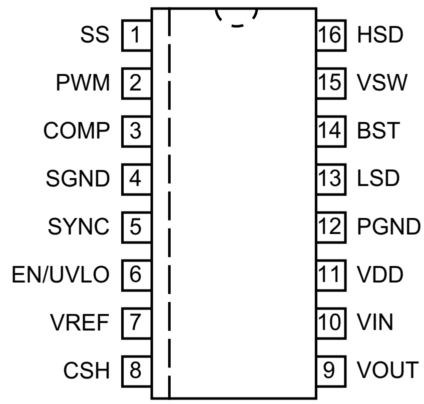
The MIC2182 is available in a 16-lead SOIC (small-outline package) and SSOP (shrink small-outline package) with an operating ambient temperature range from –40°C to +85°C.

Package Types

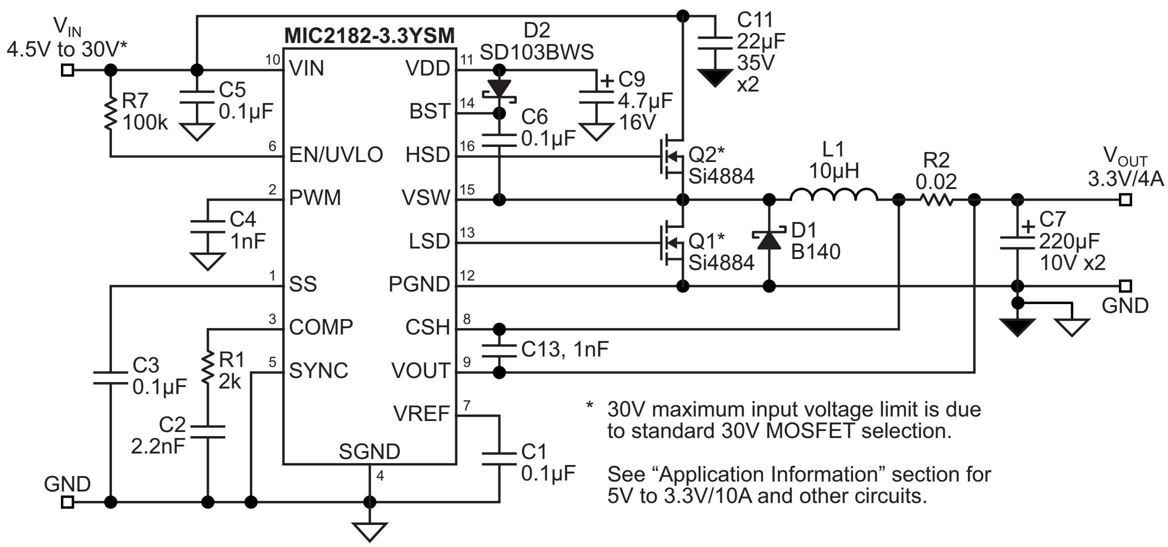
MIC2182 (Adjustable)
16-Lead SOIC(M)
16-Lead SSOP (SM)



MIC2182 (Fixed)
16-Lead SOIC(M)
16-Lead SSOP (SM)

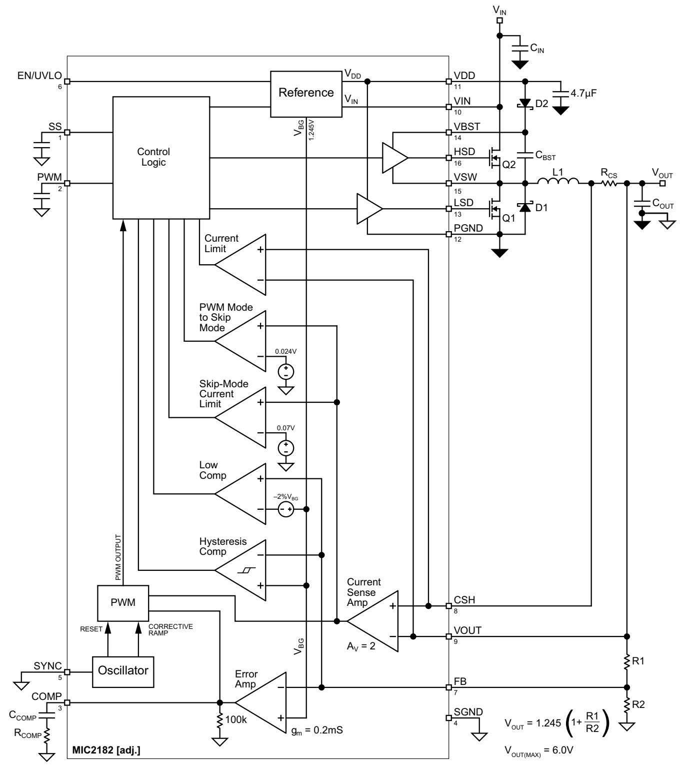


Typical Application Circuit

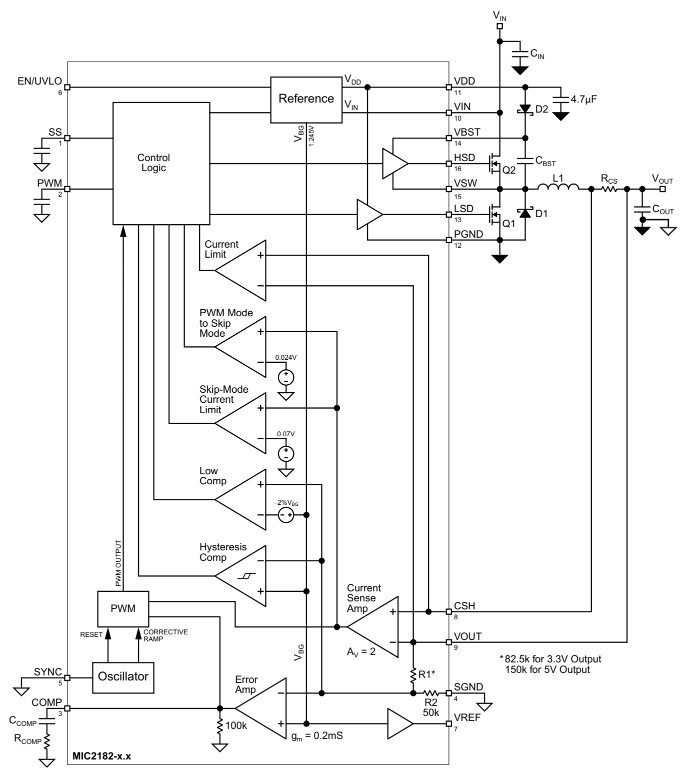


Block Diagrams

Adjustable Output Voltage Version



Fixed Output Voltage Version



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Analog Supply Voltage (V_{IN}) ....+34V
Digital Supply Voltage (V_{DD}) ....+7V
Driver Supply Voltage (B_{ST}) .... V_{IN} +7V
Sense Voltage (V_{OUT}, C_{SH}).................... 7V to –0.3V
Sync Pin Voltage (V_{SYNC}) .... 7V to –0.3V
Enable Pin Voltage ($V_{EN/UVLO}$) ....V_{IN}
Power Dissipation (P_D)
SOIC .... 400 mW @ T_A = 85°C
SSOP .... 270 mW @ T_A = 85°C
ESD Rating .... (Note 1)

Operating Ratings ‡

Analog Supply Voltage (V_{IN}) .... +4.5V to +32V

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability. Specifications are for packaged product only.

‡ Notice: The device is not guaranteed to function outside its operating ratings.

Note 1: Devices are ESD sensitive. Handling precautions are recommended. Human body model, 1.5 kΩ in series with 100 pF.

ELECTRICAL CHARACTERISTICS

Electrical Characteristics: V_{IN} = 15V; SS = Open; V_{SHDN} = 5V; I_{LOAD} = 0.1A, T_A = +25°C, **Bold** values indicate –40°C ≤ T_A ≤ +85°C; unless otherwise specified.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
MIC2182 (Adjustable) (Note 1)						
Feedback Voltage Reference	V_{REF}	1.233	1.245	1.257	V	—
		1.220	1.245	**1.270**	V	—
		1.208	1.245	**1.282**	V	4.5V < V_{IN} < 32V, full load range, 0 mV < V_{CSH} – V_{OUT} < 75 mV
Feedback Bias Current	I_{FB}	—	10	—	nA	—
Output Voltage Range	V_{OUT}	**1.25**	—	**6**	V	—
Output Voltage Line Regulation	ΔV_{O_LN}	—	0.03	—	%/V	V_{IN} = 4.5V to 32V, V_{CSH} – V_{OUT} = 50 mV
Output Voltage Load Regulation	ΔV_{O_LD}	—	0.5	—	%	25 mV < (V_{CSH} – V_{OUT}) < 75 mV (PWM mode only)
Output Voltage Total Regulation	ΔV_{O_TOT}	—	0.6	—	%	0 mV < (V_{CSH} – V_{OUT}) < 75 mV (full load range), 4.5V < V_{IN} < 32V
MIC2182-3.3						
Output Voltage	V_{OUT}	3.267	3.3	3.333	V	—
		3.234	3.3	**3.366**	V	—
		3.201	3.3	**3.399**	V	4.5V < V_{IN} < 32V, full load range, 0 mV < V_{CSH} – V_{OUT} < 75 mV
Output Voltage Line Regulation	ΔV_{O_LN}	—	0.03	—	%/V	V_{IN} = 4.5V to 32V, V_{CSH} – V_{OUT} = 50 mV
Output Voltage Load Regulation	ΔV_{O_LD}	—	0.5	—	%	25 mV < (V_{CSH} – V_{OUT}) < 75 mV (PWM mode only)

ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: V_{IN} = 15V; SS = Open; V_{SHDN} = 5V; I_{LOAD} = 0.1A, T_A = +25°C, **Bold** values indicate –40°C ≤ T_A ≤ +85°C; unless otherwise specified.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Output Voltage Total Regulation	ΔV_{O_TOT}	—	0.8	—	%	0 mV < (V_{CSH} – V_{OUT}) < 75 mV (full load range), 4.5V < V_{IN} < 32V
MIC2182-5.0						
Output Voltage	V_{OUT}	4.95	5.0	5.05	V	—
		4.90	5.0	**5.10**	V	—
		4.85	5.0	**5.150**	V	6.5V < V_{IN} < 32V, full load range, 0 mV < V_{CSH} – V_{OUT} < 75 mV
Output Voltage Line Regulation	ΔV_{O_LN}	—	0.03	—	%/V	V_{IN} = 6.5V to 32V, V_{CSH} – V_{OUT} = 50 mV
Output Voltage Load Regulation	ΔV_{O_LD}	—	0.5	—	%	25 mV < (V_{CSH} – V_{OUT}) < 75 mV (PWM mode only)
Output Voltage Total Regulation	ΔV_{O_TOT}	—	0.8	—	%	0 mV < (V_{CSH} – V_{OUT}) < 75 mV (full load range), 6.5V < V_{IN} < 32V
Input and VDD Supply Quiescent Current						
PWM Mode Quiescent Current	I_{Q_PWM}	—	1.6	**2.5**	mA	V_{PWM} = 0V, excluding external MOSFET gate drive current
Skip Mode Quiescent Current	I_{Q_SKIP}	—	600	**1500**	µA	I_{LOAD} = 0 mA, V_{PWM} floating (1 nF capacitor to ground)
Shutdown Quiescent Current	I_{SD}	—	0.1	**5**	µA	$V_{EN/UVLO}$ = 0V
Digital Supply Voltage	V_{DD}	4.7	—	5.3	V	I_{LOAD} = 0 mA to 5 mA
Undervoltage Lockout	V_{DDUV_R}	—	4.2	—	V	V_{DD} upper threshold (turn-on threshold)
	V_{DDUV_F}	—	4.1	—	V	V_{DD} lower threshold (turn-off threshold)
Reference Output (Fixed Versions Only						
Reference Voltage	V_{REF}	**1.220**	1.245	**1.270**	V	—
Reference Line Regulation	ΔV_{REF_LN}	—	1	—	mV	6V < V_{IN} < 32V
Reference Load Regulation	ΔV_{REF_LD}	—	2	—	mV	0 µA < I_{REF} < 100 µA
Enable/UVLO						
Enable Input Threshold	V_{EN_TH}	**0.6**	1.1	**1.6**	V	—
UVLO Threshold	V_{ENUV_TH}	**2.2**	2.5	**2.8**	V	—
Enable Input Current	I_{EN}	—	0.1	**5**	µA	$V_{EN/UVLO}$ = 5V
Soft-Start						
Soft-Start Source Current	I_{SS}	–3.5	–5	–6.5	µA	V_{SS} = 0V
Current Limit						
Current Limit Threshold Voltage	V_{ILIM_TH}	75	100	135	mV	V_{CSH} = V_{OUT}
Error Amplifier						
Error Amplifier Voltage Gain	$A_{V(EA)}$	—	20	—	V/V	$g_{m(EA)}$ = 0.2 mS, $R_{O(EA)}$ = 100 kΩ
Current Amplifier						
Current Sense Amplifier Gain	$A_{V(CS)}$	—	2.0	—	V/V	—
Oscillator Section						
Oscillator Frequency	f_{OSC}	270	300	330	kHz	—
Maximum Duty Cycle	D_{MAX}	—	86	—	%	—
Minimum On-Time	$t_{ON(MIN)}$	—	140	**250**	ns	V_{OUT} = $V_{OUT(NOMINAL)}$ + 200 mV

ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: V_{IN} = 15V; SS = Open; V_{SHDN} = 5V; I_{LOAD} = 0.1A, T_A = +25°C, **Bold** values indicate –40°C ≤ T_A ≤ +85°C; unless otherwise specified.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
SYNC Threshold Level	V_{SYNC_TH}	**0.7**	1.3	**1.9**	V	—
SYNC Input Current	I_{SYNC}	—	0.1	**5**	µA	V_{SYNC} = 5V
SYNC Minimum Pulse Width	$t_{SYNC(MIN)}$	200	—	—	ns	—
SYNC Capture Range	f_{SYNC}	330	—	—	kHz	Note 2
Frequency Foldback Threshold	V_{FOLD_TH}	0.75	0.95	1.15	V	Measured at V_{OUT} Pin
Foldback Frequency	f_{FOLD}	—	60	—	kHz	—
Gate Drivers						
Rise/Fall Time	t_R, t_F	—	60	—	ns	C_{LOAD} = 3000 pF
Output Driver Impedance	R_{ON_H}	—	5	**8.5**	Ω	Source
	R_{ON_L}	—	3.5	**6**		Sink
Driver Non-overlap Time	t_{NON}	—	80	—	ns	—
PWM Input						
PWM Input Source Current	I_{PWM_SRC}	—	–10	—	µA	V_{PWM} = 0V

1: V_{IN} > 1.3 x V_{OUT} (for the feedback voltage reference and output voltage line and total regulation).

2: See the Oscillator and Sync section for limitations on the synchronizing signal frequency.

TEMPERATURE SPECIFICATIONS (Note 1)

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Ambient Storage Temperature Range	T_S	–65	—	+150	°C	—
Ambient Temperature Range	T_A	–40	—	+85	°C	—
Junction Temperature Range	T_J	–40	—	+125	°C	—
Package Thermal Resistances						
Thermal Resistance SOIC 16-Ld	θ_{JA}	—	100	—	°C/W	—
Thermal Resistance SSOP 16-Ld	θ_{JA}	—	150	—	°C/W	—

Note 1: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +125°C rating. Sustained junction temperatures above +125°C can impact the device reliability.

2.0 TYPICAL PERFORMANCE CURVES

Note:	The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

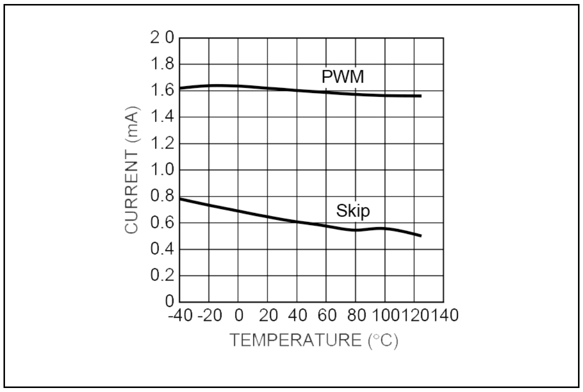


FIGURE 2-1: Quiescent Current vs. Temperature.

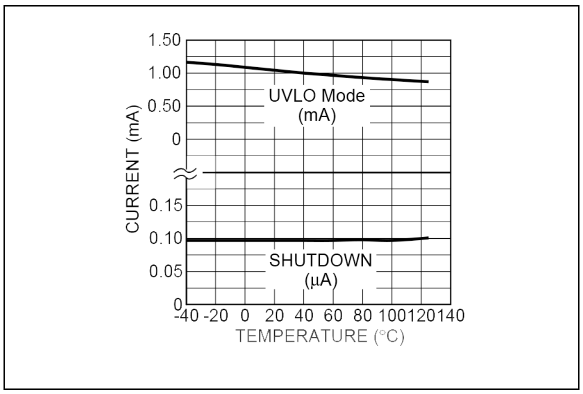


FIGURE 2-2: Quiescent Current vs. Temperature.

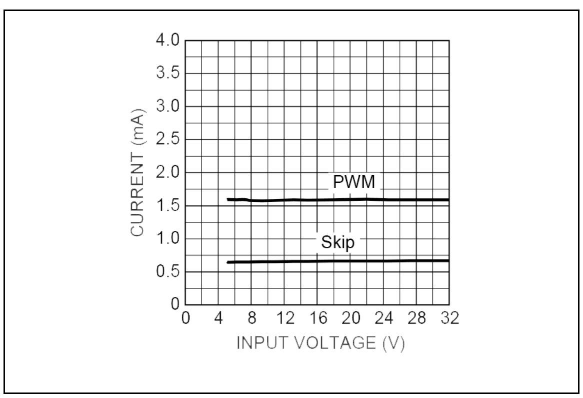


FIGURE 2-3: Quiescent Current vs. Supply Voltage.

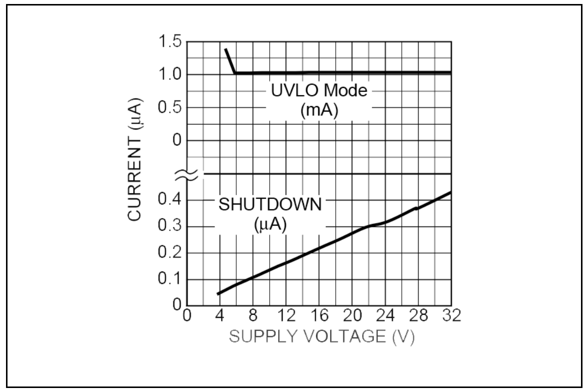


FIGURE 2-4: Quiescent Current vs. Supply Voltage.

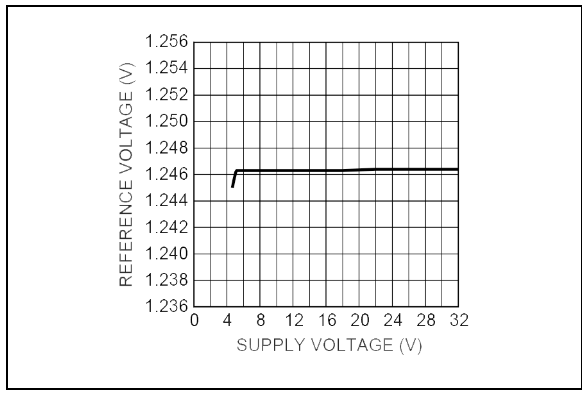


FIGURE 2-5: V_{REF} (Fixed Versions) Line Regulation.

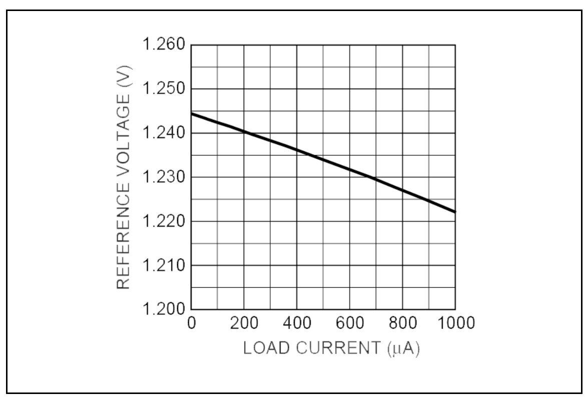


FIGURE 2-6: V_{REF} (Fixed Versions) Load Regulation.

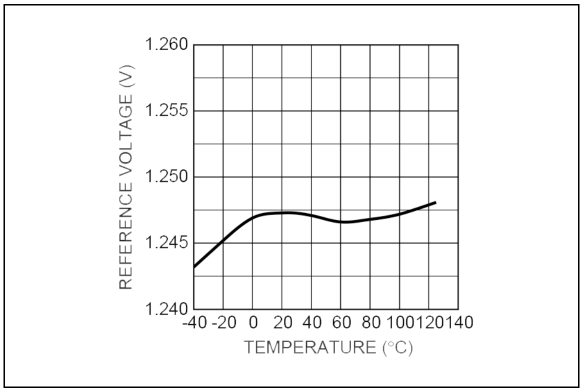


FIGURE 2-7: *V_{REF} (Fixed Versions) vs. Temperature.*

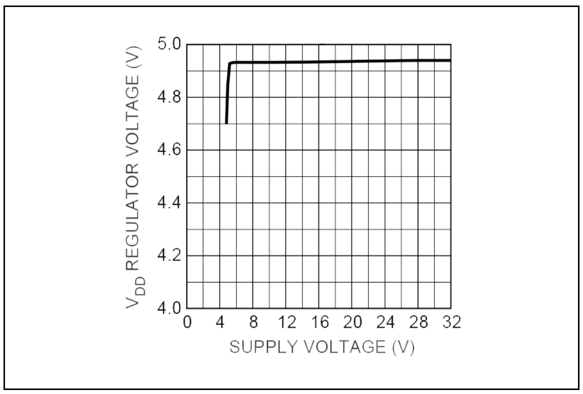


FIGURE 2-8: *V_{DD} Line Regulation.*

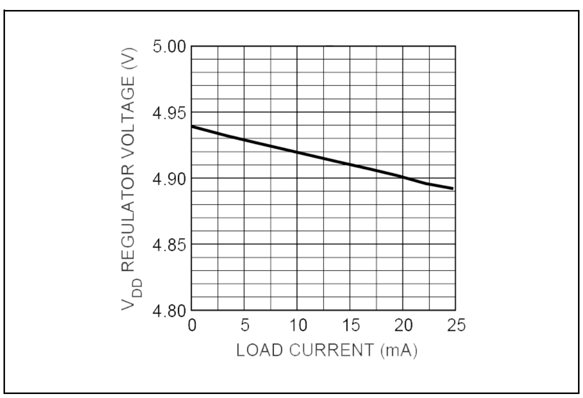


FIGURE 2-9: *V_{DD} Load Regulation.*

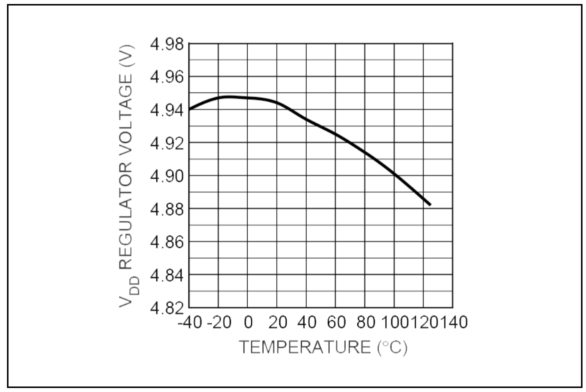


FIGURE 2-10: *V_{DD} vs. Temperature.*

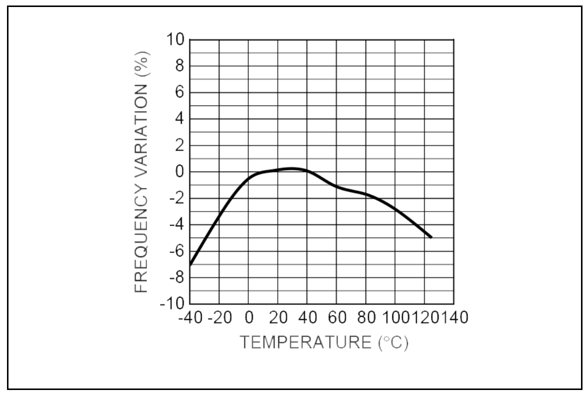


FIGURE 2-11: *Oscillator Frequency Variation vs. Temperature.*

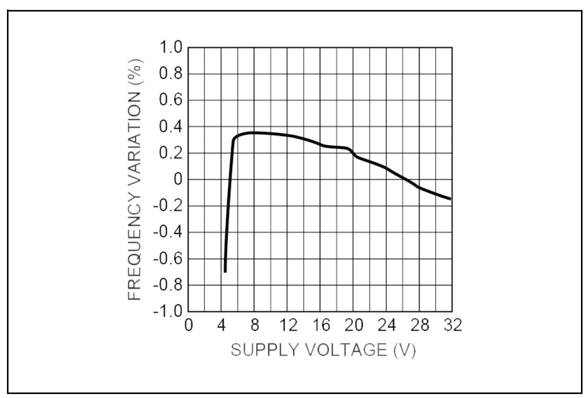


FIGURE 2-12: *Oscillator Frequency Variation vs. Supply Voltage.*

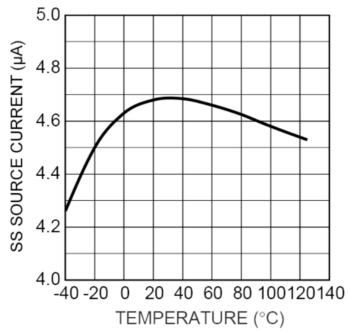


FIGURE 2-13: *Soft-Start Source Current vs. Temperature.*

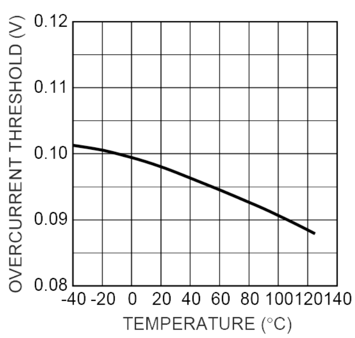


FIGURE 2-14: *Overcurrent Threshold Voltage vs. Temperature.*

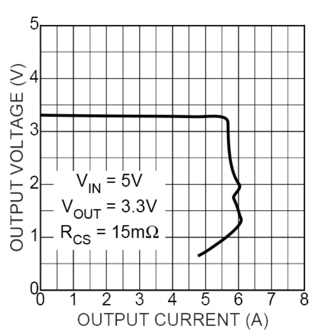


FIGURE 2-15: *Current-Limit Foldback.*

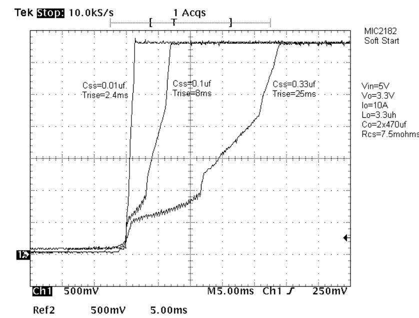


FIGURE 2-16: *Effect of Soft-Start Capacitor (C_{SS}) Value on Output Voltage Waveforms During Turn-On (10A Power Supply Configuration).*

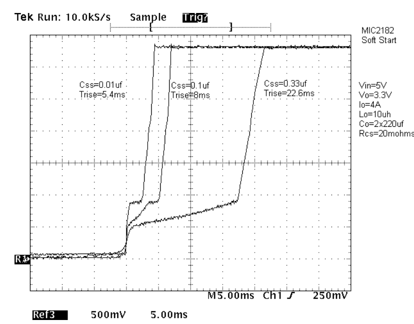


FIGURE 2-17: *Effect of Soft-Start Capacitor (C_{SS}) Value on Output Voltage Waveforms During Turn-On (4A Power Supply Configuration).*

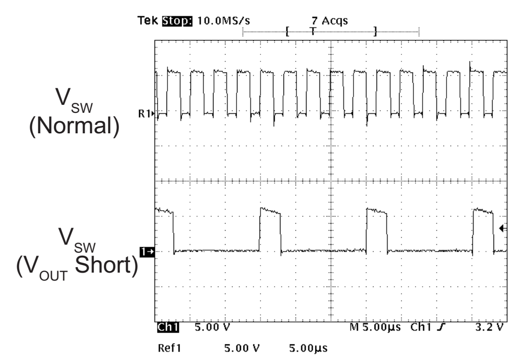


FIGURE 2-18: *Normal (300 kHz Switching Frequency) and Output Short-Circuit (60 kHz) Conditions Switch Node (Pin 15) Waveforms.*

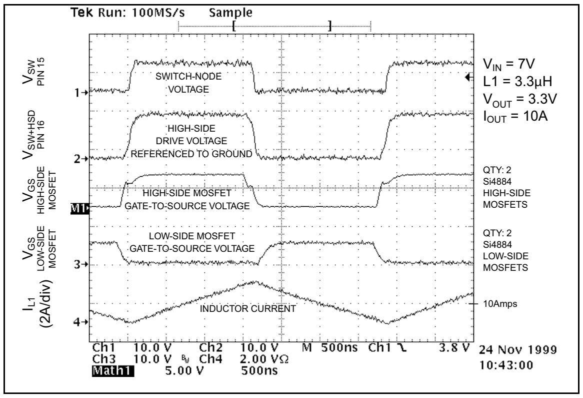


FIGURE 2-19: *Converter Waveforms.*

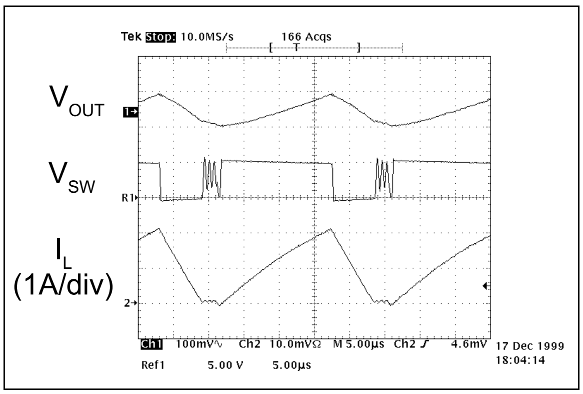


FIGURE 2-20: *Typical Skip-Mode Waveforms.*

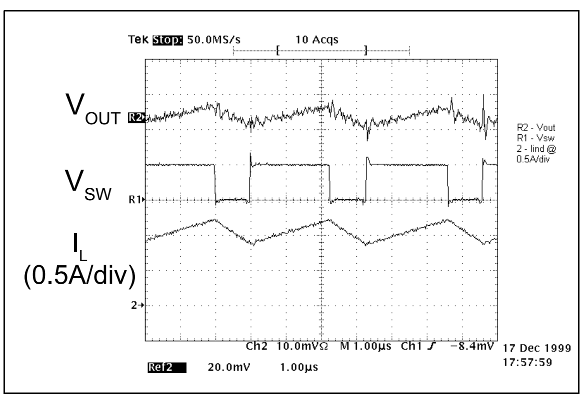


FIGURE 2-21: *Typical PWM Mode Waveforms.*

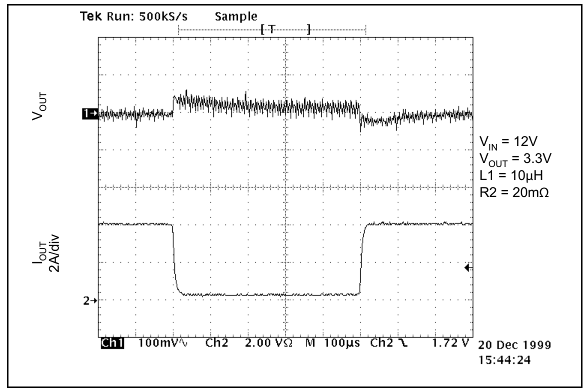


FIGURE 2-22: *Load Transient Response (4A Power Supply Configuration).*

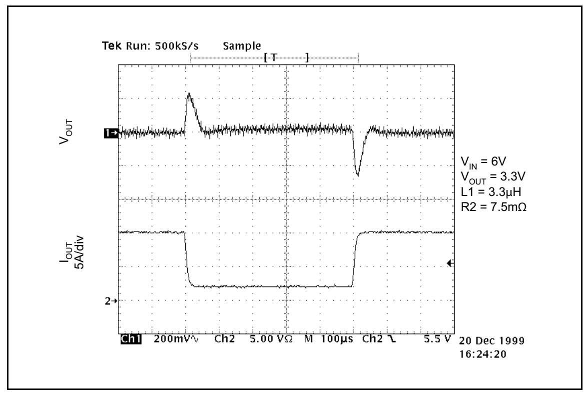


FIGURE 2-23: *Load Transient Response (10A Power Supply Configuration).*

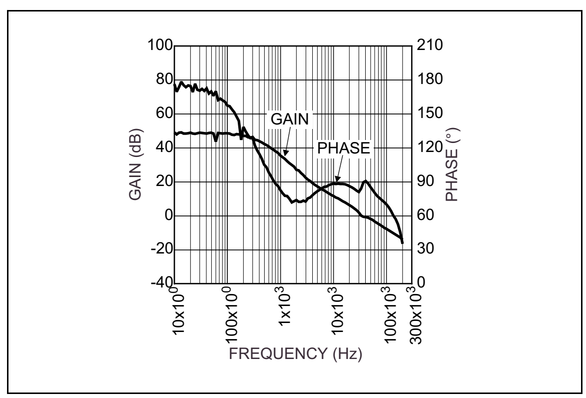


FIGURE 2-24: *Bode Plot (4A Power Supply Configuration).*

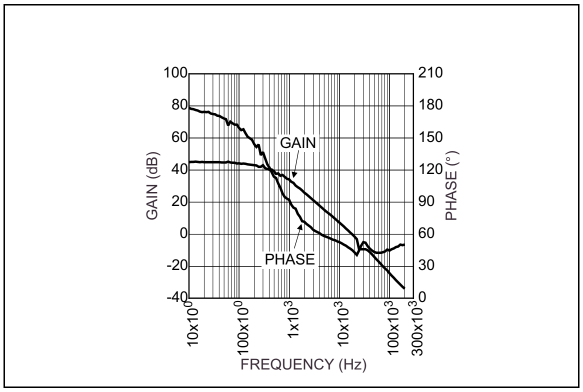


FIGURE 2-25: *Bode Plot (10A Power Supply Configuration).*

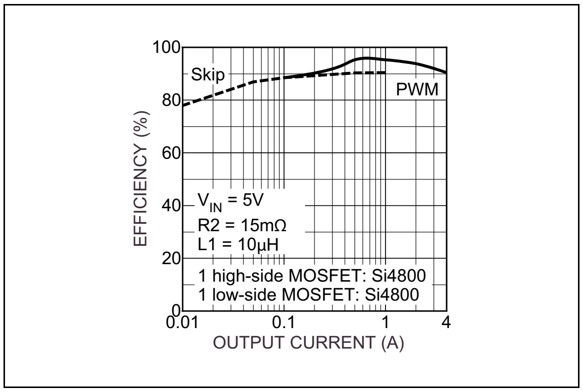


FIGURE 2-26: *Efficiency at V_{IN} = 5V, V_{OUT} = 3.3V (4A Power Supply Configuration).*

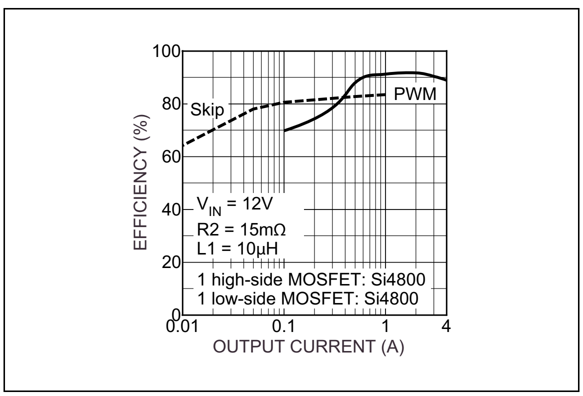


FIGURE 2-27: *Efficiency at V_{IN} = 12V, V_{OUT} = 3.3V (4A Power Supply Configuration).*

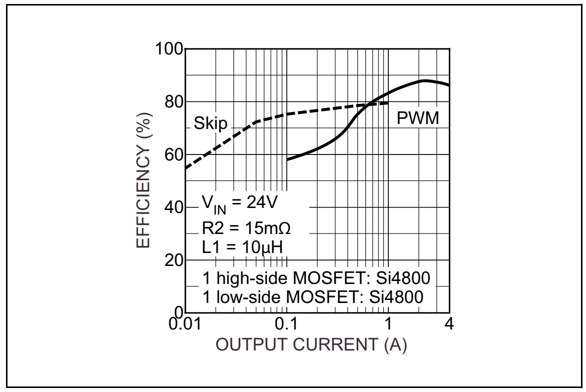


FIGURE 2-28: *Efficiency at V_{IN} = 24V, V_{OUT} = 3.3V (4A Power Supply Configuration).*

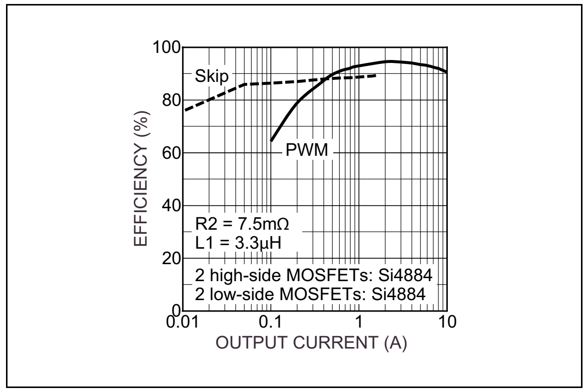


FIGURE 2-29: *Efficiency at V_{IN} = 5V, V_{OUT} = 3.3V (10A Power Supply Configuration).*

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	SS	Soft-Start (External Component): Connect external capacitor to ground to reduce inrush current by delaying and slowing the output voltage rise time. Rise time is controlled by an internal 5 µA current source that charges an external capacitor to V_{DD}.
2	PWM	PWM/Skip-Mode Select (Input): Low sets PWM-mode operation. 1 nF capacitor to ground sets automatic PWM/skip-mode selection.
3	COMP	Compensation (Output): Internal error amplifier output. Connect to capacitor or series RC network to compensate the regulator control loop.
4	SGND	Small Signal Ground (Return): Route separately from other ground traces to the (–) terminal of C_{OUT}.
5	SYNC	Frequency Synchronization (Input): Optional. Connect to external clock signal to synchronize the oscillator. Leading edge of signal above the threshold terminates the switching cycle. Connect to SGND if unused.
6	EN/UVLO	Enable/Undervoltage Lockout (Input): Low-level signal powers down the controller. Input below the 2.5V UVLO threshold voltage disables switching and functions as an accurate undervoltage lockout (UVLO). Input below the 1.1V enable threshold voltage forces complete micropower (< 0.1 µA) shutdown.
7 (Fixed)	VREF	Reference Voltage (Output): 1.245V output. Requires 0.1 µF capacitor to ground.
7 (Adj.)	FB	Feedback (Input): Regulates FB pin to 1.245V. See the Applications Information section for resistor divider calculations.
8	CSH	Current-Sense High (Input): Current-limit comparator non-inverting input. A built-in offset of 100 mV between CSH and VOUT pins in conjunction with the current-sense resistor set the current-limit threshold level. This is also the positive input to the current sense amplifier.
9	VOUT	Current-Sense Low (Input): Output voltage feedback input and inverting input for the current limit comparator and the current sense amplifier.
10	VIN	[Battery] Unregulated Input (Input): +4.5V to +32V supply input.
11	VDD	5V Internal Linear-Regulator (Output): V_{DD} is the external MOSFET gate drive supply voltage and an internal supply bus for the IC. Bypass to SGND with a 4.7 µF capacitor. V_{DD} can supply up to 5 mA for external loads.
12	PGND	MOSFET Driver Power Ground (Return): Connects to source of synchronous MOSFET and the (–) terminal of C_{IN}.
13	LSD	Low-Side Drive (Output): High-current driver output for external synchronous MOSFET. Voltage swing is between ground and VDD.
14	BST	Boost (Input): Provides drive voltage for the high-side MOSFET driver. The drive voltage is higher than the input voltage by VDD minus a diode drop.
15	VSW	Switch (Return): High-side MOSFET driver return.
16	HSD	High-Side Drive (Output): High-current driver output for high-side MOSFET. This node voltage swing is between ground and V_{IN} + 5V - $V_{diode\ drop}$.

4.0 FUNCTIONAL DESCRIPTION

The MIC2182 is a BiCMOS, switched-mode, synchronous step-down (buck) converter controller. Current-mode control is used to achieve superior transient line and load regulation. An internal corrective ramp provides slope compensation for stable operation above 50% duty cycle. The controller is optimized for high-efficiency, high-performance DC-DC converter applications.

The MIC2182 block diagrams are shown in the Block Diagrams section.

The MIC2182 controller is divided into six functions.

- Control Loop
  - PWM Operation
  - Skip-Mode Operation
- Current Limit
- Reference, Enable, and UVLO
- MOSFET Gate Drive
- Oscillator and Sync
- Soft Start

4.1 Control Loop

4.1.1 PWM AND SKIP MODES OF OPERATION

The MIC2182 operates in PWM (pulse-width modulation) mode at heavier output load conditions. At lighter load conditions, the controller can be configured to automatically switch to a pulse-skipping mode to improve efficiency. The potential disadvantage of skip mode is the variable switching frequency that accompanies this mode of operation. The occurrence of switching pulses depends on component values as well as line and load conditions. There is an external sync function that is disabled in skip mode. In PWM mode, the synchronous buck converter forces continuous current to flow in the inductor. In skip mode, current through the inductor can settle to zero, causing voltage ringing across the inductor. Pulling the PWM pin (Pin 2) low will force the controller to operate in PWM mode for all load conditions, which will improve cross regulation of transformer-coupled, multiple output configurations.

4.1.2 PWM CONTROL LOOP

The MIC2182 uses current-mode control to regulate the output voltage. This method senses the output voltage (outer loop) and the inductor current (inner loop). It uses inductor current and output voltage to determine the duty cycle of the buck converter. Sampling the inductor current removes the inductor from the control loop, which simplifies compensation.

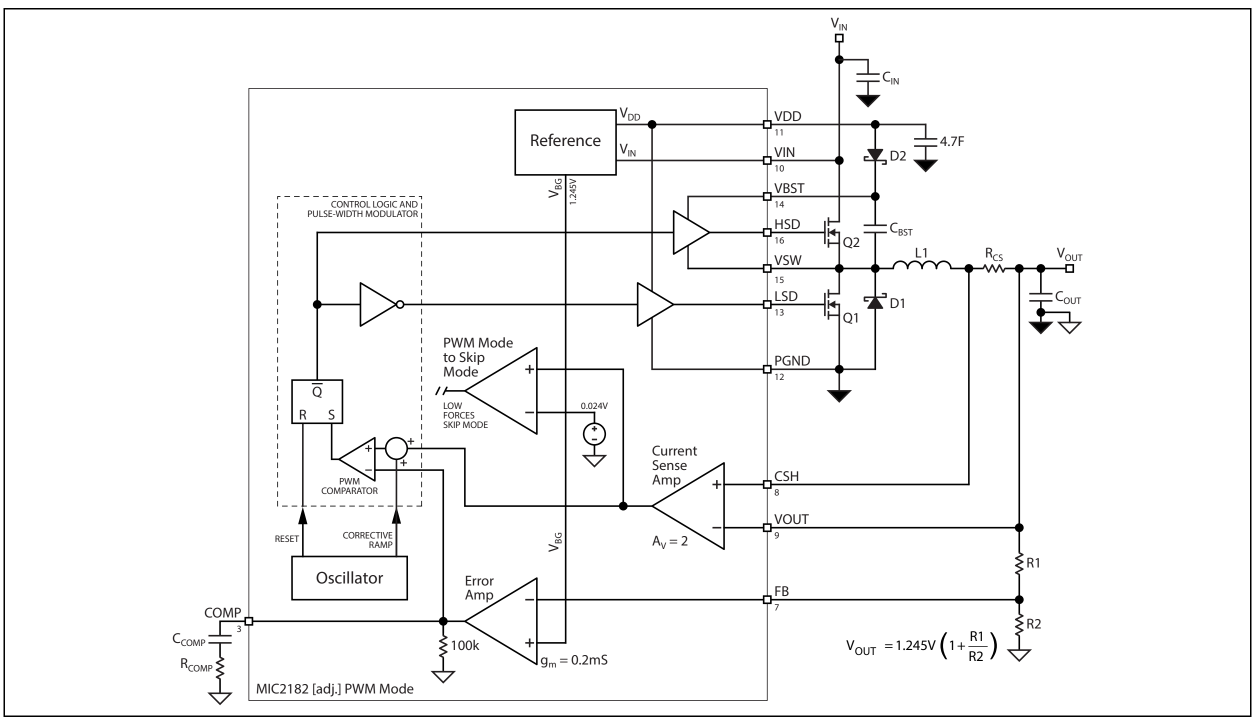


FIGURE 4-1: PWM Operation.

A block diagram of the MIC2182 PWM current-mode control loop is shown in Figure 4-1 and the PWM mode voltage and current waveforms are shown in Figure 4-3. The inductor current is sensed by measuring the voltage across the resistor, R_{CS}. A ramp is added to the amplified current-sense signal to provide slope compensation, which is required to prevent unstable operation at duty cycles greater than 50%.

A transconductance amplifier is used for the error amplifier, which compares an attenuated sample of the output voltage with a reference voltage. The output of the error amplifier is the COMP (compensation) pin, which is compared to the current-sense waveform in the PWM block. When the current signal becomes greater than the error signal, the comparator turns off the high-side drive. The COMP pin (Pin 3) provides access to the output of the error amplifier and allows the use of external components to stabilize the voltage loop.

4.1.3 SKIP-MODE CONTROL LOOP

This control method is used to improve efficiency at light output loads. At light output currents, the power drawn by the MIC2182 is equal to the input voltage times the IC supply current (I_Q). At light output currents, the power dissipated by the IC can be a significant portion of the total output power, which lowers the efficiency of the buck converter. The MIC2182 draws less supply current in skip mode by disabling portions of the control and drive circuitry when the IC is not switching. The disadvantage of this method is greater output voltage ripple and variable switching frequency.

A block diagram of the MIC2182 skip mode is shown in Figure 4-2. Skip mode voltage and current waveforms are shown in Figure 4-4.

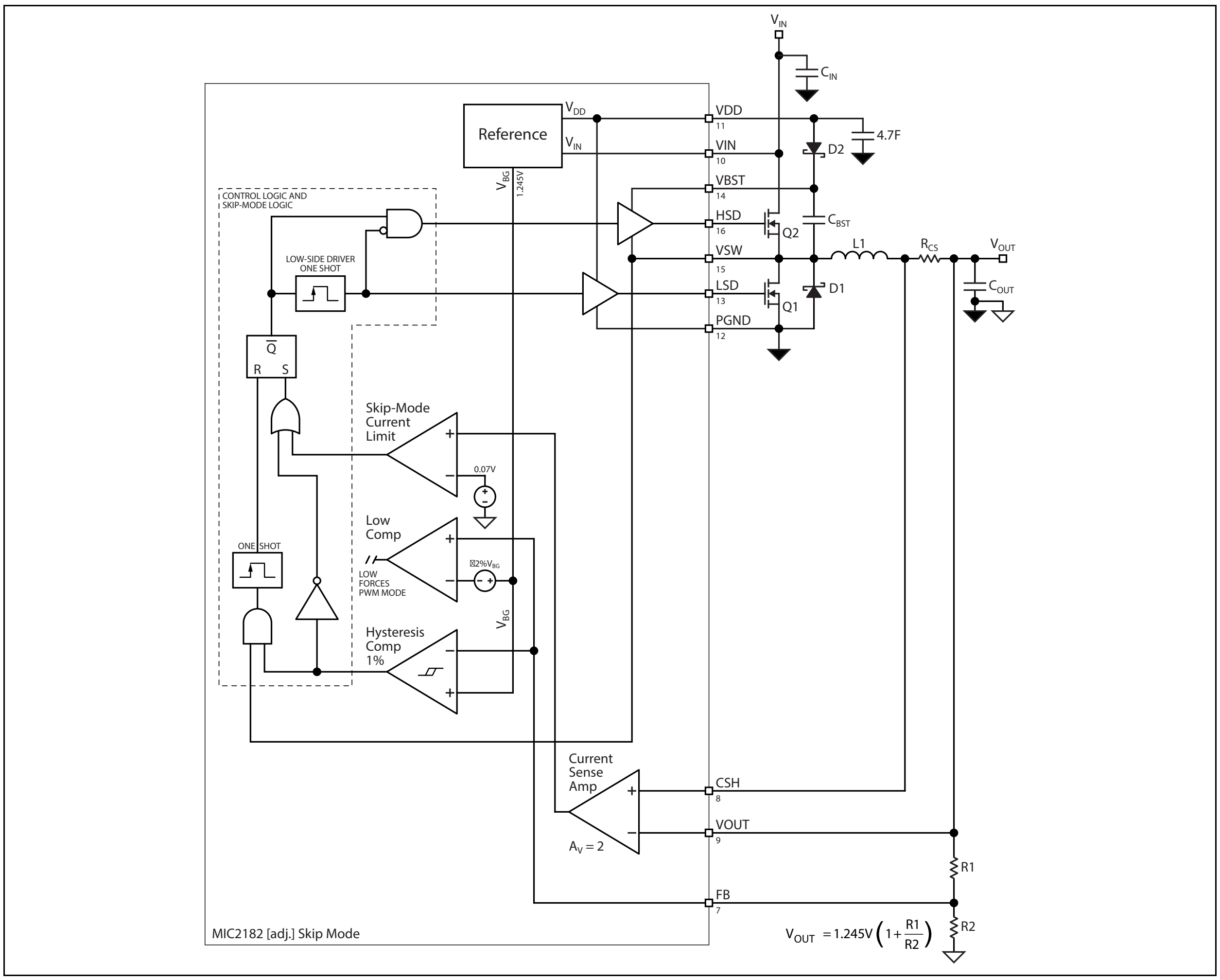


FIGURE 4-2: *Skip-Mode Operation.*

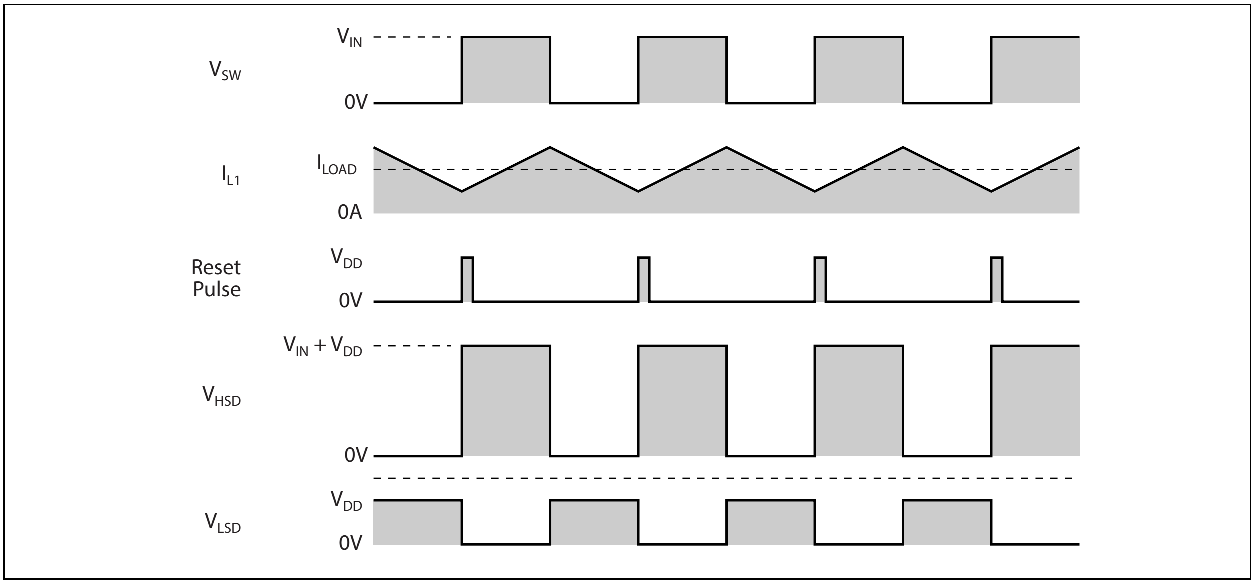


FIGURE 4-3: *PWM-Mode Timing.*

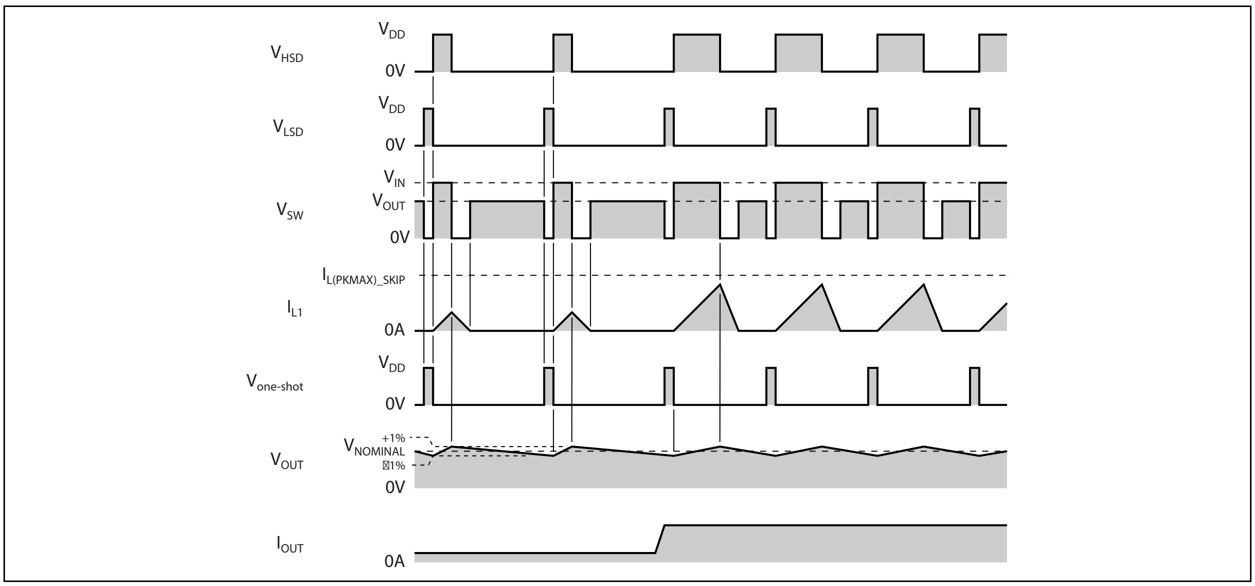


FIGURE 4-4: *Skip-Mode Timing.*

A hysteretic comparator is used in place of the PWM error amplifier and a current-limit comparator senses the inductor current. A one-shot starts the switching cycle by momentarily turning on the low side MOSFET to insure the high-side drive boost capacitor, C_{BST}, is fully charged. The high-side MOSFET is turned on and current ramps up in the inductor, L1. The high-side drive is turned off when either the peak voltage on the input of the current-sense comparator exceeds the threshold, typically 35 mV, or the output voltage rises above the hysteretic threshold of the output voltage comparator. Once the high-side MOSFET is turned off, the load current discharges the output capacitor, causing V_{OUT} to fall. The cycle repeats when V_{OUT} falls below the lower threshold, –1%.

The maximum peak inductor current in Skip Mode depends on the skip-mode current-limit threshold and the value of the current-sense resistor, R_{CS}.

EQUATION 4-1:

$$I_{L(PKMAX)\_SKIP} = \frac{35mV}{R_{CS}}$$

Figure 4-5 shows the improvement in efficiency that skip mode makes at lower output currents.

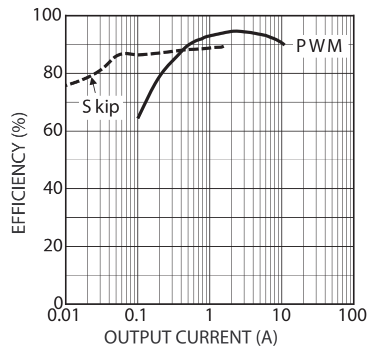


FIGURE 4-5: *Efficiency.*

4.1.4 SWITCHING FROM PWM TO SKIP MODE

The current sense amplifier in Figure 4-1 monitors the average voltage across the current-sense resistor. The controller will switch from PWM to skip mode when the average voltage across the current-sense resistor drops below approximately 12 mV if the PWM/Skip mode selection is set to automatic. This is shown in Figure 4-6. The average output current at this transition level for is calculated below.

EQUATION 4-2:

$$I_{OUT(MINPWM)} = \frac{0.012V}{R_{CS}}$$

Where:

0.012V = Threshold Voltage of the Internal Comparator

R_{CS} = Current-Sense Resistor Value

4.1.5 SWITCHING FROM SKIP TO PWM MODE

The frequency of occurrence of the skip-mode current pulses increase as the output current increases until the hysteretic duty cycle reaches full CCM duty cycle (continuous pulses). Increasing the current past this point will cause the output voltage to drop. The low limit comparator senses the output voltage when it drops below 2% of the set output and automatically switches the converter to PWM mode.

The inductor current in skip mode is a triangular wave shape a minimum value of 0 and a maximum value of 35 mV/R_{CS} (see Figure 4-7). The maximum average output current in skip mode is the average value of the inductor waveform:

EQUATION 4-3:

$$I_{OUT(MAXSKIP)} = 0.5 \times \frac{35mV}{R_{CS}}$$

The PWM pin (Pin 2) is the PWM/Skip mode selection pin. When the PWM pin is logic level low, the device is set in forced PWM operation. A capacitor (typically 1 nF) connected across the PWM pin and ground sets the device to automatic PWM/Skip selection according to the output current level.

The capacitor on the PWM pin (Pin 2) is discharged when the IC transitions from skip to PWM mode. This forces the IC to remain in PWM mode for a fixed period of time. The added delay prevents unwanted switching between PWM and skip mode. The capacitor is charged with a 10 µA current source on Pin 2. The threshold on Pin 2 is 2.5V. The delay for a typical 1 nF capacitor is:

EQUATION 4-4:

$$t_{DELAY} = \frac{C_{PWM} \times V_{\mathrm{TH\_MODESEL}}}{I_{\mathrm{PWM\_SRC}}} = \frac{1nF \times 2.5V}{10\mu A} = 250\mu s$$

Where:

C_{PWM} = Capacitor connected to Pin 2.

$V_{TH\_MODESEL}$ = Mode selection threshold voltage (2.5V typ.)

I_{PWM_SRC} = PWM pin source current (10 µA typ.)

4.2 Current Limit

The current-limit circuit operates during PWM mode. The output current is detected by the voltage drop across the external current-sense resistor (R_{CS} in the Block Diagrams). The current-limit threshold voltage is 100 mV +35 mV/–25 mV. The current-sense resistor must be sized using the minimum current-limit threshold voltage. The external components must be designed to withstand the maximum current limit. The current-sense resistor value is calculated by the equation below:

EQUATION 4-5:

$$R_{CS} \le \frac{75mV}{I_{OUT(MAX)}}$$

Where:

$I_{OUT(MAX)}$ = Target maximum output current.

The maximum current limit is:

EQUATION 4-6:

$$I_{LIM(MAX)} = \frac{135mV}{R_{CS}}$$

The current-sense pins CSH (Pin 8) and VOUT (Pin 9) are noise sensitive due to the low signal level and high input impedance. The PCB traces should be short and routed close to each other. A small (1 nF to 0.1 µF) capacitor across the pins will attenuate high frequency switching noise.

When the peak inductor current exceeds the current-limit threshold, the current-limit comparator, in the Block Diagrams, turns off the high-side MOSFET for the remainder of the cycle. The output voltage drops as additional load current is pulled from the converter. When the output voltage reaches approximately 0.95V, the circuit enters frequency-foldback mode and the oscillator frequency will drop to 60 kHz while maintaining the peak inductor current equal to the nominal 100 mV across the external current-sense resistor. This limits the maximum output power delivered to the load under a short circuit condition.

4.3 Reference, Enable, and UVLO Circuits

The output drivers are enabled when the following conditions are satisfied:

- The V_{DD} voltage (Pin 11) is greater than its undervoltage threshold (typically 4.2V)
- The voltage on the enable pin is greater than the enable UVLO threshold (typically 2.5V)

The internal bias circuit generates a 1.245V bandgap reference voltage for the voltage error amplifier and a 5V V_{DD} voltage for the gate drive circuit. The reference voltage in the fixed-output-voltage versions of the MIC2182 is buffered and brought to Pin 7. The V_{REF} pin should be bypassed to GND (Pin 4) with a 0.1 µF capacitor. The adjustable version of the MIC2182 uses Pin 7 for output voltage sensing. A decoupling capacitor on Pin 7 is not used in the adjustable output voltage version.

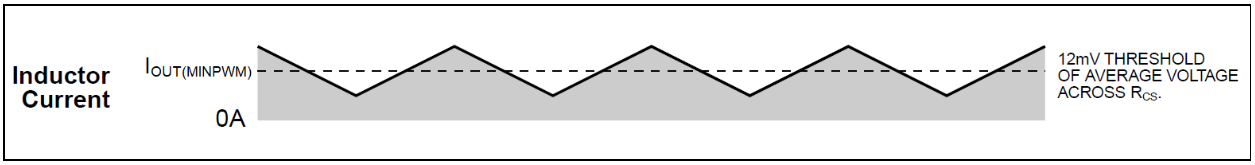


FIGURE 4-6: *Minimum PWM-Mode Load Inductor Current for PWM Operation.*

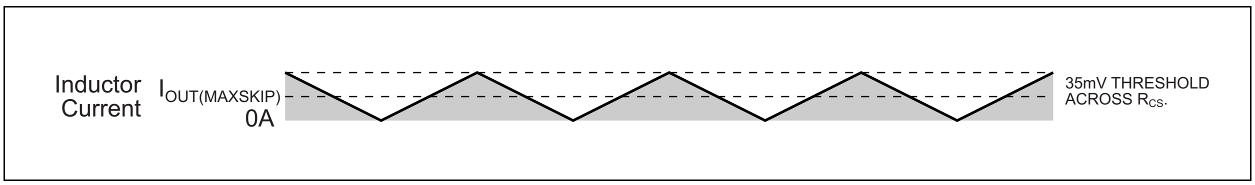


FIGURE 4-7: *Maximum Skip-Mode-Load Inductor Current.*

The enable pin (Pin 6) has two threshold levels, allowing the MIC2182 to shut down in a low current mode, or turn off output switching in UVLO mode. An enable pin voltage lower than the shutdown threshold turns off all the internal circuitry and reduces the input current to typically 0.1 µA.

If the enable pin voltage is between the shutdown and UVLO thresholds, the internal bias, V_{DD}, and reference voltages are turned on. The soft-start pin is forced low by an internal discharge MOSFET. The output drivers are inhibited from switching and remain in a low state. Raising the enable voltage above the UVLO threshold of 2.5V allows the soft-start capacitor to charge and enables the output drivers.

Either of two UVLO conditions will pull the soft-start capacitor low.

- When the V_{DD} drops below 4.1V
- When the enable pin drops below the 2.5V threshold

4.4 MOSFET Gate Drive

The MIC2182 high-side drive circuit is designed to switch an N-channel MOSFET. Referring to the Block Diagrams, a bootstrap circuit, consisting of D2 and C_{BST}, supplies energy to the high-side drive circuit. Capacitor C_{BST} is charged while the low-side MOSFET is on and the voltage on the V_{SW} pin (Pin 15) is approximately 0V. When the high-side MOSFET driver is turned on, energy from C_{BST} is used to turn the high-side MOSFET on. As the MOSFET turns on, the voltage on the V_{SW} pin increases to approximately V_{IN}. Diode D2 is reversed biased and voltage at the BST pin floats high while continuing to keep the high-side MOSFET on. When the low-side switch is turned back on, C_{BST} is recharged through D2.

The drive voltage is derived from the internal 5V V_{DD} bias supply. The nominal low-side gate drive voltage is 5V and the nominal high-side gate drive voltage is approximately 4.5V due the voltage drop across D2. A fixed 80 ns delay between the high-side and low-side driver transitions is used to prevent current from simultaneously flowing unimpeded through both MOSFETs.

4.5 Oscillator and Sync

The internal oscillator is free running and requires no external components. The nominal oscillator frequency is 300 kHz. If the output voltage is below approximately 0.95V, the oscillator operates in a frequency-foldback mode and the switching frequency is reduced to 60 kHz.

The SYNC input (Pin 5) allows the MIC2182 to synchronize with an external clock signal. The rising edge of the sync signal generates a reset signal in the oscillator, which turns off the low-side gate drive output. The high-side drive then turns on, restarting the switching cycle. The sync signal is inhibited when the controller operates in skip mode or during frequency foldback. The sync signal frequency must be greater than the maximum specified free running frequency of the MIC2182. If the synchronizing frequency is lower, double pulsing of the gate drive outputs will occur. When not used, the sync pin must be connected to ground.

Figure 4-8 shows the timing between the external sync signal (trace 2), the low-side drive (trace 1) and the high-side drive (trace R1). There is a delay of approximately 250 ns between the rising edge of the external sync signal and turnoff of the low-side MOSFET gate drive.

Some concerns of operating at higher frequencies are:

- Higher power dissipation in the internal V_{DD} regulator. This occurs because the MOSFET gates require charge to turn on the device. The average current required by the MOSFET gate increases with switching frequency. This increases the power dissipated by the internal V_{DD} regulator. Figure 4-9 and Figure 4-10 shows the total gate charge which can be driven by the MIC2182 over the input voltage range, for different values of switching frequency. The total gate charge includes both the high-side and low-side MOSFETs. The larger SOIC package is capable of dissipating more power than the SSOP package and can drive larger MOSFETs with higher gate drive requirements.

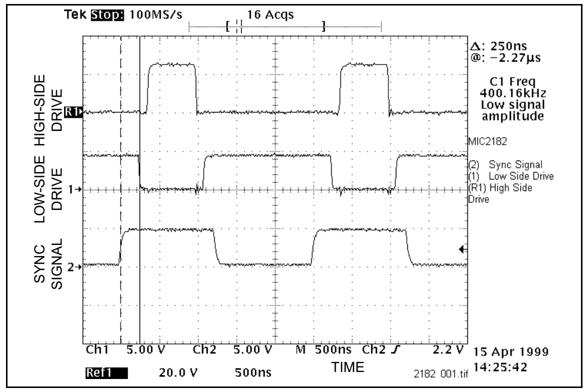


FIGURE 4-8: Sync Waveforms.

- Reduced maximum duty cycle due to switching transition times and constant delay times in the controller. As the switching frequency increased, the switching period decreases. The switching transition times and constant delays in the MIC2182 start to become noticeable. The effect is to reduce the maximum duty cycle of the controller. This will cause the minimum input to output differential voltage (dropout voltage) to increase.

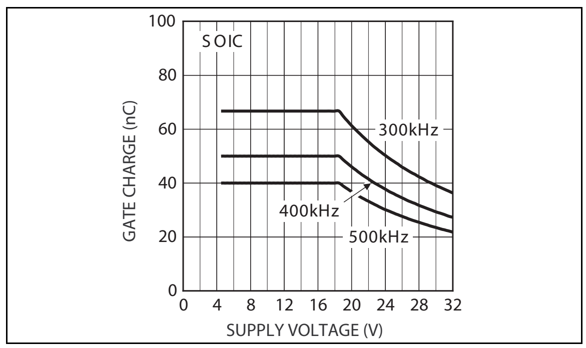


FIGURE 4-9: *SOIC Package Device MOSFET Gate Charge Driving Ability vs. Input Voltage.*

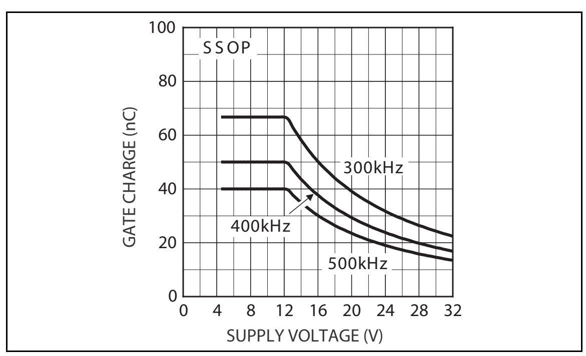


FIGURE 4-10: *SSOP Package Device MOSFET Gate Charge Driving Ability vs. Input Voltage.*

It is recommended that the user limits the maximum synchronized frequency to 600 kHz. If a higher synchronized frequency is required, it may be possible and will be design dependent.

4.6 Soft-Start

Soft start reduces the power supply input surge current at startup by controlling the output voltage rise time. The input surge appears while the output capacitance is charged up. A slower output rise time will draw a lower input surge current. Soft start may also be used for power supply sequencing.

The soft-start voltage is applied directly to the PWM comparator. A 5 µA internal current source is used to charge up the soft-start capacitor. The capacitor is discharged when either the enable voltage drops below the UVLO threshold (2.5V) or the V_{DD} voltage drops below the UVLO level (4.1V).

The part switches at a minimum duty cycle when the soft-start pin voltage is less than 0.4V. This maintains a charge on the bootstrap capacitor and insures high-side gate drive voltage. As the soft-start voltage rises above 0.4V, the duty cycle increases from the minimum duty cycle to the operating duty cycle. The oscillator runs at the foldback frequency of 60 kHz until the output voltage rises above 0.95V. Above 0.95V, the switching frequency increases to 300 kHz (or the synced frequency), causing the output voltage to rise a greater rate. The rise time of the output is dependent on the soft-start capacitor, output capacitance, output voltage, and load current. The oscilloscope photo in Figure 4-11 show the output voltage and the soft-start pin voltage at startup.

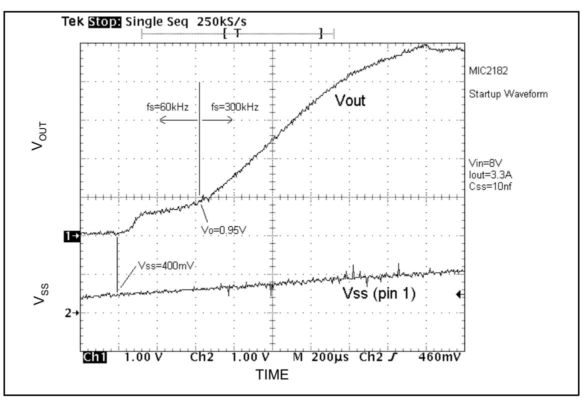


FIGURE 4-11: Startup Waveforms.

4.7 Minimum Pulse Width

The MIC2182 has a specified minimum pulse width. This minimum pulse width places a lower limit on the minimum duty cycle of the buck converter. When the MIC2182 is operating in forced PWM mode (Pin 2 low) and when the output current is very low or zero, there is a limit on the ratio of V_{OUT}/V_{IN}. If this limit is exceeded, the output voltage will rise above the regulated voltage level. A minimum load is required to prevent the output from rising up. This will not occur for output voltages greater than 3V.

Figure 4-12 should be used as a guide when the MIC2182 is forced into PWM-only mode. The actual maximum input voltage will depend on the exact external components used (MOSFETs, inductors, etc.).

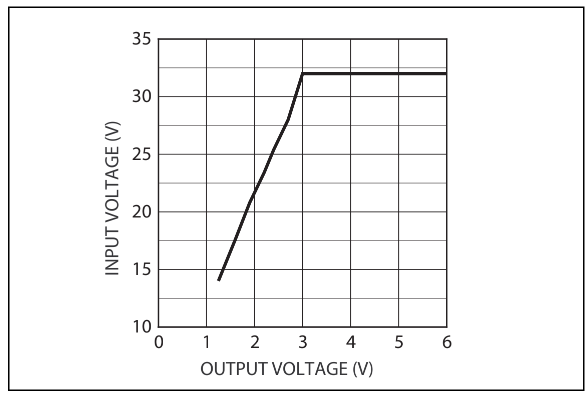


FIGURE 4-12: Max. Input Voltage in Forced-PWM Mode.

This restriction does not occur when the MIC2182 is set to automatic mode (Pin 2 connected to a capacitor) since the converter operates in skip mode at low output current.

5.0 APPLICATIONS INFORMATION

5.1 Inductor Selection

Values for inductance, peak, and RMS currents are required to select the output inductor. The input and output voltages and the inductance value determine the peak to peak inductor ripple current. Generally, higher inductance values are used with higher input voltages. Larger peak to peak ripple currents will increase the power dissipation in the inductor and MOSFETs. Larger output ripple currents will also require more output capacitance to smooth out the larger ripple current. Smaller peak to peak ripple currents require a larger inductance value and therefore a larger and more expensive inductor. A good compromise between size, loss and cost is to set the inductor ripple current to be equal to 20% of the maximum output current.

The inductance value is calculated by the equation below:

EQUATION 5-1:

$$L = \frac{V_{OUT} \times (V_{IN(MAX)} - V_{OUT})}{V_{IN(MAX)} \times f_{SW} \times 0.2 \times I_{OUT(MAX)}}$$

Where:

f_{SW} = Switching frequency

0.2 = Ratio of AC ripple current to maximum DC output current.

$V_{IN(MAX)}$ = Maximum input voltage

$I_{OUT(MAX)}$ = Maximum DC output current

The peak-to-peak inductor current (AC ripple current) is:

EQUATION 5-2:

$$\Delta I_{L(PP)} = \frac{V_{OUT} \times (V_{IN(MAX)} - V_{OUT})}{V_{IN(MAX)} \times f_{SW} \times L}$$

The peak inductor current is equal to the average output current plus one half of the peak to peak inductor ripple current.

EQUATION 5-3:

$$I_{L(PK)} = I_{OUT(MAX)} + 0.5 \times \Delta I_{L(PP)}$$

The RMS inductor current is used to calculate the I^2 x R losses in the inductor.

EQUATION 5-4:

$$I_{L(RMS)} = I_{OUT(MAX)} \times \sqrt{1 + \frac{1}{12}\left(\frac{\Delta I_{L(PP)}}{I_{OUT(MAX)}}\right)^2}$$

Maximizing efficiency requires the proper selection of core material and minimizing the winding resistance. The high frequency operation of the MIC2182 requires the use of ferrite materials for all but the most cost sensitive applications. Lower cost iron powder cores may be used but the increase in core loss will reduce the efficiency of the buck converter. This is especially noticeable at low output power. The winding resistance decreases efficiency at the higher output current levels. The winding resistance must be minimized although this usually comes at the expense of a larger inductor.

The power dissipated in the inductor is equal to the sum of the core and copper losses. At higher output loads, the core losses are usually insignificant and can be ignored. At lower output currents, the core losses can be a significant contributor. Core loss information is usually available from the magnetics vendor.

Copper loss in the inductor is calculated by the equation below:

EQUATION 5-5:

$$P_{LOSS(Cu)} = I_{L(RMS)}^{\ 2} \times R_{WINDING}$$

The resistance of the copper wire, $R_{WINDING}$, increases with temperature. The value of the winding resistance used should be at the operating temperature.

EQUATION 5-6:

$$R_{WINDING(HOT)} = R_{WINDING(20°C)} \times (1 + 0.0042 \times (T_{HOT} - T_{20°C}))$$

Where:

T_{HOT} =	Temperature of the wire under operating load
$T_{20°C}$ =	Ambient room temperature
$R_{WINDING(20°C)}$ =	Room temperature winding resistance (usually specified by the manufacturer)

5.2 Current-Sense Resistor Selection

Low inductance power resistors, such as metal film resistors should be used. Most resistor manufacturers make low inductance resistors with low temperature coefficients, designed specifically for current-sense applications. Both resistance and power dissipation must be calculated before the resistor is selected. The value of R_{CS} is chosen based on the maximum output current and the minimum current-limit threshold voltage level. The power dissipated is based on the maximum peak current limit at the maximum current-limit threshold voltage.

EQUATION 5-7:

$$R_{CS} \le \frac{75mV}{I_{OUT(MAX)}}$$

The maximum overcurrent at the maximum current-limit threshold voltage is:

EQUATION 5-8:

$$I_{OVERCURRENT(MAX)} = \frac{135mV}{R_{CS}}$$

The maximum power dissipated in the sense resistor is:

EQUATION 5-9:

$$P_{D(RCS)} = I_{OVERCURRENT(MAX)}^2 \times R_{CS}$$

5.3 MOSFET Selection

External N-channel logic-level power MOSFETs must be used for the high-side and low-side switches. The MOSFET gate-to-source drive voltage of the MIC2182 is regulated by an internal 5V V_{DD} regulator. Logic-level MOSFETs, whose operation is specified at V_{GS} = 4.5V must be used.

It is important to note the on-resistance of a MOSFET increases with increasing temperature. A 75°C rise in junction temperature will increase the channel resistance of the MOSFET by 50% to 75% of the resistance specified at 25°C. This change in resistance must be accounted for when calculating MOSFET power dissipation.

Total gate charge is the charge required to turn the MOSFET on and off under specified operating conditions (V_{DS} and V_{GS}). The gate charge is supplied by the MIC2182 gate drive circuit. At 300 kHz switching frequency and above, the gate charge can be a significant source of power dissipation in the MIC2182. At low output load, this power dissipation is noticeable as a reduction in efficiency. The average current required to drive the high-side MOSFET is:

EQUATION 5-10:

$$I_{GHS(AVG)} = Q_G \times f_{SW}$$

Where:

$I_{GHS(AVG)}$ =	Average High-Side MOSFET Gate Current
Q_G =	Total Gate Charge for the High-Side MOSFET Taken from Manufacturer's Data Sheet with V_{GS} = 5V
f_{SW} =	Switching Frequency

The low-side MOSFET is turned on and off at V_{DS} = 0 because the freewheeling diode is conducting during this time. The switching losses for the low-side MOSFET is usually negligible. Also, the gate drive current for the low-side MOSFET is more accurately calculated using C_{ISS} at V_{DS} = 0V instead of gate charge.

The gate drive current for the low-side MOSFET:

EQUATION 5-11:

$$I_{GLS(AVG)} = C_{ISS} \times V_{GS} \times f_{SW}$$

Where:

C_{ISS} = Input capacitance of the low-side MOSFET at V_{DS} = 0V.

Because the current from the gate drive comes from the input voltage, the power dissipated in the MIC2182 due to gate drive is:

EQUATION 5-12:

$$P_{D(GDRV)} = V_{IN} \times (I_{GHS(AVG)} + I_{GLS(AVG)})$$

Where:

$P_{D(GDRV)}$ = Power Dissipated Due to Gate Drive

A convenient figure of merit for switching MOSFETs is the on-resistance times the total gate charge ($R_{DS(ON)}$ x Q_G). Lower numbers translate into higher efficiency. Low gate-charge logic-level MOSFETs are a good choice for use with the MIC2182. Power dissipation in the MIC2182 package limits the maximum gate drive current. Refer to Figure 4-9 and Figure 4-10 for the MIC2182 gate drive limits.

Parameters that are important to MOSFET switch selection are:

- Voltage rating
- On-resistance
- Total gate charge

The voltage rating of the MOSFETs are essentially equal to the input voltage. A safety factor of 20% should be added to the $V_{DS(max)}$ of the MOSFETs to account for voltage spikes due to circuit parasitics.

The power dissipated in the switching transistor is the sum of the conduction losses during the on-time ($P_{CONDUCTION}$) and the switching losses that occur during the period of time when the MOSFETs turn on and off (P_{AC}).

EQUATION 5-13:

$$P_{D(SW)} = P_{CONDUCTION} + P_{AC}$$

Where:

$P_{CONDUCTION}$	= $I_{SW(RMS)}^2$ x $R_{DS(ON)}$
P_{AC} =	$P_{AC(OFF)}$ + $P_{AC(ON)}$
$R_{DS(ON)}$ =	On-Resistance of the MOSFET Switch
$I_{SW(RMS)}$ =	RMS current of the MOSFET switch

Making the assumption the turn-on and turn-off transition times are equal, the transition time can be approximated by:

EQUATION 5-14:

$$t_T = \frac{C_{ISS} \times V_{GS} + C_{OSS} \times V_{IN}}{I_G}$$

Where:

C_{ISS} and C_{OSS} are Measured at V_{DS} = 0V

I_G = Gate Drive Current (1A for the MIC2182)

The total high-side MOSFET switching loss is:

EQUATION 5-15:

$$P_{AC(SWHS)} = (V_{IN} + V_D) \times I_{L(AVG)} \times t_T \times f_{SW}$$

Where:

$I_{L(AVG)}$ =	Average inductor current
t_T =	Switching transition time typically 20 ns to 50 ns)
V_D =	Freewheeling diode drop, typically 0.5V
f_{SW} =	Switching frequency, normally 300 kHz

Because the low-side MOSFET body diode is forward biased before the low-side MOSFET is turned on and after the low-side MOSFET is turned off, this keeps the voltage across the low-side MOSFET to about 0.5V during switching transitions, the low-side MOSFET switching losses are negligible and can be ignored.

5.3.1 RMS CURRENT AND MOSFET POWER DISSIPATION CALCULATION

Under normal operation, the high-side MOSFET's RMS current is greatest when V_{IN} is low (maximum duty cycle). The low-side MOSFET's RMS current is greatest when V_{IN} is high (minimum duty cycle). However, the maximum stress to the MOSFETs occurs during short circuit conditions, where the output current is equal to $I_{OVERCURRENT(MAX)}$. (See the Current-Sense Resistor Selection section). The calculations below are for normal operation. To calculate the stress under short circuit conditions, substitute $I_{OVERCURRENT(MAX)}$ for $I_{OUT(MAX)}$. Use the formula below to calculate duty cycle D under short circuit conditions.

EQUATION 5-16:

$$D_{SHORTCIRCUIT} = 0.063 - 1.8 \times 10^{-3} \times V_{IN}$$

The RMS value of the high-side switch current is:

EQUATION 5-17:

$$I_{SWHS(RMS)} = \sqrt{D \times \left(I_{OUT(MAX)}^{2} + \frac{\Delta I_{L(PP)}^{2}}{12}\right)}$$

The RMS value of the low-side switch current is:

EQUATION 5-18:

$$I_{SWLS(RMS)} =$$

$$\sqrt{(1 - D) \times \left(I_{OUT(MAX)}^{2} + \frac{\Delta I_{L(PP)}^{2}}{12}\right)}$$

Where:

D = Duty Cycle of the Converter

EQUATION 5-19:

$$D = \frac{V_{OUT}}{\eta \times V_{IN}}$$

Where:

η = Efficiency of the Converter

Converter efficiency depends on component parameters, which have not yet been selected. For design purposes, an efficiency of 90% can be used for V_{IN} less than 10V and 85% can be used for V_{IN} greater than 10V. The efficiency can be more accurately calculated once the design is complete. If the assumed efficiency is grossly inaccurate, a second iteration through the design procedure can be made.

For the high-side switch, the conduction power loss is:

EQUATION 5-20:

$$P_{COND(SWHS)} = R_{DSON(HS)} \times I_{SWHS(RMS)}^{2}$$

Where:

$R_{DSON(HS)}$ = High-side MOSFET ON-Resistance

Because the AC switching losses for the low-side MOSFET is near zero, the total power dissipation of the low-side MOSFET is:

EQUATION 5-21:

$$P_{D(SWLS)} = P_{COND(SWLS)} = R_{DSON(LS)} \times I_{SWLS(RMS)}^{2}$$

Where:

$R_{DSON(LS)}$ = Low-side MOSFET ON-Resistance

The total power dissipation for the high-side MOSFET is:

EQUATION 5-22:

$$P_{D(SWHS)} = P_{COND(SWHS)} + P_{AC(SWHS)}$$

5.4 External Schottky Diode

An external freewheeling diode is used to keep the inductor current flow continuously while both MOSFETs are turned off during dead time. This dead time prevents current from flowing unimpeded through both MOSFETs and is typically 80 ns The diode conducts twice during each switching cycle. Although the average current through this diode is small, the diode must be able to handle the peak current.

EQUATION 5-23:

$$I_{D(AVG)} = I_{OUT} \times 2 \times 80ns \times f_{SW}$$

The reverse voltage requirement of the diode is:

EQUATION 5-24:

$$V_{DIODE(RRM)} = V_{IN}$$

The power dissipated by the Schottky diode is:

EQUATION 5-25:

$$P_{DIODE} = I_{D(AVG)} \times V_F$$

Where:

V_F = Forward Voltage at the Peak Diode Current

The external freewheeling Schottky diode, D1, is not necessary for circuit operation since the low-side MOSFET contains a parasitic body diode. The external diode will improve efficiency and decrease high frequency noise. If the MOSFET body diode is used, it must be rated to handle the peak and average current. The body diode has a relatively slow reverse recovery time and a relatively high forward voltage drop. The power lost in the diode is proportional to the forward voltage drop of the diode. As the high-side MOSFET starts to turn on, the body diode becomes a short circuit for the reverse recovery period, dissipating additional power. The diode recovery and the circuit inductance will cause ringing during the high-side MOSFET turn-on.

An external Schottky diode conducts at a lower forward voltage preventing the body diode in the MOSFET from turning on. The lower forward voltage drop dissipates less power than the body diode. The lack of a reverse recovery mechanism in a Schottky diode causes less ringing and less power loss. Depending on the circuit components and operating conditions, an external Schottky diode will give a 1/2% to 1% improvement in efficiency. Figure 5-1 illustrates the difference in noise on the VSW pin with and without a Schottky diode.

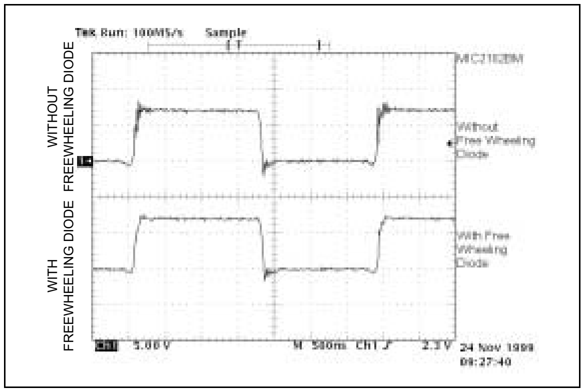


FIGURE 5-1: Switch Output Noise With and Without Schottky Diode.

5.5 Output Capacitor Selection

The output capacitor values are usually determined by the capacitors ESR (equivalent series resistance). Voltage rating and RMS current capability are two other important factors in selecting the output capacitor. Recommended capacitors are tantalum, low-ESR aluminum electrolytics, and OS-CON.

The output capacitor's ESR is usually the main cause of output ripple. The maximum value of ESR is calculated by:

EQUATION 5-26:

$$ESR_{COUT} \leq \frac{\Delta V_{OUT}}{\Delta I_{L(PP)}}$$

Where:

ΔV_{OUT} = Peak-to-peak output voltage ripple

$\Delta I_{L(PP)}$ = Peak-to-peak inductor ripple current

The total output ripple is a combination of output ripple voltages due to the ESR and the output capacitance. The total ripple is calculated below:

EQUATION 5-27:

$$\Delta V_{OUT} = \sqrt{\left(\frac{\Delta I_{L(PP)}}{8 \times C_{OUT} \times f_{SW}}\right)^2 + (\Delta I_{L(PP)} \times ESR_{COUT})^2}$$

Where:
C_{OUT} = Output capacitance value
f_{SW} = Switching frequency
ESR_{COUT} = ESR of output capacitor

The voltage rating of capacitor should be twice the output voltage for a tantalum and 20% greater for an aluminum electrolytic or OS-CON.

The output capacitor RMS current is calculated below:

EQUATION 5-28:

$$I_{COUT(RMS)} = \frac{\Delta I_{L(PP)}}{\sqrt{12}}$$

The power dissipated in the output capacitor is:

EQUATION 5-29:

$$P_{DISS(COUT)} = I_{COUT(RMS)}^2 \times ESR_{COUT}$$

5.6 Input Capacitor Selection

The input capacitor should be selected for ripple current rating and voltage rating. Tantalum input capacitors may fail when subjected to high inrush currents, caused by turning the input supply on. Tantalum input capacitor voltage rating should be at least twice the maximum input voltage to maximize reliability. Aluminum electrolytic, OS-CON, and multilayer polymer film capacitors can handle the higher inrush currents without voltage derating.

The input voltage ripple will primarily depend on the input capacitors ESR. The peak input current is equal to the peak inductor current, so:

EQUATION 5-30:

$$\Delta V_{IN} = I_{L(PK)} \times ESR_{CIN}$$

Where:
ESR_{CIN} = ESR of input capacitor.

The input capacitor must be rated for the input current ripple. The RMS value of input capacitor current is determined at the maximum output current. Assuming the peak to peak inductor ripple current is low:

EQUATION 5-31:

$$I_{CIN(RMS)} \approx I_{OUT(MAX)} \times \sqrt{D \times (1 - D)}$$

The power dissipated in the input capacitor is:

EQUATION 5-32:

$$P_{DISS(CIN)} = I_{CIN(RMS)}^2 \times ESR_{CIN}$$

5.7 Voltage Setting Components

The MIC2182-3.3 and MIC2182-5.0 ICs contain internal voltage dividers that set the output voltage. The MIC2182 adjustable version requires two resistors to set the output voltage as shown in Figure 5-2.

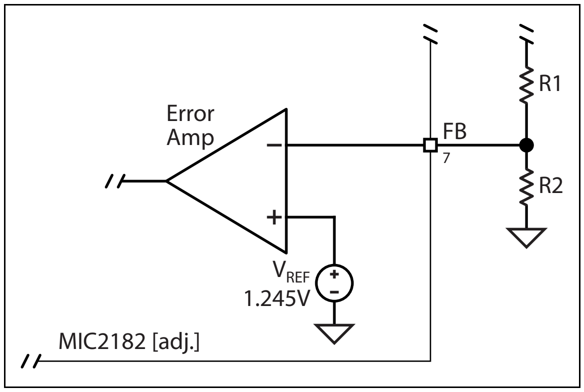


FIGURE 5-2: *Voltage Divider Configuration.*

The output voltage is determined by the equation:

EQUATION 5-33:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R1}{R2}\right)$$

Where:

V_{REF} for the MIC2182 is typically 1.245V

A typical value of R1 can be between 3 kΩ and 10 kΩ. If R1 is too large, it may allow noise to be introduced into the voltage feedback loop. If R1 is too small in value, it will decrease the efficiency of the buck converter, especially at low output loads.

Once R1 is selected, R2 can be calculated using:

EQUATION 5-34:

$$R2 = \frac{V_{REF} \times R1}{V_{OUT} - V_{REF}}$$

5.7.1 VOLTAGE DIVIDER POWER DISSIPATION

The reference voltage and R2 set the current through the voltage divider.

EQUATION 5-35:

$$I_{DIVIDER} = \frac{V_{REF}}{R2}$$

The power dissipated by the divider resistors is:

EQUATION 5-36:

$$P_{DIVIDER} = (R1 + R2) \times I_{DIVIDER}^{\ 2}$$

5.8 Efficiency Calculation and Considerations

Efficiency is the ratio of output power to input power. The difference is dissipated as heat in the buck converter. Under light output load, the significant contributors are:

- Supply current to the MIC2182
- MOSFET gate-charge power (included in the IC supply current)
- Core losses in the output inductor

To maximize efficiency at light loads:

- Use a low gate-charge MOSFET or use the smallest MOSFET, which is still adequate for maximum output current.
- Allow the MIC2182 to run in skip mode at lower currents.
- Use a ferrite material for the inductor core, which has less core loss than an MPP or iron powder core.

Under heavy output loads, the significant contributors to power loss are (in approximate order of magnitude):

- Resistive on-time losses in the MOSFETs
- Switching transition losses in the MOSFETs
- Inductor resistive losses
- Current-sense resistor losses
- Input capacitor resistive losses (due to the capacitor's ESR)

To minimize power loss under heavy loads:

- Use logic-level, low on-resistance MOSFETs. Multiplying the gate charge by the on-resistance gives a figure of merit, providing a good balance between low and high load efficiency.
- Slow transition times and oscillations on the voltage and current waveforms dissipate more power during turn-on and turnoff of the MOSFETs. A clean layout will minimize parasitic inductance and capacitance in the gate drive and high current paths. This will allow the fastest transition times and waveforms without oscillations. Low gate-charge MOSFETs will transition faster than those with higher gate-charge requirements.
- For the same size inductor, a lower value will have fewer turns and therefore, lower winding resistance. However, using too small of a value will require more output capacitors to filter the output ripple, which will force a smaller bandwidth, slower transient response and possible instability under certain conditions.
- Lowering the current-sense resistor value will decrease the power dissipated in the resistor. However, it will also increase the overcurrent limit and will require larger MOSFETs and inductor components.
- Use low-ESR input capacitors to minimize the power dissipated in the capacitors ESR.

5.9 Decoupling Capacitor Selection

The 4.7 µF decoupling capacitor is used to minimize noise on the VDD pin. The placement of this capacitor is critical to the proper operation of the IC. It must be placed right next to the pins and routed with a wide trace. The capacitor should be a good quality tantalum. An additional 1 µF ceramic capacitor may be necessary when driving large MOSFETs with high gate capacitance. Incorrect placement of the VDD decoupling capacitor will cause jitter or oscillations in the switching waveform and large variations in the overcurrent limit.

A 0.1 µF ceramic capacitor is required to decouple the VIN. The capacitor should be placed near the IC and connected directly to between Pin 10 (VIN) and Pin 12 (PGND).

5.10 Components Selection of Predesigned Circuits

A single schematic diagram, shown in Figure 5-3, can be used to build power supplies ranging from 3A to 10A at the common output voltages of 1.8V, 2.5V, 3.3V, and 5V. Components that vary, depending upon output current and voltage, are listed in Table 5-3 through Table 5-6.

Power supplies larger than 10A can also be constructed using the MIC2182 by using larger power-handling components.

Figure 2-16 through Figure 2-29 provide useful information about the actual performance of some of these circuits.

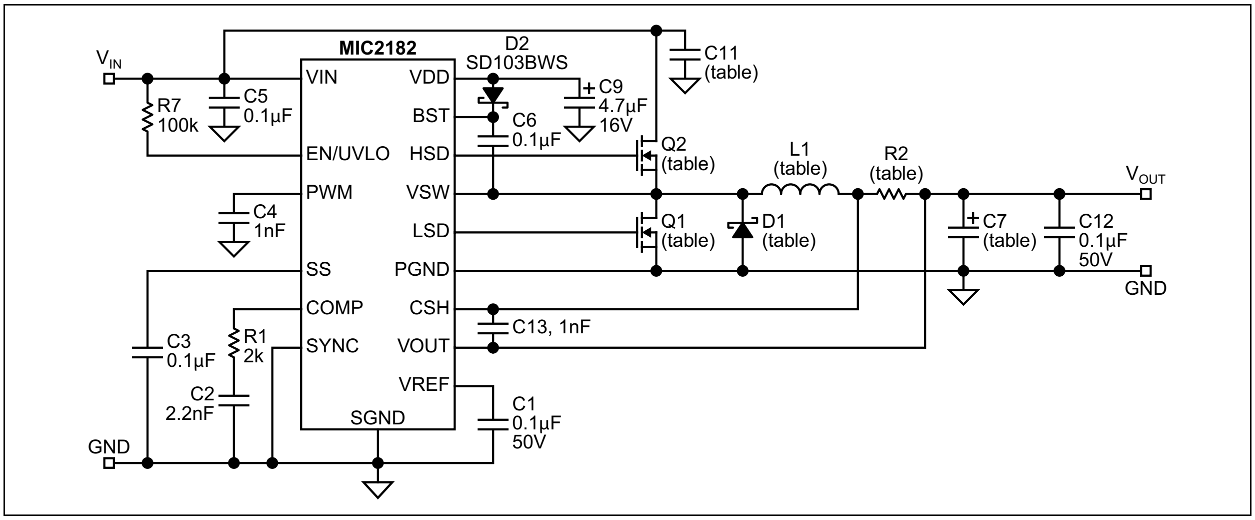


FIGURE 5-3: *Basic Circuit Diagram for use with Table 5-3 through Table 5-6.*

TABLE 5-1: SPECIFICATIONS FOR FIGURE 5-3 & TABLE 5-3 THROUGH TABLE 5-6

Specification	Limit
Switching Frequency Ripple	1% of Output Voltage
Max. Ambient Temp.	+85°C
Short-Circuit Capability	Continuous
Switching Frequency	300 kHz

TABLE 5-2: COMPONENT SUPPLIERS

Manufacturer	Website Address
Microchip Technology Inc.	www.microchip.com
Kyocera AVX	www.kyocera-avx.com
Central Semiconductor	www.centralsemi.com
Eaton	www.eaton.com
Infineon	www.infineon.com
Vishay	www.vishay.com
Sumida	www.sumida.com

TABLE 5-3: COMPONENTS FOR 5V OUTPUT

Reference	3A (6.5V to 30V) Part No./Desc.	4A (6.5V to 30V) Part No./Desc.	5A (6.5V to 30V) Part No./Desc.	10A (6.5V to 30V) Part No./Desc.
C7	Qty: 2 TPSE227M010R0100 Kyocera AVX, 220µF 10V, 0.1Ω ESR, Output filter capacitor	Qty: 2 TPSE227M010R0100 Kyocera AVX, 220µF 10V, 0.1Ω ESR, Output filter capacitor	Qty: 2 TPSE227M010R0060 Kyocera AVX, 220µF 10V, 0.06Ω ESR, Output filter capacitor	Qty: 2 TPSV337M010R0060 Kyocera AVX, 330µF 10V, 0.06Ω ESR, Output filter capacitor
C11	Qty: 2 TPSE226M035R0300 Kyocera AVX, 22µF 35V, 0.3Ω ESR, Input filter capacitor	Qty: 3 TPSE226M035R0300 Kyocera AVX, 22µF 35V, 0.3Ω ESR, Input filter capacitor	Qty: 4 TPSE226M035R0300 Kyocera AVX, 22µF 35V, 0.3Ω ESR, Input filter capacitor	Qty: 4 TPSV107M020R0085 Kyocera AVX, 100µF 20V, 0.085Ω ESR, Input filter capacitor
D1	Qty: 1 B140, Vishay, Freewheeling diode	Qty: 1 B140, Vishay, Freewheeling diode	Qty: 1 B140, Vishay, Freewheeling diode	Qty: 1 B330, Vishay, Freewheeling diode
L1	Qty: 1 CDRH125NP-100MC, Sumida, 10µH 4A, Output inductor	Qty: 1 CDRH127NP-100MC, Sumida, 10µH 5A, Output inductor	Qty: 1 CDRH127NP-100MC, Sumida, 10µH 5A, Output inductor	Qty: 1 UP4B-3R3, Eaton, 3.3µH 11A, Output inductor
Q1	Qty: 1 Si4800BDY, Vishay, Low-side MOSFET	Qty: 1 Si4800BDY, Vishay, Low-side MOSFET	Qty: 1 Si4884BDY, Vishay, Low-side MOSFET	Qty: 2 Si4884BDY, Vishay, Low-side MOSFET
Q2	Qty: 1 Si4800BDY, Vishay, High-side MOSFET	Qty: 1 Si4800BDY, Vishay, High-side MOSFET	Qty: 1 Si4884BDY, Vishay, High-side MOSFET	Qty: 2 Si4884BDY, Vishay, High-side MOSFET
R2	Qty: 1 WSL2010R0250F, Vishay, 0.025, 1%, 0.5W, Current sense resistor	Qty: 1 WSL2010R0200F, Vishay, 0.02, 1%, 0.5W, Current sense resistor	Qty: 1 WSL2512R0150F, Vishay, 0.015, 1%, 1W, Current sense resistor	Qty: 2 WSL2512R0150F, Vishay, 0.015, 1%, 1W, Current sense resistor
U1	MIC2182-5.0YSM or MIC2182-5.0YM	MIC2182-5.0YSM or MIC2182-5.0YM	MIC2182-5.0YSM or MIC2182-5.0YM	MIC2182-5.0YM

TABLE 5-4: COMPONENTS FOR 3.3V OUTPUT

Reference	3A (6.5V to 30V) Part No./Desc.	4A (6.5V to 30V) Part No./Desc.	5A (6.5V to 30V) Part No./Desc.	10A (6.5V to 30V) Part No./Desc.
C7	Qty: 2 TPSE227M010R0100 Kyocera AVX, 220µF 10V, 0.1Ω ESR, Output filter capacitor	Qty: 2 TPSE227M010R0100 Kyocera AVX, 220µF 10V, 0.1Ω ESR, Output filter capacitor	Qty: 2 TPSE227M010R0060 Kyocera AVX, 220µF 10V, 0.06Ω ESR, Output filter capacitor	Qty: 2 TPSV477M006R0055 Kyocera AVX, 470µF 6.3V, 0.055Ω ESR, Output filter capacitor
C11	Qty: 2 TPSE226M035R0300 Kyocera AVX, 22µF 35V, 0.3Ω ESR, Input filter capacitor	Qty: 2 TPSE226M035R0300 Kyocera AVX, 22µF 35V, 0.3Ω ESR, Input filter capacitor	Qty: 3 TPSE226M035R0300 Kyocera AVX, 22µF 35V, 0.3Ω ESR, Input filter capacitor	Qty: 3 TPSV227M016R0075 Kyocera AVX, 220µF 16V, 0.075Ω ESR, Input filter capacitor
D1	Qty: 1 B140, Vishay, Freewheeling diode	Qty: 1 B140, Vishay, Freewheeling diode	Qty: 1 B140, Vishay, Freewheeling diode	Qty: 1 B330, Vishay, Freewheeling diode
L1	Qty: 1 CDRH125NP-100MC, Sumida, 10µH 4A, Output inductor	Qty: 1 CDRH127NP-100MC, Sumida, 10µH 5A, Output inductor	Qty: 1 CDRH127NP-100MC, Sumida, 10µH 5A, Output inductor	Qty: 1 UP4B-3R3, Eaton, 3.3µH 11A, Output inductor
Q1	Qty: 1 Si4800BDY, Vishay, Low-side MOSFET	Qty: 1 Si4800BDY, Vishay, Low-side MOSFET	Qty: 1 Si4800BDY, Vishay, Low-side MOSFET	Qty: 2 Si4884BDY, Vishay, Low-side MOSFET
Q2	Qty: 1 Si4800BDY, Vishay, High-side MOSFET	Qty: 1 Si4800BDY, Vishay, High-side MOSFET	Qty: 1 Si4800BDY, Vishay, High-side MOSFET	Qty: 2 Si4884BDY, Vishay, High-side MOSFET
R2	Qty: 1 WSL2010R0250F, Vishay, 0.025, 1%, 0.5W, Current sense resistor	Qty: 1 WSL2010R0200F, Vishay, 0.02, 1%, 0.5W, Current sense resistor	Qty: 1 WSL2512R0150F, Vishay, 0.015, 1%, 1W, Current sense resistor	Qty: 2 WSL2512R0150F, Vishay, 0.015, 1%, 1W, Current sense resistor
U1	MIC2182-3.3YSM or MIC2182-3.3YM	MIC2182-3.3YSM or MIC2182-3.3YM	MIC2182-3.3YSM or MIC2182-3.3YM	MIC2182-3.3YM

TABLE 5-5: COMPONENTS FOR 2.5V OUTPUT

Reference	3A (6.5V to 30V) Part No./Desc.	4A (6.5V to 30V) Part No./Desc.	5A (6.5V to 30V) Part No./Desc.	10A (6.5V to 30V) Part No./Desc.
C7	Qty: 2 TPSE227M010R0100 Kyocera AVX, 220µF 10V, 0.1Ω ESR, Output filter capacitor	Qty: 2 TPSE227M010R0100 Kyocera AVX, 220µF 10V, 0.1Ω ESR, Output filter capacitor	Qty: 2 TPSE227M010R0060 Kyocera AVX, 220µF 10V, 0.06Ω ESR, Output filter capacitor	Qty: 2 TPSV477M006R0055 Kyocera AVX, 470µF 6.3V, 0.055Ω ESR, Output filter capacitor
C11	Qty: 2 TPSE226M035R0300 Kyocera AVX, 22µF 35V, 0.3Ω ESR, Input filter capacitor	Qty: 2 TPSE226M035R0300 Kyocera AVX, 22µF 35V, 0.3Ω ESR, Input filter capacitor	Qty: 2 TPSE226M035R0300 Kyocera AVX, 22µF 35V, 0.3Ω ESR, Input filter capacitor	Qty: 3 TPSV227M016R0075 Kyocera AVX, 220µF 16V, 0.075Ω ESR, Input filter capacitor
D1	Qty: 1 B140, Vishay, Freewheeling diode	Qty: 1 B140, Vishay, Freewheeling diode	Qty: 1 B140, Vishay, Freewheeling diode	Qty: 1 B330, Vishay, Freewheeling diode
L1	Qty: 1 CDRH125NP-100MC, Sumida, 10µH 4A, Output inductor	Qty: 1 CDRH127NP-100MC, Sumida, 10µH 5A, Output inductor	Qty: 1 CDRH127NP-100MC, Sumida, 10µH 5A, Output inductor	Qty: 1 UP4B-3R3, Eaton, 3.3µH 11A, Output inductor
Q1	Qty: 1 Si4800BDY, Vishay, Low-side MOSFET	Qty: 1 Si4884BDY, Vishay, Low-side MOSFET	Qty: 1 Si4884BDY, Vishay, Low-side MOSFET	Qty: 2 Si4884BDY, Vishay, Low-side MOSFET
Q2	Qty: 1 Si4800BDY, Vishay, High-side MOSFET	Qty: 1 Si4800BDY, Vishay, High-side MOSFET	Qty: 1 Si4800BDY, Vishay, High-side MOSFET	Qty: 2 Si4884BDY, Vishay, High-side MOSFET
R2	Qty: 1 WSL2010R0250F, Vishay, 0.025, 1%, 0.5W, Current sense resistor	Qty: 1 WSL2010R0200F, Vishay, 0.02, 1%, 0.5W, Current sense resistor	Qty: 1 WSL2512R0150F, Vishay, 0.015, 1%, 1W, Current sense resistor	Qty: 2 WSL2512R0150F, Vishay, 0.015, 1%, 1W, Current sense resistor
U1	MIC2182YSM or MIC2182YM	MIC2182YSM or MIC2182YM	MIC2182YSM or MIC2182YM	MIC2182YM

TABLE 5-6: COMPONENTS FOR 1.8V OUTPUT

Reference	3A (6.5V to 30V) Part No./Desc.	4A (6.5V to 30V) Part No./Desc.	5A (6.5V to 30V) Part No./Desc.	10A (6.5V to 30V) Part No./Desc.
C7	Qty: 2 TPSE227M010R0100 Kyocera AVX, 220µF 10V, 0.1Ω ESR, Output filter capacitor	Qty: 2 TPSE227M010R0100 Kyocera AVX, 220µF 10V, 0.1Ω ESR, Output filter capacitor	Qty: 2 TPSE227M010R0060 Kyocera AVX, 220µF 10V, 0.06Ω ESR, Output filter capacitor	Qty: 2 TPSV477M006R0055 Kyocera AVX, 470µF 6.3V, 0.055Ω ESR, Output filter capacitor
C11	Qty: 2 TPSE226M035R0300 Kyocera AVX, 22µF 35V, 0.3Ω ESR, Input filter capacitor	Qty: 2 TPSE226M035R0300 Kyocera AVX, 22µF 35V, 0.3Ω ESR, Input filter capacitor	Qty: 2 TPSE226M035R0300 Kyocera AVX, 22µF 35V, 0.3Ω ESR, Input filter capacitor	Qty: 2 TPSV227M016R0075 Kyocera AVX, 220µF 16V, 0.075Ω ESR, Input filter capacitor
D1	Qty: 1 B140, Vishay, Freewheeling diode	Qty: 1 B140, Vishay, Freewheeling diode	Qty: 1 B140, Vishay, Freewheeling diode	Qty: 1 B330, Vishay, Freewheeling diode
L1	Qty: 1 CDRH125NP-100MC, Sumida, 10µH 4A, Output inductor	Qty: 1 CDRH127NP-100MC, Sumida, 10µH 5A, Output inductor	Qty: 1 CDRH127NP-100MC, Sumida, 10µH 5A, Output inductor	Qty: 1 UP4B-3R3, Eaton, 3.3µH 11A, Output inductor
Q1	Qty: 1 Si4800BDY, Vishay, Low-side MOSFET	Qty: 1 Si4884BDY, Vishay, Low-side MOSFET	Qty: 1 Si4884BDY, Vishay, Low-side MOSFET	Qty: 2 Si4884BDY, Vishay, Low-side MOSFET
Q2	Qty: 1 Si4800BDY, Vishay, High-side MOSFET	Qty: 1 Si4800BDY, Vishay, High-side MOSFET	Qty: 1 Si4800BDY, Vishay, High-side MOSFET	Qty: 2 Si4884BDY, Vishay, High-side MOSFET
R2	Qty: 1 WSL2010R0250F, Vishay, 0.025, 1%, 0.5W, Current sense resistor	Qty: 1 WSL2010R0200F, Vishay, 0.02, 1%, 0.5W, Current sense resistor	Qty: 1 WSL2512R0150F, Vishay, 0.015, 1%, 1W, Current sense resistor	Qty: 2 WSL2512R0150F, Vishay, 0.015, 1%, 1W, Current sense resistor
U1	MIC2182YSM or MIC2182YM	MIC2182YSM or MIC2182YM	MIC2182YSM or MIC2182YM	MIC2182YM

5.11 PCB Layout and Checklist

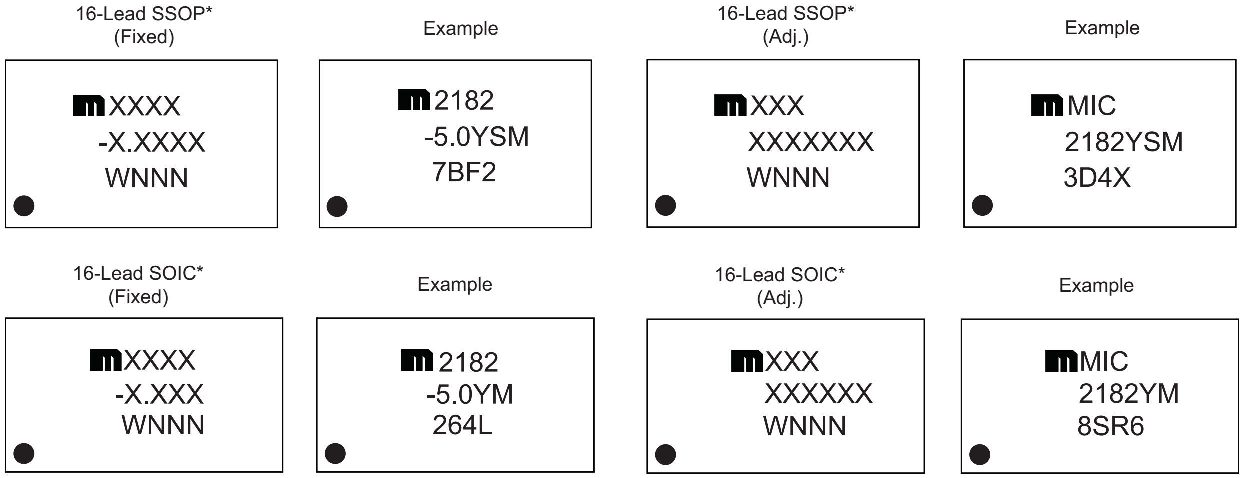
PCB layout is critical to achieve reliable, stable and efficient performance. A ground plane is required to control EMI and minimize the inductance in power and signal return paths.

The following guidelines should be followed to insure proper operation of the circuit.

- Signal and power grounds should be kept separate and connected at only one location. Large currents or high di/dt signals that occur when the MOSFETs turn on and off must be kept away from the small signal connections.
- The connection between the current-sense resistor and the MIC2182 current-sense inputs (Pins 8 and 9) should have separate traces, routed from the terminals directly to the IC pins. The traces should be routed as closely as possible to each other and their length should be minimized. Avoid running the traces under the inductor and other switching components. A 1 nF to 0.1 µF capacitor placed between Pins 8 and 9 will help attenuate switching noise on the current sense traces. This capacitor should be placed close to Pins 8 and 9.
- When the high-side MOSFET is switched on, the critical flow of current is from the input capacitor through the MOSFET, inductor, sense resistor, output capacitor, and back to the input capacitor. These paths must be made with short, wide pieces of trace. It is good practice to locate the ground terminals of the input and output capacitors close to each other.
- When the low-side MOSFET is switched on, current flows through the inductor, sense resistor, output capacitor, and MOSFET. The source of the low-side MOSFET should be located close to the output capacitor.
- The freewheeling diode, D1 in the Block Diagrams, conducts current during the dead time, when both MOSFETs are off. The anode of the diode should be located close to the output capacitor ground terminal and the cathode should be located close to the input side of the inductor.
- The 4.7 µF capacitor, which connects to the VDD terminal (Pin 11) must be located right at the IC. The VDD terminal is very noise sensitive and placement of this capacitor is very critical. Connections must be made with wide trace. The capacitor may be located on the bottom layer of the board and connected to the IC with multiple vias.
- The VIN bypass capacitor should be located close to the IC and connected between Pins 10 and 12. Connections should be made with a ground and power plane or with short, wide trace.

6.0 PACKAGING INFORMATION

6.1 Package Marking Information



Legend:		
	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.

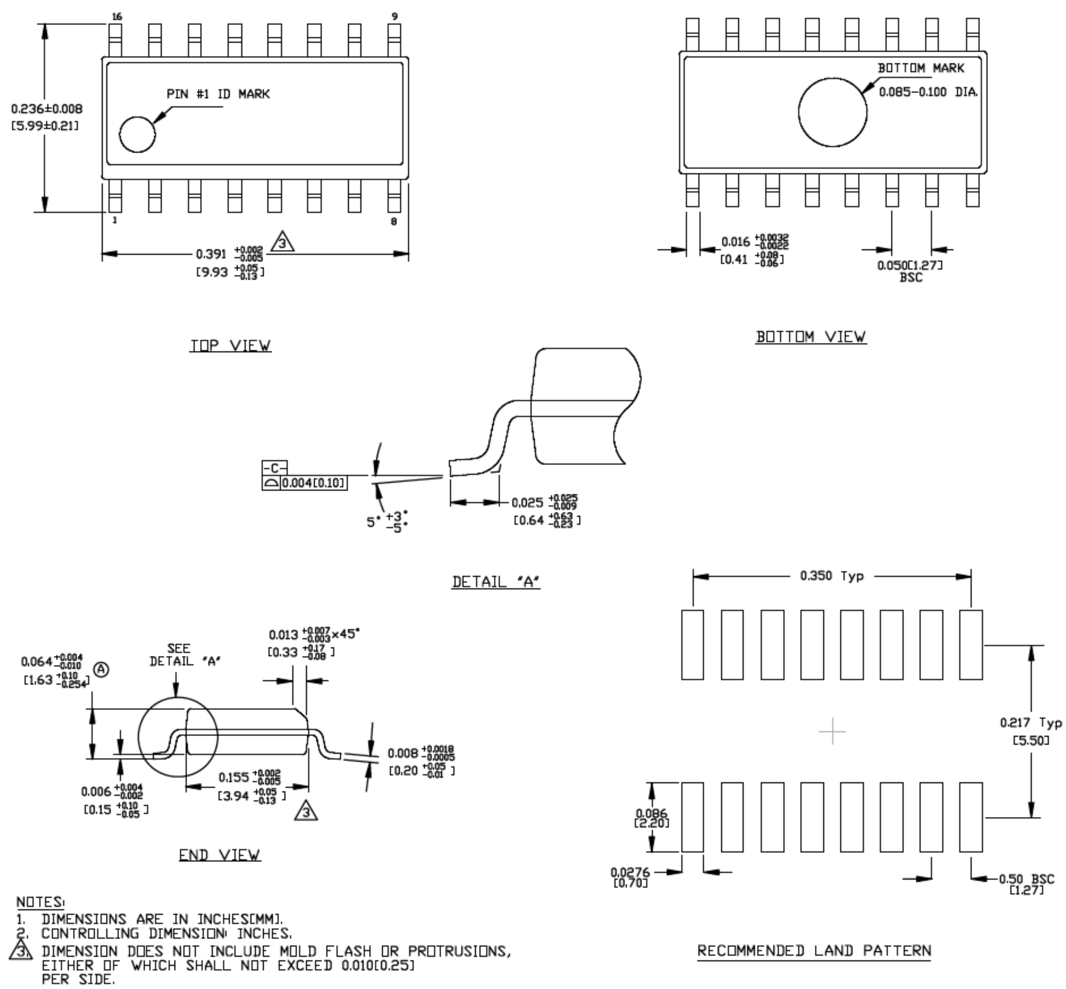
Underbar (_) and/or Overbar (‾) symbol may not be to scale.

Note: If the full seven-character YYWWNNN code cannot fit on the package, the following truncated codes are used based on the available marking space:
6 Characters = YWWNNN; 5 Characters = WWNNN; 4 Characters = WNNN; 3 Characters = NNN;
2 Characters = NN; 1 Character = N

16-Lead SOIC Package Outline and Recommended Land Pattern

TITLE
16 LEAD SOICN PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

DRAWING #	SOICN-16LD-PL-1	**UNIT**	INCH [MM]
Lead Frame	Copper	**Lead Finish**	Matte Tin

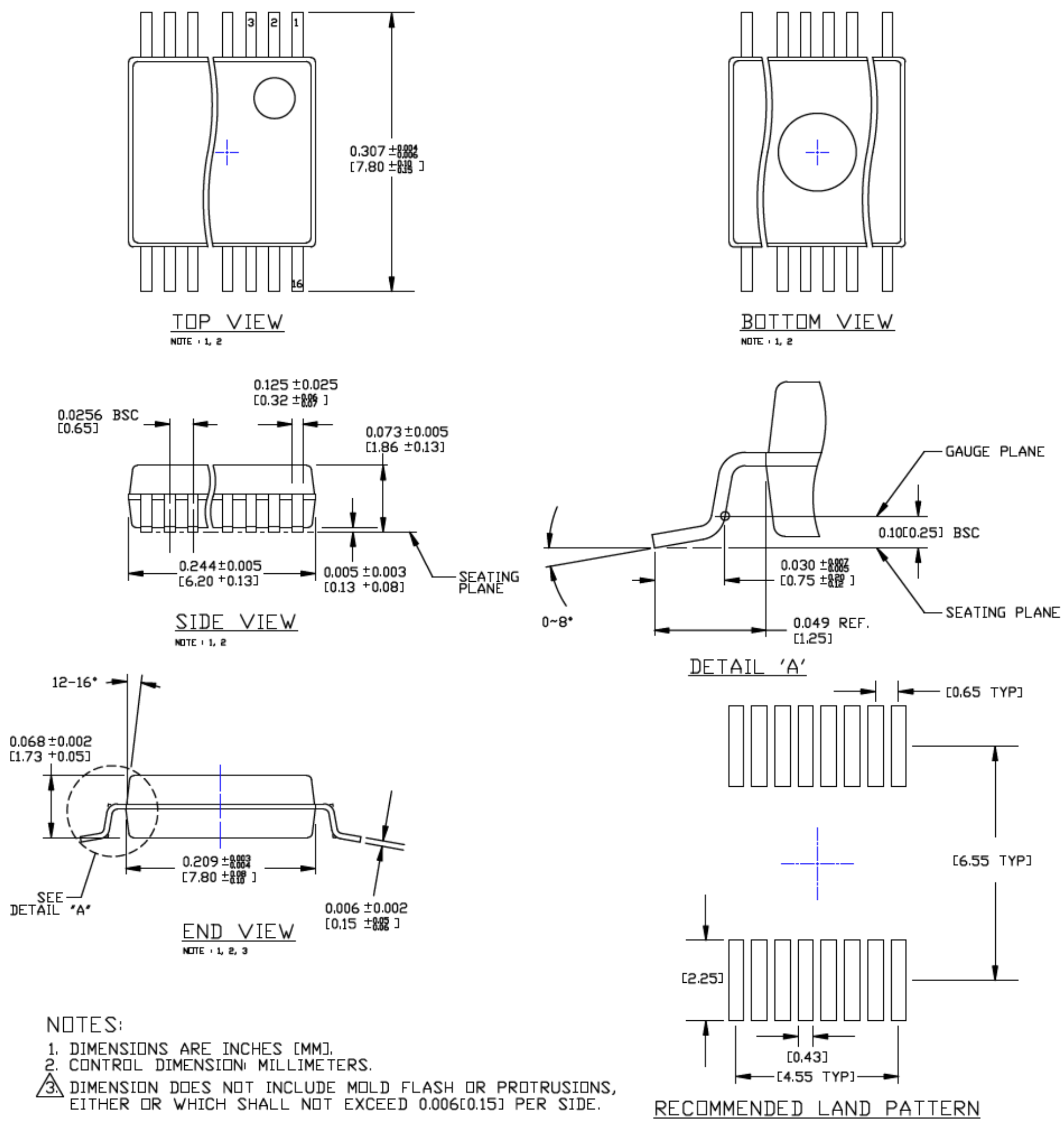


Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

16-Lead SSOP Package Outline and Recommended Land Pattern

TITLE
16 LEAD SSOP PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

DRAWING #	SSOP-16LD-PL-1	**UNIT**	INCH [MM]



Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (February 2022)

- Converted Micrel document MIC2182 to Microchip data sheet DS20006644A.
- Minor text changes throughout.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	–X.X	X	XX	–XX
Device	Output Voltage	Junction Temperature Range	Package	Media Type

Device:	MIC2182: High-Efficiency Synchronous Buck Controller
Output Voltage:	<blank> = Adjustable -3.3 = 3.3V -5.0 = 5.0V
Junction Temperature Range:	Y = –40°C to +125°C (RoHs Compliant)
Package:	M = 16-Lead SOIC (.150in) SM = 16-Lead SSOP (5.3mm)
Media Type:	<blank> = 48/Tube (M, SOIC) <blank> = 77/Tube (SM, SSOP) TR = 1,000/Reel (SM, SSOP) TR = 2,500/Reel (M, SOIC)

Examples:

a) MIC2182YM:	High Efficiency Synchronous Buck Controller, ADJ Output Voltage, –40°C to +125°C Junction Temperature Range, RoHS Compliant, 16-Lead SOIC (.150 in) Package, 48/Tube
b)MIC2182-3.3YM:	High Efficiency Synchronous Buck Controller, 3.3V Output Voltage, –40°C to +125°C Junction Temperature Range, RoHS Compliant, 16-Lead SOIC (.150 in) Package, 48/Tube
c) MIC2182-5.0YM-TR:	High Efficiency Synchronous Buck Controller, 5.0V Output Voltage, –40°C to +125°C Junction Temperature Range, RoHS Compliant, 16-Lead SOIC (.150 in) Package, 2500/Reel
d) MIC2182YSM:	High Efficiency Synchronous Buck Controller, ADJ Output Voltage, –40°C to +125°C Junction Temperature Range, RoHS Compliant, 16-Lead SSOP (5.3 mm) Package, 77/Tube
e) MIC2182-3.3YSM	High Efficiency Synchronous Buck Controller, 3.3V Output Voltage, –40°C to +125°C Junction Temperature Range, RoHS Compliant, 16-Lead SSOP (5.3 mm) Package, 77/Tube
f) MIC2182-5.0YSM-TR:	High Efficiency Synchronous Buck Controller, 5.0V Output Voltage, –40°C to +125°C Junction Temperature Range, RoHS Compliant, 16-Lead SSOP (5.3 mm) Package, 1000/Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

Note the following details of the code protection feature on Microchip products:

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