采用PD的可编程USB Type-C控制器

FUSB302B

WLCSP9
CASE 567TN

WQFN14
CASE 510BR

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

说明

FUSB302B面向期望实现DRP/SRC/SNK USB Type-C连接器，但需要少量编程的系统设计人员。

FUSB302B支持USB Type-C检测，包括连接和方向。FUSB302B集成了USB BMC电力输送协议的物理层，允许高达100 W功率和角色互换。BMC的PD模块全面支持Type-C规格的替代接口。

产品特性

- 自动DRP切换的双角色功能
- 基于连接对象可以作为主机或设备进行连接的能力。
- 软件可配置为专用主机、专用设备或双角色。
  - 专用设备可以在带固定CC或VCONN通道的Type-C插座或插头上运行。
- 完全支持Type-C 1.2。集成CC引脚的以下功能
  - 作为主机进行连接/分离检测
  - 作为主机进行电流能力指示
  - 作为设备进行电流能力指示
  - 音频适配器附件模式
  - 调试附件模式
  - 主动电缆检测
- 将CCx集成到VCONN开关上，为所有具有USB 3.1功能的电源线缆提供过流限制。
- USB电力输送(PD) 2.0，支持1.2版本
  - 自动GoodCRC报文响应
  - 未收到GoodCRC时自动重发报文
  - 需要时，自动软重置重发报文
  - 自动硬重置发送命令集
- 电池耗尽支持(无电量时支持SNK模式)
- 低功耗运行： I_{CC} = 25 μA (典型值)
- 封装：
  - 9焊点WLCSP (1.215 mm × 1.260 mm)
  - 14引脚MLP (2.5 mm × 2.5 mm, 0.5 mm间距)

应用

- 智能手机
- 平板电脑
- 膝上型电脑
- 笔记本电脑
- 电源适配器
- 相机
- 加密狗

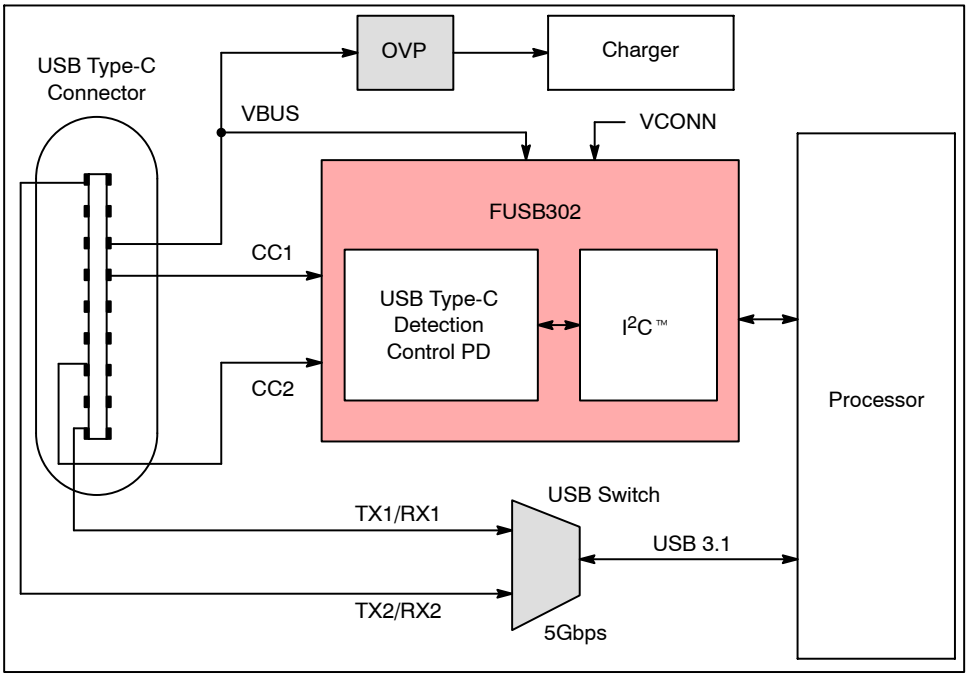


Figure 1. Block Diagram

Table 1. ORDERING INFORMATION

Part Number	Top Mark	Operating Temperature Range	Package	Shipping†
FUSB302BUCX	H4	−40 to 85°C	9-ball Wafer-level Chip Scale Package (WLCSP), 0.4 mm Pitch	3,000 / Tape and Reel
FUSB302BMPX	UA	−40 to 85°C	14-lead MLP 2.5 mm × 2.5 mm, 0.5 mm Pitch	
FUSB302B01MPX	UP			
FUSB302B10MPX	US			
FUSB302B11MPX	UT			
FUSB302BVMPX	DA	−40 to 105°C		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

典型应用

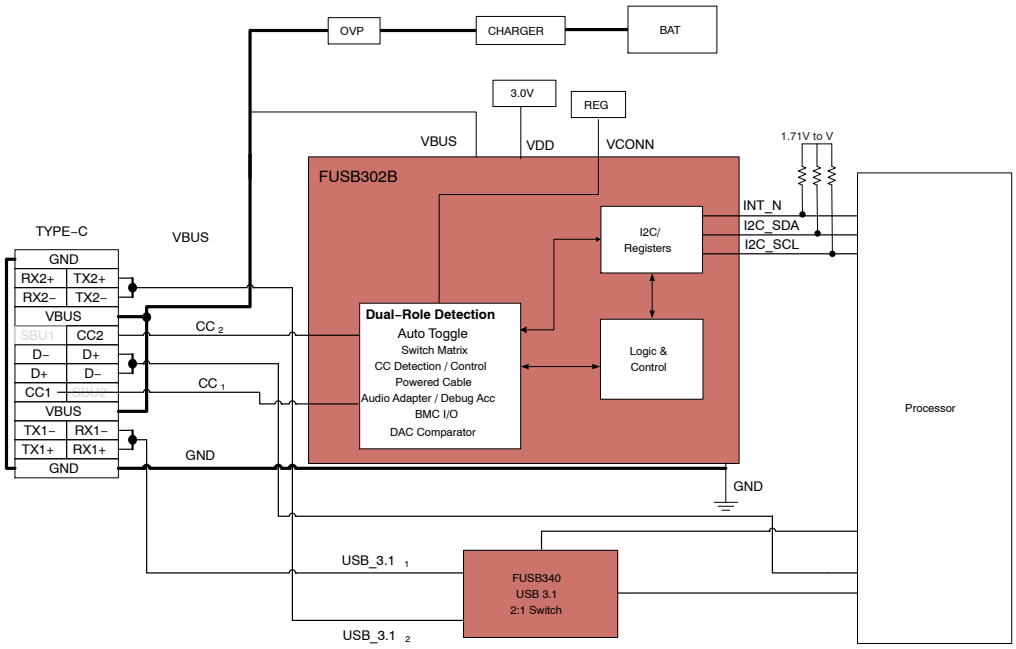


Figure 2. Typical Application

框图

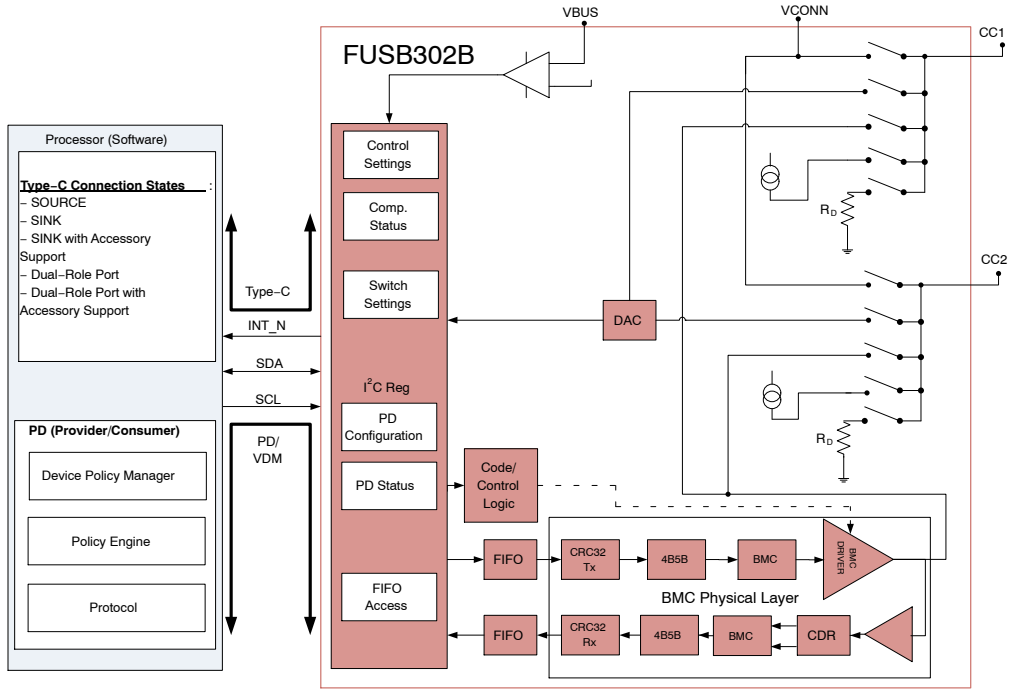


Figure 3. Functional Block Diagram

引脚布局

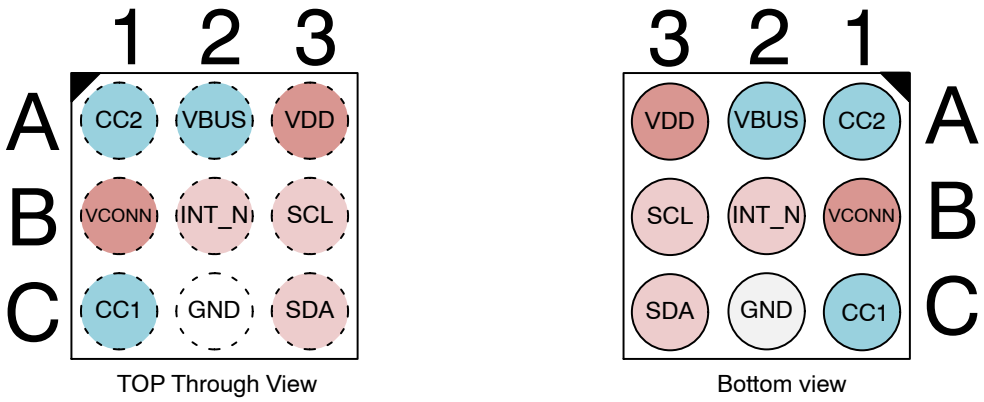


Figure 4. FUSB302BUCX Pin Assignment

Table 2. PIN MAP

	Column 1	Column 2	Column 3
Row A	CC2	VBUS	VDD
Row B	VCONN	INT_N	SCL
Row C	CC1	GND	SDA

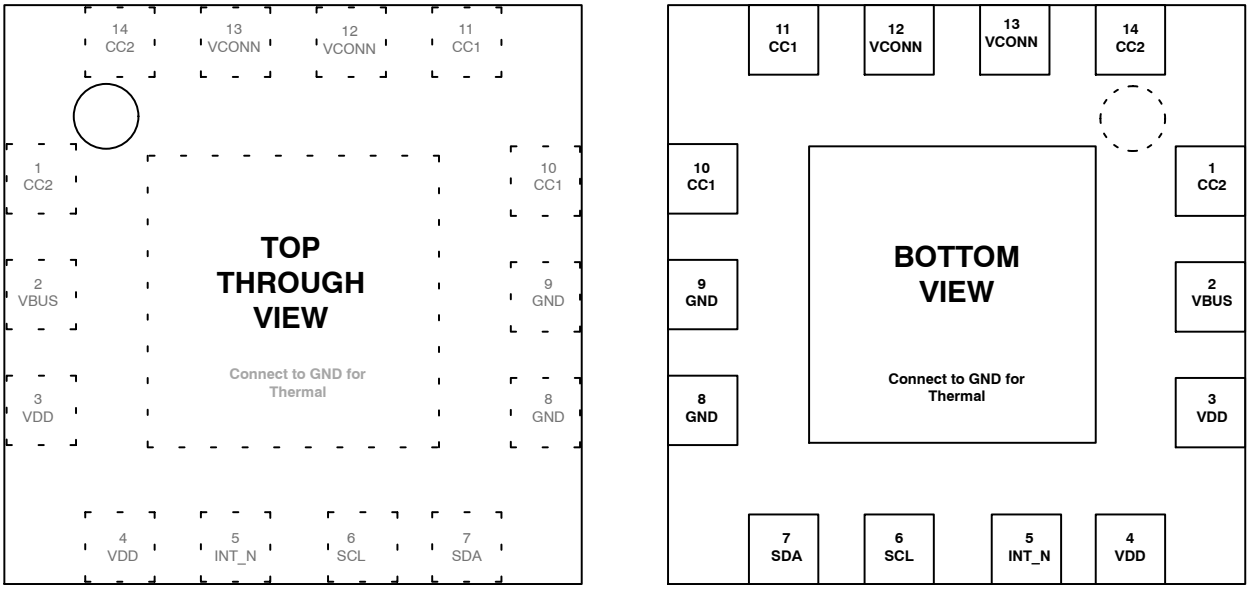


Figure 5. FUSB302BMPX Pin Assignment (N/C = No Connect)

Table 3. PIN DESCRIPTION

Name	Type	Description
USB TYPE-C CONNECTOR INTERFACE		
CC1/CC2	I/O	Type-C connector Configuration Channel (CC) pins. Initially used to determine when an attach has occurred and what the orientation of the insertion is. Functionality after attach depends on mode of operation detected. Operating as a host: 1. Sets the allowable charging current for VBUS to be sensed by the attached device 2. Used to communicate with devices using USB BMC Power Delivery 3. Used to detect when a detach has occurred Operating as a device: 1. Indicates what the allowable sink current is from the attached host. Used to communicate with devices using USB BMC Power Delivery
GND	Ground	Ground
VBUS	Input	VBUS input pin for attach and detach detection when operating as an upstream facing port (Device). Expected to be an OVP protected input.
POWER INTERFACE		
VDD	Power	Input supply voltage.
VCONN	Power Switch	Regulated input to be switched to correct CC pin as VCONN to power USB3.1 full-featured cables and other accessories.
SIGNAL INTERFACE		
SCL	Input	I^2C serial clock signal to be connected to the phone-based I^2C master.
SDA	Open-Drain I/O	I^2C serial data signal to be connected to the phone-based I^2C master
INT_N	Open-Drain Output	Active LOW open drain interrupt output used to prompt the processor to read the I^2C register bits

配置通道开关

FUSB302B集成了实施USB Type-C主机、器件或以下双重角色端口所需的控制和检测功能：

- 器件端口下拉(RD)
- 主机端口上拉(IP)
- 带OCP功能的VCONN电源开关，适用于全功能USB3.1电缆
- USB BMC电力输送物理层
- 配置通道(CC)阈值比较器。

每个CC引脚包含一个灵活的开关矩阵，可让主机软件控制要执行的Type-C端口类型。开关如Figure 6所示。

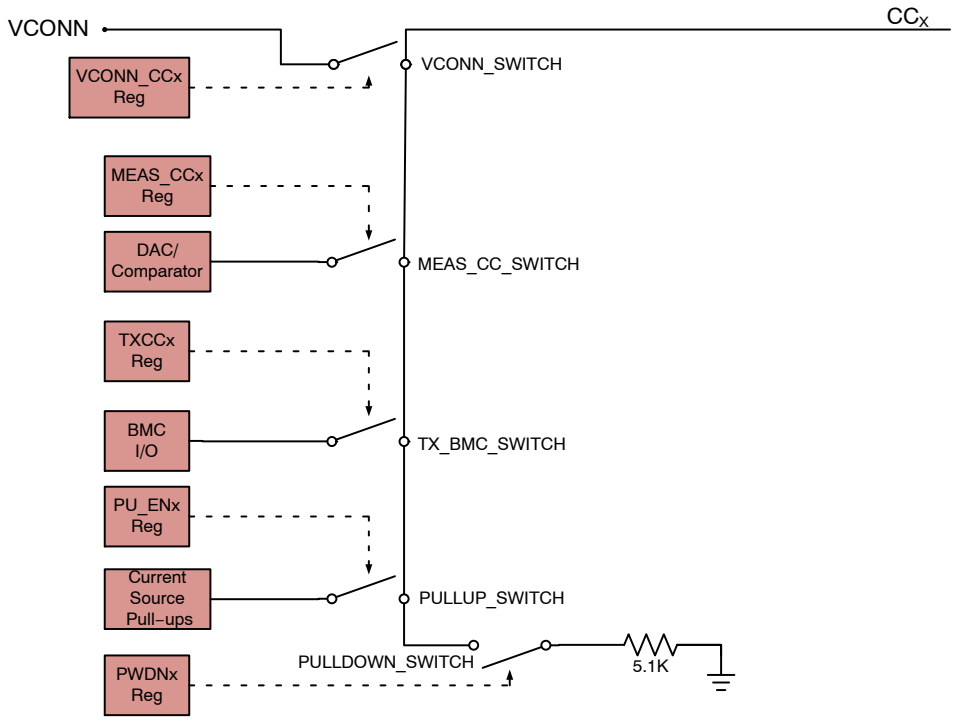


Figure 6. Configuration Channel Switch Functionality

TYPE-C检测

FUSB302B执行多个比较器和一个可编程的DAC，软件可用其确定CC和VBUS引脚的状态。此状态信息为处理器提供了确定连接、断开连接以及Type-C端口连接充电电流配置所需的全部信息。

FUSB302B配有三个固定阈值比较器，用于比较针对Type-C可检测的三种充电电流电平来匹配USB Type−C规格。状态变化时，这些比较器自动使BC_LVL和COMP发生中断。除固定阈值比较器外，主机软件还可使用6位DAC更准确地确定CC线状态。

FUSB302B还配有一个用于监控VBUS是否达到有效阈值的固定比较器。DAC可用于测量最高20 V的VBUS，让软件能够确认VBUS线已根据PD或其他通信方式发生预期变化，以更改充电电平。

通过自动切换器件进行检测

FUSB302B能够自动切换DRP。在自动切换时，FUSB302B可在内部控制PDWN1、PDWN2、PU_EN1、PU_EN2、MEAS_CC1和MEAS_CC2，并在SRC模式和SNK模式间切换固定DRP。或者，可仅以SRC或SNK模式运行，并持续轮询CC1和CC2。

Table 4. PROCESSOR CONFIGURES THE FUSB302B THROUGH I²C

I²C Registers/Bits	Value
TOGGLE	1
PWR	07H
HOST_CUR0	1
HOST_CUR1	0
MEAS_VBUS	0
VCONN_CC1	0
VCONN_CC2	0
Mask Register	0xFE
Maska Register	0xBF
Maskb Register (Except I_TOGDONE and I_BC_LVL Interrupt)	0x01
PWR[3:0]	0xBF

1. Once it has been determined what the role is of the FUSB302B, it returns I_TOGDONE and TOGSS1/2.
2. Processor then can perform a final manual check through I²C.

手动切换器件

FUSB302B能够手动切换DRP。在手动切换过程中，可使用处理器软件通过I²C和设置TOGGLE = 0来配置FUSB302B。

手动检测和配置器件

Type-C器件必须监控VBUS以确定其是否连接或断开连接。FUSB302B通过VBUSOK中断提供此信息。Type-C器件确定已连接了Type-C主机后，需要确定各CC引脚采用的端子类型。软件将确定是否根据BC_LVL和COMP中断和状态位来设置Ra或Rd端子。

另外，对于Rd端子，软件可通过读取BC_LVL状态位，进一步确定Type-C主机容许的充电电流。Table 5中进行了汇总。

切换功能

设置TOGGLE位(Control2寄存器)后，FUSB302B将在SRC模式和SNK模式间切换DRP。还可配置为仅SRC或仅SNK模式，并持续轮询CC1和CC2。此运行模式可通过设置TOGGLE = 1开启，且处理器应最初写入HOST_CUR1 = 0、HOST_CUR0 = 1 (对于默认电流)、VCONN_CC1 = VCONN_CC2 = 0、Mask Register = 0xFE、Maska register = 0xBF、Maskb register = 0x01、PWR = 0x01。处理器还应读取中断寄存器以将其清除，然后再设置TOGGLE位。

Table 5. DEVICE INTERRUPT SUMMARY

Status Type	Interrupt Status				Meaning
	BC_LVL[1:0]	COMP	COMP Setting	VBUSOK	
CC Detection	2'b00	NA	NA	1	vRA
	2'b01	NA	NA	1	vRd−Connect and vRd−USB
	2'b10	NA	NA	1	vRd−Connect and vRd−1.5
	2'b11	0	6'b11_0100 (2.05 V)	1	vRd−Connect and vRd−3.0
Attach	NA	NA	NA	1	Host Attached, VBUS Valid
Detach	NA	NA	NA	0	Host Detached, VBUS Invalid

Type-C器件(SNK)的高层级软件流程图如Figure 7所示。

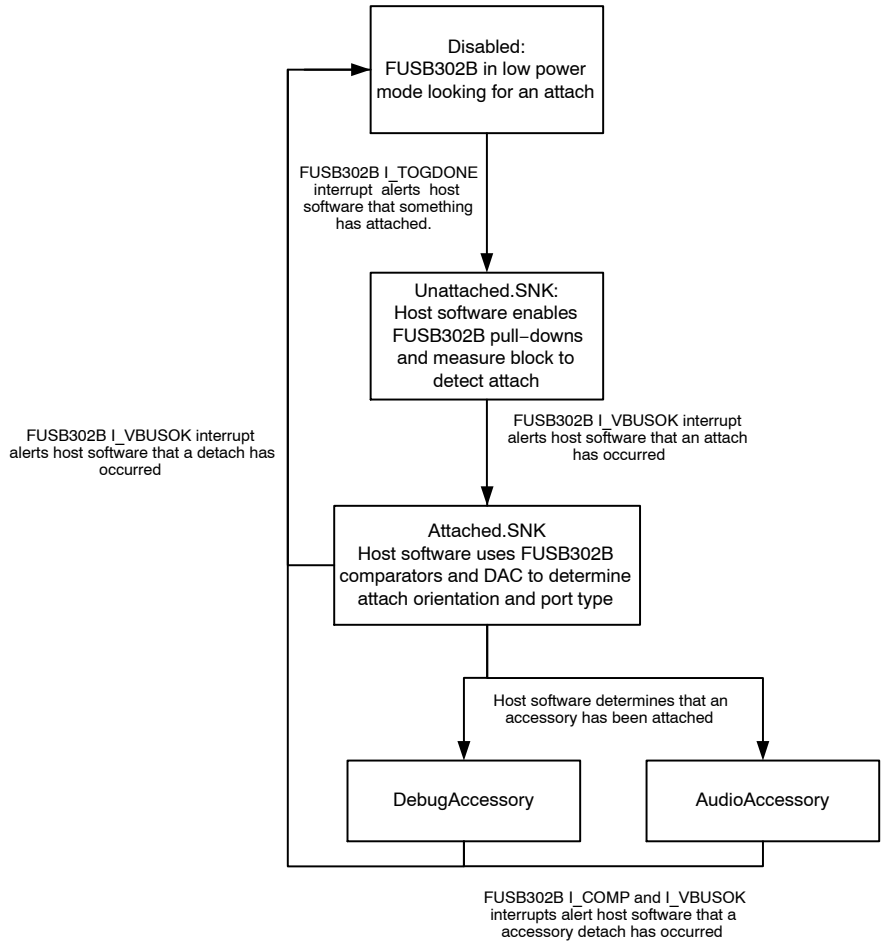


Figure 7. SNK Software Flow

手动检测和配置主机

当FUSB302B配置为Type-C主机时，软件可使用比较器和DAC的状态来确定连接或断开连接Type-C器件的时间，以及各CC引脚连接的端子类型。

FUSB302B允许主机软件通过HOST_CUR控制位更改端子的充电电流能力。如果在连接前更改了HOST_CUR位，连接器件后，FUSB302B将自动指示所设置的电流能力。如果在连接器件后更改电流能力，FUSB302B会立即将CC行更改为所设置的能力。

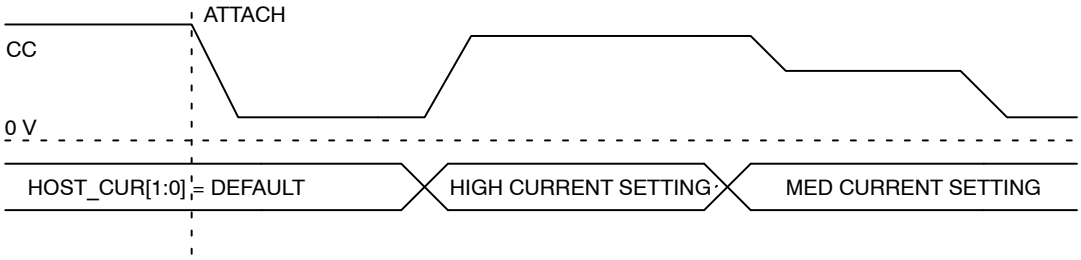


Figure 8. HOST_CUR Changed after Attach

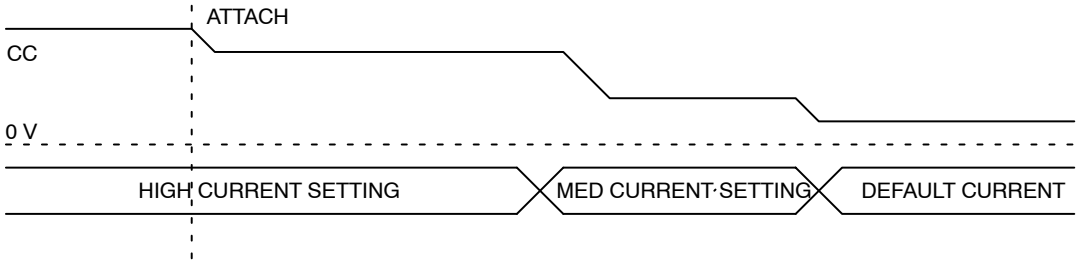


Figure 9. HOST_CUR Changed prior to Attach

Type-C规格简要说明了Type-C主机的不同连接和断开连接阈值，这些值基于供给各CC引脚的电流。根据HOST_CUR设置，软件将调节DAC比较器阈值，以匹配Type-C规格要求。BC_LVL比较器还可用作Ra检测流程的一部分。Table 6中进行了汇总。

Table 6. HOST INTERRUPT SUMMARY

Termination	HOST_CUR[1:0]	Interrupt Status			Attach/Detach
		BC_LVL[1:0]	COMP	COMP Setting	
Ra	2'b01	2'b00	NA	NA	NA
	2'b10	2'b01	0	6'b00_1010 (0.42 V)	
	2'b11	2'b10	0	6'b01_0011 (0.8 V)	
Rd	2'b01, 2'b10	NA	0	6'b10_0110 (1.6 V)	Attach
		NA	1	6'b10_0110 (1.6 V)	Detach
	2'b11	NA	0	6'b11_1110 (2.6 V)	Attach
		NA	1	6'b11_1110 (2.6 V)	Detach

Type−C主机(SRC)的高层级软件流程图如Figure 10中所示。

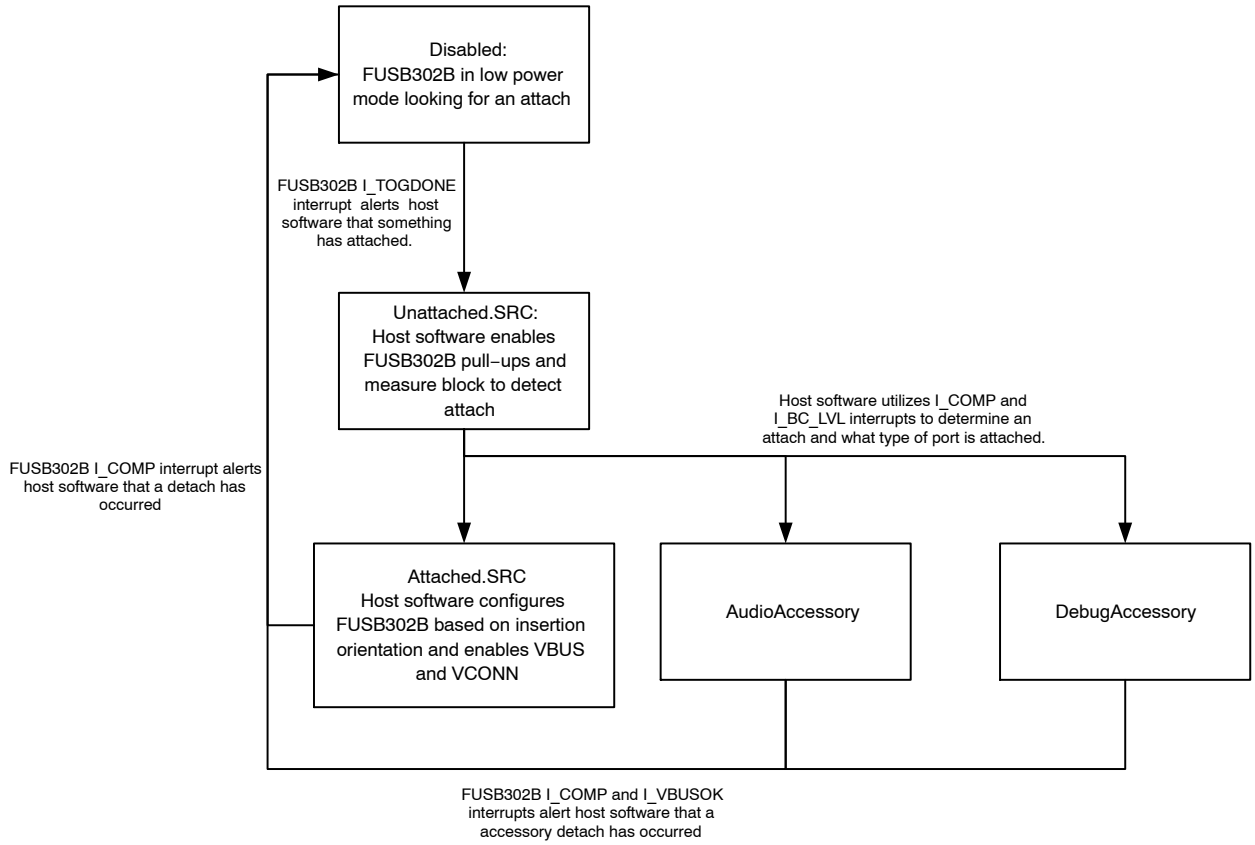


Figure 10. SRC Software Flow

手动检测和配置双重角色

Type-C规格允许根据所连接的端口类型，将端口设置为器件或主机。此功能类似于采用最新USB连接器的USB OTG端口，也被称为双重角色端口。FUSB302B可用于实现双重角色端口。Type-C双重角色端口在Type-C器件和Type-C主机模式间进行切换。主机软件控制FUSB302B在各状态下的切换时间和配置，如Figure 11所示。

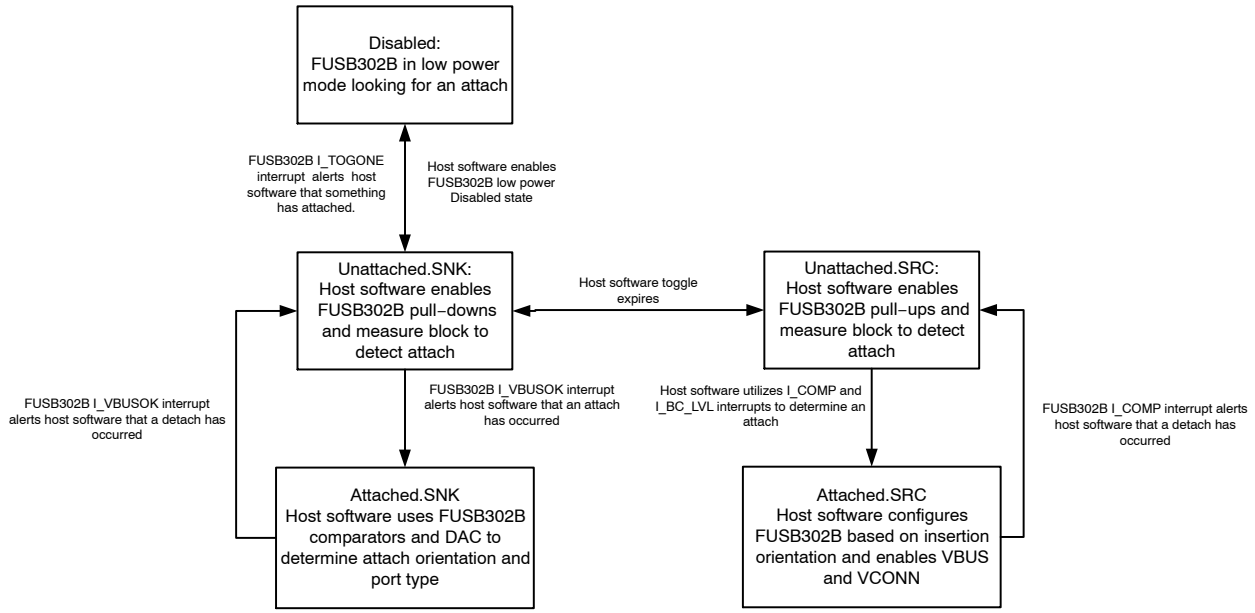


Figure 11. DRP Software Flow

BMC电力输送

Type-C连接器允许USB电力输送(PD)功能通过两个端口间连接的CC引脚进行通信。通信方法是借助BMC电力输送协议，但出于多种不同的原因，需要与Type-C连接器配合使用。下面简要介绍了可能的用途。

- 协商和控制充电功率级
- 可选接口包括MHL、Display Port
- 用于定制扩展坞或配件的厂商特定接口
- 双重角色端口的角色切换功能(在主机或器件模式间切换)
- 与USB3.1全功能电缆通信

FUSB302B集成了BMC PD瘦客户端，包括BMC 物理层和数据包FIFO (48字节用于发送，80字节用于接收)，可通过访问I^{2}C的主机软件发送和接收数据包。

FUSB302B允许主机软件通过写入和读取FIFO以及控制FUSB302B物理接口来实现USB BMC PD的所有功能。

FUSB302B使用令牌控制BMC PD数据包的传输。可通过写入这些令牌来传输FIFO，并控制数据包在CC引脚上的传输方式。令牌设计灵活，能够全面支持USB PD规格。FUSB302B还可通过令牌控制BMC发射器。通过特定令牌写入可启用或禁用发射器，通过将传输数据包所需的全部信息突发写入FIFO，能够更快地处理数据包。

CC引脚上收到有效的数据包后，FUSB302B接收器将储存接收FIFO中收到的数据和CRC。CC引脚上检测到活动时，BMC接收器将自动启用内部振荡器，并在收到数据包后，加载至FIFO。I_ACTIVITY和I_CRC_CHK中断将提醒主机软件收到了有效数据包。

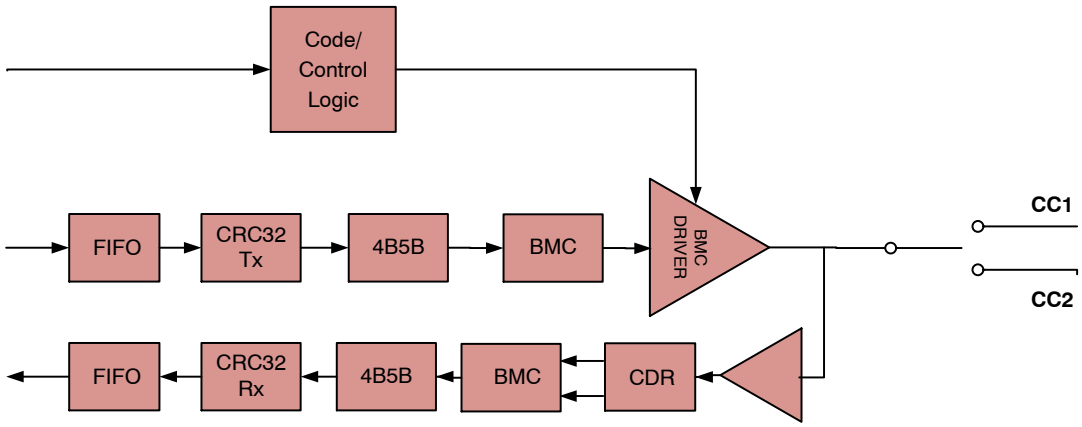


Figure 12. USB BMC Power Delivery Blocks

功率级测定

Type-C规格概述了功率级测定的优先顺序，涵盖了从基本USB2.0到最高层级USB PD的功率级。需要使用主机软件，根据FUSB302B检测、外部BC1.2检测以及任何USB电力输送模块通信的反馈，来执行USB Type-C规格中的充电电流优先顺序。

FUSB302B未集成BC1.2充电器检测功能，该功能一般在系统的USB收发器或USB充电器中提供。

通电、初始化和复位

首先通过VDD供电时，FUSB302B将复位，寄存器将初始化至默认值，如寄存器映射中所示。

可通过设置RESET寄存器中的SW_RES位，使用软件复位FUSB302B。

如果VDD未通电，则SRC会将FUSB302B识别为SNK。

PD自动接收GoodCRC

电力输送数据包需要针对所接收的每个数据包发送GoodCRC确认数据包，其中计算的CRC是正确值。此计算由FUSB302B完成，且如果CRC正常，则会触发I_CRC_CHK中断。如果设置AUTO_CRC (Switches1寄存器位)且AUTO_PRE=0，则FUSB302B将自动发送GoodCRC控制数据包，以减轻本机处理器的负载，从而快速响应所接收的数据包。如果GoodCRC所需超出SOP，则启用SOP*。

PD发送

为了以自动模式发送数据包，FUSB302B实现了部分PD协议层。

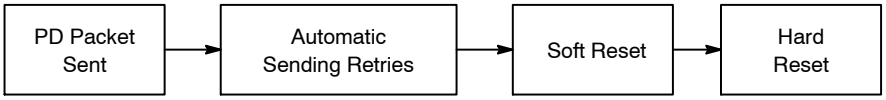


Figure 13.

PD自动重发

如果未收到GoodCRC数据包且设置了AUTO_RETRY，将会在t_{Retry}内重新发送处理器在TxFIFO中写入的相同消息，且重复NRETRY次。

PD发送软复位

如果所有重发结束后仍未收到正确的GoodCRC数据包，则会触发I_RETRYFAIL中断，如果设置了AUTO_SOFT_RESET，将会创建软复位数据包(MessageID设为0，且处理器在处理I_RETRYFAIL后会立即将真MessageIDCounter设为0)。

如果在收到GoodCRC控制数据包且MessageID=0的情况下成功发送软复位，则会出现I_TXSENT中断。

如果不是，且CRCReceiveTimer过期($t_{Receive}$最大值为1.1 ms)时未收到GoodCRC确认数据包，则会将此软复位数据包重发NRETRIES次(对于所有重试，MessageID始终为0)。如果所有重发操作失败，则会触发I_SOFTFAIL中断。

PD发送硬复位

如果所有软复位数据包重发操作均失败且设置了AUTO_HARD_RESET，则会通过在TxFIFO中加载RESET1、RESET1、RESET1、RESET2并发送硬复位，来发送复位命令集。请注意，由于未应用典型重试机制，仅会发送一个硬复位。如果处理器的策略引擎固件未收到所需的相应，则会负责重发硬复位。

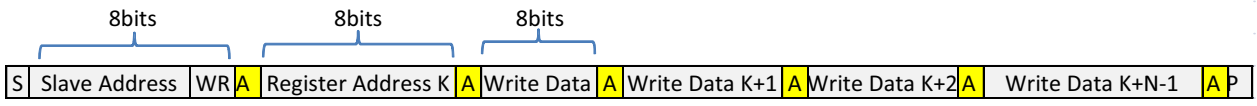
使用BIST (内建自测试)测试数据来刷新Rx−FIFO

在PD合规性测试期间，使用BIST测试数据包测试PD接口的物理层，例如，频率推导、幅值测量等。一个BIST测试数据包有7个数据对象(28字节数据)、标头和CRC，但消息ID不变，数据包应当被忽略，不用于PD策略引擎。在每一个数据包发送后，PD协议层都需要发回一条GoodCRC消息。BIST数据可从测试器连续送达，这可能导致FUSB302B Rx FIFO溢出，且PD协议层停止发送GoodCRC消息，除非FIFO已被快速读取或清除。FUSB302B在I²C寄存器中有一个特殊的寄存器，即[5]位地址0x09，设置该位后，接下来收到的所有数据都将从RxFIFO自动刷新，且PD协议层将持续传回GoodCRC消息。BIST测试完成后，测试器将发送HardReset，而对于HardReset，处理器必须重新写入该位以禁用。此外，如果该位可以随时取消选择，则传入的数据包必须由协议层和政策引擎进行管理。

I²C接口

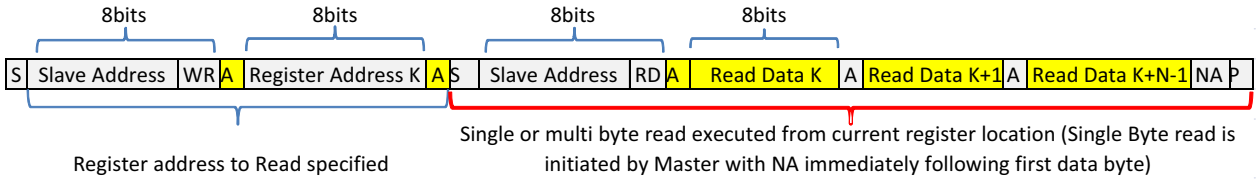
FUSB302B集成了完整的I²C从机控制器。I²C从机完全符合I²C规格版本6的要求。此模块专门设计用于运行高达1 MHz SCL的增强快速模式流量。

TOGGLE (切换)功能可在实现非常低功耗的运行和慢时钟，因此可能不完全符合1 MHz运行要求。关于I²C写入与读取序列示例，请分别参见Figure 14和Figure 15。



Note: Single Byte read is initiated by Master with P immediately following first data byte

Figure 14. I²C Write Example



Note: If Register is not specified Master will begin read from current register. In this case only sequence showing in Red bracket is needed

	From Master to Slave	**S**	Start Condition	**NA**	NOT Acknowledge (SDA High)	**RD**	Read =1
	From Slave to Master	**A**	Acknowledge (SDA Low)	**WR**	Write=0	**P**	Stop Condition

Figure 15. I²C Read Example

Table 7. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min	Max	Unit
V_{VDD}	Supply Voltage from V_{DD}	−0.5	6.0	V
V_{CC_HDDRP}	CC pins when configured as Host, Device or Dual Role Port	−0.5	6.0	V
V_{VBUS}	VBUS Supply Voltage	−0.5	28.0	V
$T_{STORAGE}$	Storage Temperature Range	−65	+150	°C
T_J	Maximum Junction Temperature	−	+150	°C
T_L	Lead Temperature (Soldering, 10 Seconds)	−	+260	°C
ESD	Human Body Model, ANSI/ESDA/JEDEC JS−001−2012	4	−	kV
	Charged Device Model, JEDEC JESD22−C101	1	−	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
(参考译文)
如果电压超过最大额定值表中列出的值范围，器件可能会损坏。如果超过任何这些限值，将无法保证器件功能，可能会导致器件损坏，影响可靠性。

Table 8. RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V_{VBUS}	VBUS Supply Voltage	4.0	5.0	21.0	V
V_{VDD}	VDD Supply Voltage	2.7 (Note 3)	3.3	5.5	V
V_{VCONN}	VCONN Supply Voltage	2.7	−	5.5	V
I_{VCONN}	VCONN Supply Current	−	−	560	mA
T_A	Operating Temperature	−40	−	+85	°C
T_A	Operating Temperature (Note 11)	−40	−	+105	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.
(参考译文)
高于推荐工作范围表格中所列电压时，不保证能够正常运行。长时间在推荐工作范围表格中规定范围以外的电压下运行，可能会影响器件的可靠性。

3. This is for functional operation only and not the lowest limit for all subsequent electrical specifications below. All electrical parameters have a minimum of 3.0 V operation.

DC和瞬态特性

除非另有说明，否则所有典型值都在T_A = 25°C条件下测得。

Table 9. BASEBAND PD

Symbol	Parameter	T_A = −40 to +85°C T_A = −40 to +105°C (Note 11) T_J = −40 to +125°C			Unit
		Min	Typ	Max	
UI	Unit Interval	3.03	–	3.70	μs
TRANSMITTER					
zDriver	Transmitter Output Impedance	33	–	75	Ω
$t_{EndDriveBMC}$	Time to Cease Driving the Line after the end of the last bit of the Frame	–	–	23	μs
$t_{HoldLowBMC}$	Time to Cease Driving the Line after the final High-to-Low Transition	1	–	–	μs
V_{OH}	Logic High Voltage	1.05	–	1.20	V
V_{OL}	Logic Low Voltage	0	–	75	mV
$t_{StartDrive}$	Time before the start of the first bit of the preamble when the transmitter shall start driving the line	−1	–	1	μs
t_{RISE_TX}	Rise Time	300	–	–	ns
t_{FALL_TX}	Fall Time	300	–	–	ns
RECEIVER					
cReceiver	Receiver Capacitance when Driver isn't Turned On	–	50	–	pF
zBmcRx	Receiver Input Impedance	1	–	–	MΩ
tRxFilter	Rx Bandwidth Limiting Filter (Note 4)	100	–	–	ns

4. Guaranteed by Characterization and/or Design. Not production tested.

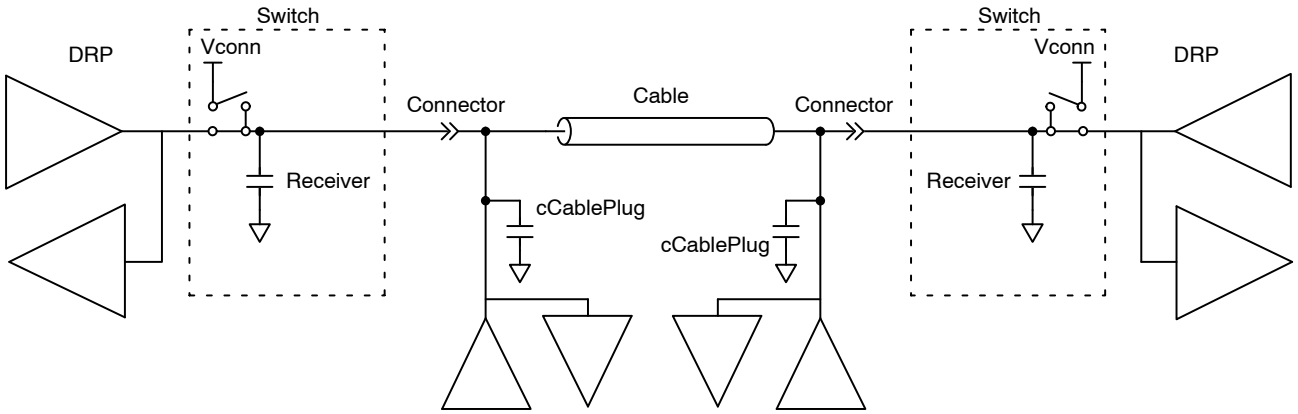


Figure 16. Transmitter Test Load

Table 10. TYPE-C CC SWITCH

Symbol	Parameter	T_A = −40 to +85°C T_A = −40 to +105°C (Note 11) T_J = −40 to +125°C			Unit
		Min	Typ	Max	
R_{SW_CCx}	R_{DSON} for SW1_CC1 and SW1_CC2, VCONN to CC1 & CC2	–	0.4	1.2	Ω
I_{SW_CCX}	Over-Current Protection (OCP) limit at which VCONN switch shuts off over the entire VCONN voltage range (OCPreg = 0Fh)	600	800	1000	mA
tSoftStart	Time taken for the VCONN switch to turn on during which Over-Current Protection is disabled	–	1.5	–	ms
I_{80_CCX}	SRC 80 μA CC current (Default) HOST_CUR1 = 0, HOST_CUR0 = 1	64	80	96	μA
I_{180_CCX}	SRC 180 μA CC Current (1.5 A) HOST_CUR1 = 1, HOST_CUR0 = 0	166	180	194	μA
I_{330_CCX}	SRC 330 μA CC Current (3 A) HOST_CUR1 = 1, HOST_CUR0 = 1	304	330	356	μA
V_{UFPDB}	SNK Pull-down Voltage in Dead Battery under all Pull-up SRC Loads	–	–	2.18	V
R_{DEVICE}	Device Pull-down Resistance (Note 5)	4.6	5.1	5.6	kΩ
zOPEN	CC Resistance for Disabled State	126	–	–	kΩ
$WAKE_{low}$	Wake threshold for CC pin SRC or SNK LOW value. Assumes bandgap and wake circuit turned on ie PWR[0] = 1	–	0.25	–	V
$WAKE_{high}$	Wake threshold for CC pin SRC or SNK HIGH value. Assumes bandgap and wake circuit turned on ie PWR[0] = 1	–	1.45	–	V
vBC_LVLhys	Hysteresis on the Ra and Rd Comparators (Note 7)	–	20	–	mV
vBC_LVL	CC Pin Thresholds, Assumes PWR = 4'h7 BC = 2'b00 BC = 2'b01 BC = 2'b10	 0.15 0.61 1.16	 0.20 0.66 1.23	 0.25 0.70 1.31	V
vMDACstepCC	Measure block MDAC step size for each code in MDAC[5:0] register	–	42	–	mV
vMDACstepVBUS	Measure block MDAC step size for each code in MDAC[5:0] register for VBUS measurement	–	420	–	mV
vVBUSthr	VBUS threshold at which I_VBUSOK interrupt is triggered. Assumes measure block on ie PWR[2] = 1	–	–	4.0	V
tTOG1	When TOGGLE = 1, time at which internal versions of PU_EN1 = PU_EN2 = 0 and PWDN1 = PDWN2 = 1 selected to present externally as a SNK in the DRP toggle	30	45	60	ms
tTOG2	When TOGGLE = 1, time at which internal versions of PU_EN1 = 1 or PU_EN2 = 1 and PWDN1 = PDWN2 = 0 selected to present externally as a SRC in the DRP toggle	20	30	40	ms
tDIS	Disable time after a full toggle (tTOG1 + tTOG2) cycle so as to save power TOG_SAVE_PWR2:1 = 00 TOG_SAVE_PWR2:1 = 01 TOG_SAVE_PWR2:1 = 10 TOG_SAVE_PWR2:1 = 11	 – – – –	 0 40 80 160	 – – – –	ms
Tshut	Temp. for Vconn Switch Off	–	145	–	°C
Thys	Temp. Hysteresis for Vconn Switch Turn On	–	10	–	°C

5. R_{DEVICE} minimum and maximum specifications are only guaranteed when power is applied.

Table 11. CURRENT CONSUMPTION

Symbol	Parameter	V_{DD} (V)	Conditions	T_A = −40 to +85°C T_A = −40 to +105°C (Note 11) T_J = −40 to +125°C			Unit
				Min	Typ	Max	
Idisable	Disabled Current	3.0 to 5.5	Nothing Attached, No I^2C Transactions	–	0.37	5.0	μA
Idisable	Disabled Current (Note 11)	3.0 to 5.5	Nothing Attached, No I^2C Transactions	–	0.37	8.5	μA
Itog	Unattached (standby) Toggle Current	3.0 to 5.5	Nothing attached, TOGGLE = 1, PWR[3:0] = 1h, WAKE_EN = 0, TOG_SAVE_PWR2:1 = 01	–	25	40	μA
Ipd_stby_meas	BMC PD Standby Current	3.0 to 5.5	Device Attached, BMC PD Active But Not Sending or Receiving Anything, PWR[3:0] = 7h	–	40	–	μA

Table 12. USB PD SPECIFIC PARAMETERS

Symbol	Parameter	T_A = −40 to +85°C T_A = −40 to +105°C (Note 11) T_J = −40 to +125°C			Unit
		Min	Typ	Max	
tHardReset	If a Soft Reset message fails, a Hard Reset is sent after tHardReset of CRCReceiveTimer expiring	–	–	5	ms
tHardReset Complete	If the FUSB302B cannot send a Hard Reset within tHardResetComplete time because of a busy line, then a I_HARDFAIL interrupt is triggered	–	–	5	ms
tReceive	This is the value for which the CRCReceiveTimer expires. The CRCReceiveTimer is started upon the last bit of the EOP of the transmitted packet	0.9	–	1.1	ms
tRetry	Once the CRCReceiveTimer expires, a retry packet has to be sent out within tRetry time. This time is hard to separate externally from tReceive since they both happen sequentially with no visible difference in the CC output	–	–	75	μs
tSoftReset	If a GoodCRC packet is not received within tReceive for NRETRIES then a Soft Reset packet is sent within tSoftReset time.	–	–	5	ms
tTransmit	From receiving a packet, we have to send a GoodCRC in response within tTransmit time. It is measured from the last bit of the EOP of the received packet to the first bit sent of the preamble of the GoodCRC packet	–	–	195	μs

Table 13. IO SPECIFICATIONS

Symbol	Parameter	V_{DD} (V)	Conditions	T_A = −40 to +85°C T_A = −40 to +105°C (Note 11) T_J = −40 to +125°C			Unit
				Min	Typ	Max	
HOST INTERFACE PINS (INT_N)							
V_{OLINTN}	Output Low Voltage	3.0 to 5.5	I_{OL} = 4 mA	–	–	0.4	V
T_{INT_Mask}	Time from global interrupt mask bit cleared to when INT_N goes LOW	3.0 to 5.5		50	–	–	μs
I^2C INTERFACE PINS – STANDARD, FAST, OR FAST MODE PLUS SPEED MODE (SDA, SCL) (Note 6)							
V_{ILI2C}	Low-Level Input Voltage	3.0 to 5.5		–	–	0.51	V
V_{IHI2C}	High-Level Input Voltage	3.0 to 5.5		1.32	–	–	V

Table 13. IO SPECIFICATIONS

Symbol	Parameter	V_{DD} (V)	Conditions	T_A = −40 to +85°C T_A = −40 to +105°C (Note 11) T_J = −40 to +125°C			Unit
				Min	Typ	Max	
I²C INTERFACE PINS – STANDARD, FAST, OR FAST MODE PLUS SPEED MODE (SDA, SCL) (Note 6)							
V_{HYS}	Hysteresis of Schmitt Trigger Inputs	3.0 to 5.5		94	–	–	mV
I_{I2C}	Input Current of SDA and SCL Pins	3.0 to 5.5	Input Voltage 0.26 V to 2.0 V	−10	–	10	μA
I_{CCTI2C}	VDD Current when SDA or SCL is HIGH	3.0 to 5.5	Input Voltage 1.8 V	−10	–	10	μA
V_{OLSDA}	Low-Level Output Voltage (Open-Drain)	3.0 to 5.5	I_{OL} = 2 mA	0	–	0.35	V
I_{OLSDA}	Low-Level Output Current (Open-Drain)	3.0 to 5.5	V_{OLSDA} = 0.4 V	20	–	–	mA
C_I	Capacitance for Each I/O Pin (Note 7)	3.0 to 5.5		–	5	–	pF

6. I²C pull up voltage is required to be between 1.71 V and V_{DD}.

Table 14. I²C SPECIFICATIONS FAST MODE PLUS I²C SPECIFICATIONS

Symbol	Parameter	Fast Mode Plus		Unit
		Min	Max	
f_{SCL}	I2C_SCL Clock Frequency	0	1000	kHz
$t_{HD;STA}$	Hold Time (Repeated) START Condition	0.26	–	μs
t_{LOW}	Low Period of I2C_SCL Clock	0.5	–	μs
t_{HIGH}	High Period of I2C_SCL Clock	0.26	–	μs
$t_{SU;STA}$	Set-up Time for Repeated START Condition	0.26	–	μs
$t_{HD;DAT}$	Data Hold Time	0	–	μs
$t_{SU;DAT}$	Data Set-up Time	50	–	ns
t_r	Rise Time of I2C_SDA and I2C_SCL Signals (Note 7)	–	120	ns
t_f	Fall Time of I2C_SDA and I2C_SCL Signals (Note 7)	6	120	ns
$t_{SU;STO}$	Set−up Time for STOP Condition	0.26	–	μs
t_{BUF}	Bus-Free Time between STOP and START Conditions (Note 7)	0.5	–	μs
t_{SP}	Pulse Width of Spikes that Must Be Suppressed by the Input Filter	0	50	ns
C_b	Capacitive Load for each Bus Line (Note 7)	–	550	pF
t_{VD-DAT}	Data Valid Time for Data from SCL LOW to SDA HIGH or LOW Output (Note 7)	0	0.45	μs
t_{VD-ACK}	Data Valid Time for acknowledge from SCL LOW to SDA HIGH or LOW Output (Note 7)	0	0.45	μs
V_{nL}	Noise Margin at the LOW Level (Note 7)	0.2	–	V
V_{nH}	Noise Margin at the HIGH Level (Note 7)	0.4	–	V

7. Guaranteed by Characterization and/or Design. Not production tested.

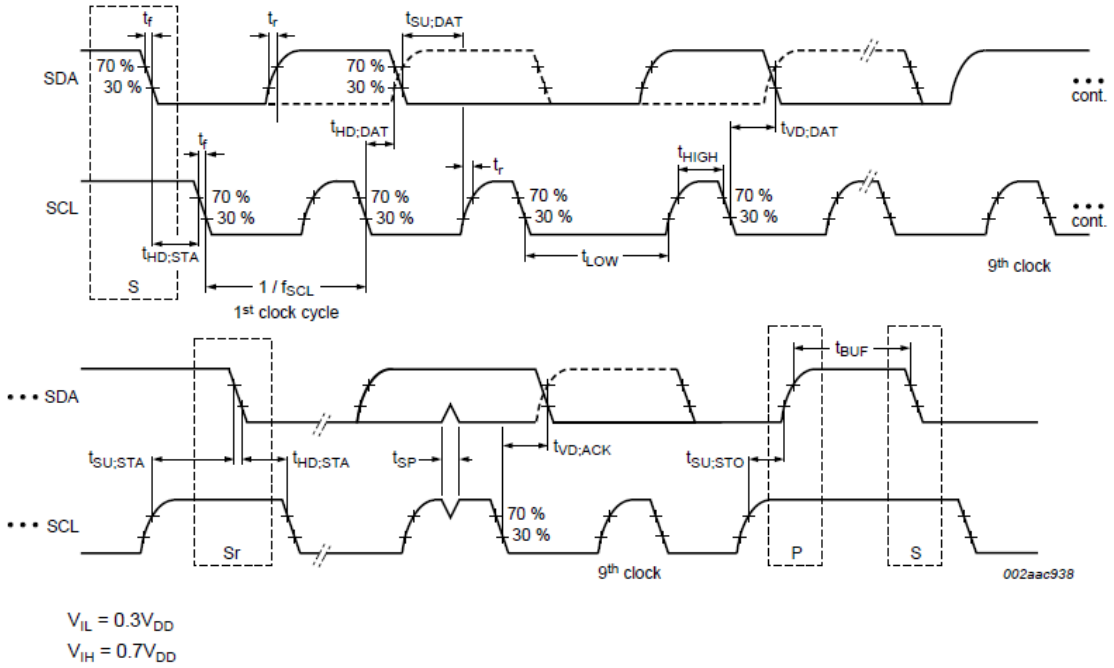


Figure 17. Definition of Timing for Full-Speed Mode Devices on the I²C Bus

Table 15. I²C SLAVE ADDRESS

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FUSB302BUCX, FUSB302BMPX, FUSB302BVMPX	0	1	0	0	0	1	0	R/W
FUSB302B01MPX	0	1	0	0	0	1	1	R/W
FUSB302B10MPX	0	1	0	0	1	0	0	R/W
FUSB302B11MPX	0	1	0	0	1	0	1	R/W

Table 16. REGISTER DEFINITIONS (Notes 8 and 9)

Address	Register Name	Type	Reg Value	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x01	Device ID	R	9X	Version ID[3:0]				Product ID[1:0]		Revision ID[1:0]	
0x02	Switches0	R/W	3	PU_EN2	PU_EN1	VCONN_CC2	VCONN_CC1	MEAS_CC2	MEAS_CC1	PDWN2	PDWN1
0x03	Switches1	R/W	20	POWER ROLE	SPEC REV1	SPEC REV0	DATA ROLE		AUTO_CRC	TXCC2	TXCC1
0x04	Measure	R/W	31		MEAS_VBUS	MDAC5	MDAC4	MDAC3	MDAC2	MDAC1	MDAC0
0x05	Slice	R/W	60	SDAC_HYS1	SDAC_HYS2	SDAC5	SDAC4	SDAC3	SDAC2	SDAC1	SDAC0
0x06	Control0	R/W/C	24		TX_FLUSH	INT_MASK		HOST_CUR1	HOST_CUR0	AUTO_PRE	TX_START
0x07	Control1	R/W/C	0		ENSOP 2DB	ENSOP 1DB	BIST_MODE2		RX_FLUSH	ENSOP2	ENSOP1
0x08	Control2	R/W	2	TOG_SAVE_PWR2	TOG_SAVE_PWR1	TOG_RD_ONLY		WAKE_EN	MODE[1:0]		TOGGLE
0x09	Control3	R/W	6		SEND_HARD_ RESET	BIST_TMODE	AUTO_HARD RESET	AUTO_ SOFTRESET	N_RETRIES[1:0]		AUTO_RETRY

Table 16. REGISTER DEFINITIONS (Notes 8 and 9)

Address	Register Name	Type	Reg Value	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x0A	Mask1	R/W	0	M_VBUSOK	M_ACTIVITY	M_COMP_CHNG	M_CRC_CHK	M_ALERT	M_WAKE	M_COLLISION	M_BC_LVL
0x0B	Power	R/W	1					PWR3	PWR2	PWR1	PWR0
0x0C	Reset	W/C	0							PD_RESET	SW_RES
0x0D	OCPreg	R/W	0F					OCP_RANGE	OCP_CUR2	OCP_CUR1	OCP_CUR0
0x0E	Maska	R/W	0	M_OCP_TEMP	M_TOGDONE	M_SOFTFAIL	M_RETRYFAIL	M_HARDSENT	M_TXSENT	M_SOFTRST	M_HARDRST
0x0F	Maskb	R/W	0								M_GCRCSENT
0x10	Control4	R/W	0								TOG_EXIT_AUD
0x3C	Status0a	R	0			SOFTFAIL	RETRYFAIL	POWER3	POWER2	SOFTRST	HARDRST
0x3D	Status1a	R	0			TOGSS3	TOGSS2	TOGSS1	RXSOP2DB	RXSOP1DB	RXSOP
0x3E	Interrupta	R/C	0	I_OCP_TEMP	I_TOGDONE	I_SOFTFAIL	I_RETRYFAIL	I_HARDSENT	I_TXSENT	I_SOFTRST	I_HARDRST
0x3F	Interruptb	R/C	0								I_GCRCSENT
0x40	Status0	R	0	VBUSOK	ACTIVITY	COMP	CRC_CHK	ALERT	WAKE	BC_LVL1	BC_LVL0
0x41	Status1	R	28	RXSOP2	RXSOP1	RX_EMPTY	RX_FULL	TX_EMPTY	TX_FULL	OVRTEMP	OCP
0x42	Interrupt	R/C	0	I_VBUSOK	I_ACTIVITY	I_COMP_CHNG	I_CRC_CHK	I_ALERT	I_WAKE	I_COLLISION	I_BC_LVL
0x43	FIFOs	R/W (Note 10)	0	Write to TX FIFO or read from RX FIFO repeatedly without address auto increment							

Type C Bits	USB PD Bits	General Bits

8. Do not use registers that are blank.
9. Values read from undefined register bits are not defined and invalid. Do not write to undefined registers.
10. FIFO register is serially read/written without auto address increment.
11. Automotive Part Only; FUSB302BVMPX

Table 17. DEVICE ID

(Address: 01h; Reset Value: 0x1001_XXXX; Type: Read)

Bit #	Name	R/W/C	Size (Bits)	Description
7:4	Version ID	R	4	Device version ID by Trim or etc. A_[Revision ID]: 1000 (e.g. A_revA) **B_[Revision ID]: 1001** C_[Revision ID]: 1010 etc
3:2	Product ID	R	2	“01”, “10” and “11” applies to MLP only: 00: FUSB302BMPX/FUSB302BVMPX(Default) & FUSB302BUCX 01: FUSB302B01MPX 10: FUSB302B10MPX 11: FUSB302B11MPX
1:0	Revision ID	R	2	Revision History of each version [Version ID]_revA: 00(e.g. revA) [Version ID]_revB: 01 (e.g. revB) [Version ID]_revC: 10 (e.g. revC) [Version ID]_revC: 11 (e.g. revD)

Table 18. SWITCHES0

(Address: 02h; Reset Value: 0x0000_0011; Type: Read/Write)

Bit #	Name	R/W/C	Size (Bits)	Description
7	PU_EN2	R/W	1	1: Apply host pull up current to CC2 pin
6	PU_EN1	R/W	1	1: Apply host pull up current to CC1 pin
5	VCONN_CC2	R/W	1	1: Turn on the VCONN current to CC2 pin
4	VCONN_CC1	R/W	1	1: Turn on the VCONN current to CC1 pin
3	MEAS_CC2	R/W	1	1: Use the measure block to monitor or measure the voltage on CC2
2	MEAS_CC1	R/W	1	1: Use the measure block to monitor or measure the voltage on CC1
1	PDWN2	R/W	1	1: Device pull down on CC2. 0: no pull down
0	PDWN1	R/W	1	1: Device pull down on CC1. 0: no pull down

Table 19. SWITCHES1

(Address: 03h; Reset Value: 0x0010_0000; Type: Read/Write)

Bit #	Name	R/W/C	Size (Bits)	Description
7	POWERROLE	R/W	1	Bit used for constructing the GoodCRC acknowledge packet. This bit corresponds to the Port Power Role bit in the message header if an SOP packet is received: 1: Source if SOP **0: Sink if SOP**
6:5	SPECREV1: SPECREV0	R/W	2	Bit used for constructing the GoodCRC acknowledge packet. These bits correspond to the Specification Revision bits in the message header: 00: Revision 1.0 **01: Revision 2.0** 10: Do Not Use 11: Do Not Use
4	DATAROLE	R/W	1	Bit used for constructing the GoodCRC acknowledge packet. This bit corresponds to the Port Data Role bit in the message header. For SOP: 1: SRC **0: SNK**
3	Reserved	N/A	1	Do Not Use
2	AUTO_CRC	R/W	1	1: Starts the transmitter automatically when a message with a good CRC is received and automatically sends a GoodCRC acknowledge packet back to the relevant SOP* **0: Feature disabled**
1	TXCC2	R/W	1	1: Enable BMC transmit driver on CC2 pin
0	TXCC1	R/W	1	1: Enable BMC transmit driver on CC1 pin

Table 20. MEASURE
(Address: 04h; ·Reset Value: 0x0011_0001; Type: Read/Write)

Bit #	Name	R/W/C	Size (Bits)	Description
7	Reserved	N/A	1	Do Not Use
6	MEAS_VBUS	R/W	1	0: MDAC/comparator measurement is controlled by MEAS_CC* bits 1: Measure VBUS with the MDAC/comparator. This requires MEAS_CC* bits to be 0
5:0	MDAC[5:0]	R/W	6	Measure Block DAC data input. LSB is equivalent to 42 mV of voltage which is compared to the measured CC voltage. The measured CC is selected by MEAS_CC2, or MEAS_CC1 bits. MDAC[5:0] / MEAS_VBUS = 0 / MEAS_VBUS = 1 / Unit 00_0000 / 0.042 / 0.420 / V 00_0001 / 0.084 / 0.840 / V 11_0000 / 2.058 / 20.58 / V 11_0011 / 2.184 / 21.84 / V 11_1110 / 2.646 / 26.46 / V 11_1111 / > 2.688 / 26.88 / V

Table 21. SLICE
(Address: 05h; Reset Value: 0x0110_0000; Type: Read/Write)

Bit #	Name	R/W/C	Size (Bits)	Description
7:6	SDAC_HYS[1:0]	R/W	2	Adds hysteresis where there are now two thresholds, the *lower threshold which is always the value programmed by SDAC[5:0]* and the higher threshold that is: 11: 255 mV hysteresis: higher threshold = (SDAC value + 20hex) 10: 170 mV hysteresis: higher threshold = (SDAC value + Ahex) 01: 85 mV hysteresis: higher threshold = (SDAC value + 5) 00: No hysteresis: higher threshold = SDAC value
5:0	SDAC[5:0]	R/W	6	BMC Slicer DAC data input. Allows for a programmable threshold so as to meet the BMC receive mask under all noise conditions.

Table 22. CONTROL0
(Address: 06h; Reset Value: 0x0010_0100; Type: (see column below))

Bit #	Name	R/W/C	Size (Bits)	Description
7	Reserved	N/A	1	Do Not Use
6	TX_FLUSH	W/C	1	1: Self clearing bit to flush the content of the transmit FIFO
5	INT_MASK	R/W	1	1: Mask all interrupts 0: Interrupts to host are enabled
4	Reserved	N/A	1	Do Not Use
3:2	HOST_CUR[1:0]	R/W	2	1: Controls the host pull up current enabled by PU_EN[2:1]: 00: No current 01: 80 μA – Default USB power 10: 180 μA – Medium Current Mode: 1.5 A 11: 330 μA – High Current Mode: 3 A
1	AUTO_PRE	R/W	1	1: Starts the transmitter automatically when a message with a good CRC is received. This allows the software to take as much as 300 μS to respond after the I_CRC_CHK interrupt is received. Before starting the transmitter, an internal timer waits for approximately 170 μS before executing the transmit start and preamble **0: Feature disabled**
0	TX_START	W/C	1	1: Start transmitter using the data in the transmit FIFO. Preamble is started first. During the preamble period the transmit data can start to be written to the transmit FIFO. Self clearing.

Table 23. CONTROL1
(Address: 07h; Reset Value: 0x0000_0000; Type: (see column below))

Bit #	Name	R/W/C	Size (Bits)	Description
7	Reserved	N/A	1	Do Not Use
6	ENSOP2DB	R/W	1	1: Enable SOP"_DEBUG (SOP double prime debug) packets **0: Ignore SOP"_DEBUG (SOP double prime debug) packets**
5	ENSOP1DB	R/W	1	1: Enable SOP'_DEBUG (SOP prime debug) packets **0: Ignore SOP'_DEBUG** (SOP prime debug) **packets**
4	BIST_MODE2	R/W	1	1: Sent BIST Mode 01s pattern for testing
3	Reserved	N/A	1	Do Not Use
2	RX_FLUSH	W/C	1	1: Self clearing bit to flush the content of the receive FIFO
1	ENSOP2	R/W	1	1: Enable SOP"(SOP double prime) packets **0: Ignore SOP"(SOP double prime) packets**
0	ENSOP1	R/W	1	1: Enable SOP'(SOP prime) packets **0: Ignore SOP'**(SOP prime) **packets**

Table 24. CONTROL2
(Address: 08h; Reset Value: 0x0000_0010; Type: (see column below))

Bit #	Name	R/W/C	Size (Bits)	Description
7:6	TOG_SAVE_PWR2: TOG_SAVE_PWR1	N/A	2	**00: Don't go into the DISABLE state after one cycle of toggle** 01: Wait between toggle cycles for t_{DIS} time of 40 ms 10: Wait between toggle cycles for t_{DIS} time of 80 ms 11: Wait between toggle cycles for t_{DIS} time of 160 ms
5	TOG_RD_ONLY	R/W	1	1: When TOGGLE=1 only Rd values will cause the TOGGLE state machine to stop toggling and trigger the I_TOGGLE interrupt 0: When TOGGLE=1, Rd and Ra values will cause the TOGGLE state machine to stop toggling
4	Reserved	N/A	1	Do Not Use
3	WAKE_EN	R/W	1	1: Enable Wake Detection functionality if the power state is correct **0: Disable Wake Detection functionality**
2:1	MODE	R/W	2	11: Enable SRC polling functionality if TOGGLE=1 10: Enable SNK polling functionality if TOGGLE=1 **01: Enable DRP polling functionality if TOGGLE=1** 00: Do Not Use
0	TOGGLE	R/W	1	1: Enable DRP, SNK or SRC Toggle autonomous functionality **0: Disable DRP, SNK and SRC Toggle functionality**

Table 25. CONTORL3
(Address: 09h; Reset Value: 0x0000_0110; Type: (see column below))

Bit #	Name	R/W/C	Size (Bits)	Description
7	Reserved	N/A	1	Do Not Use
6	SEND_HARD_RESET	W/C	1	1: Send a hard reset packet (highest priority) **0: Don't send a soft reset packet**
5	BIST_TMODE	R/W	1	1: BIST mode. Receive FIFO is cleared immediately after sending GoodCRC response 0: Normal operation, All packets are treated as usual
4	AUTO_HARDRESET	R/W	1	1: Enable automatic hard reset packet if soft reset fail **0: Disable automatic hard reset packet if soft reset fail**
3	AUTO_SOFTRESET	R/W	1	1: Enable automatic soft reset packet if retries fail **0: Disable automatic soft reset packet if retries fail**
2:1	N_RETRIES[1:0]	R/W	2	11: Three retries of packet (four total packets sent) 10: Two retries of packet (three total packets sent) 01: One retry of packet (two total packets sent) 00: No retries (similar to disabling auto retry)
0	AUTO_RETRY	R/W	1	1: Enable automatic packet retries if GoodCRC is not received **0: Disable automatic packet retries if GoodCRC not received**

Table 26. MASK
(Address: 0Ah; Reset Value: 0x0000_0000; Type: Read/Write)

Bit #	Name	R/W/C	Size (Bits)	Description
7	M_VBUSOK	R/W	1	1: Mask I_VBUSOK interrupt bit **0: Do not mask**
6	M_ACTIVITY	R/W	1	1: Mask interrupt for a transition in CC bus activity **0: Do not mask**
5	M_COMP_CHNG	R/W	1	1: Mask I_COMP_CHNG interrupt for change is the value of COMP, the measure comparator **0: Do not mask**
4	M_CRC_CHK	R/W	1	1: Mask interrupt from CRC_CHK bit **0: Do not mask**
3	M_ALERT	R/W	1	1: Mask the I_ALERT interrupt bit **0: Do not mask**
2	M_WAKE	R/W	1	1: Mask the I_WAKE interrupt bit 0: Do not mask
1	M_COLLISION	R/W	1	1: Mask the I_COLLISION interrupt bit **0: Do not mask**
0	M_BC_LVL	R/W	1	1: Mask a change in host requested current level **0: Do not mask**

Table 27. POWER
(Address: 0Bh; Reset Value: 0x0000_0001; Type: Read/Write)

Bit #	Name	R/W/C	Size (Bits)	Description
7:4	Reserved	N/A	4	Do Not Use
3:0	PWR[3:0]	R/W	4	Power enables: **PWR[0]: Bandgap and wake circuit** PWR[1]: Receiver powered and current references for Measure block PWR[2]: Measure block powered PWR[3]: Enable internal oscillator

Table 28. RESET
(Address: 0Ch; Reset Value: 0x0000_0000; Type: Write/Clear)

Bit #	Name	R/W/C	Size (Bits)	Description
7:2	Reserved	N/A	6	Do Not Use
1	PD_RESET	W/C	1	1: Reset just the PD logic for both the PD transmitter and receiver
0	SW_RES	W/C	1	1: Reset the FUSB302B including the I^2C registers to their default values

Table 29. OCPREG
(Address: 0Dh; Reset Value: 0x0000_1111; Type: Read/Write)

Bit #	Name	R/W/C	Size (Bits)	Description
7:4	Reserved	N/A	4	Do Not Use
3	OCP_RANGE	R/W	1	1: OCP range between 100−800 mA (max_range = 800 mA) 0: OCP range between 10−80 mA (max_range = 80 mA)
2:0	OCP_CUR2, OCP_CUR1, OCP_CUR0	R/W	3	111: max_range (see bit definition above for OCP_RANGE) 110: 7 × max_range / 8 101: 6 × max_range / 8 100: 5 × max_range / 8 011: 4 × max_range / 8 010: 3 × max_range / 8 001: 2 × max_range / 8 000: max_range / 8

Table 30. MASKA
(Address: 0Eh; Reset Value: 0x0000_0000; Type: Read/Write)

Bit #	Name	R/W/C	Size (Bits)	Description
7	M_OCP_TEMP	R/W	1	1: Mask the I_OCP_TEMP interrupt
6	M_TOGDONE	R/W	1	1: Mask the I_TOGDONE interrupt
5	M_SOFTFAIL	R/W	1	1: Mask the I_SOFTFAIL interrupt
4	M_RETRYFAIL	R/W	1	1: Mask the I_RETRYFAIL interrupt
3	M_HARDSENT	R/W	1	1: Mask the I_HARDSENT interrupt
2	M_TXSENT	R/W	1	1: Mask the I_TXSENT interrupt
1	M_SOFTRST	R/W	1	1: Mask the I_SOFTRST interrupt
0	M_HARDRST	R/W	1	1: Mask the I_HARDRST interrupt

Table 31. MASKB
(Address: 0Fh; Reset Value: 0x0000_0000; Type: Read/Write)

Bit #	Name	R/W/C	Size (Bits)	Description
7:1	Reserved	N/A	6	Do Not Use
0	M_GCRCSENT	R/W	1	1: Mask the I_GCRCSENT interrupt

Table 32. CONTROL4
(Address: 00h; Reset Value: 0x0000_0000; Type: Read/Write)

Bit #	Name	R/W/C	Size (Bits)	Description
7:1	Reserved	N/A	6	Do Not Use
0	TOG_EXIT_AUD	R/W	1	1: In auto Rd only Toggle mode, stop Toggle at Audio accessory (Ra on both CC)

Table 33. STATUS0A
(Address: 3Ch; Reset Value: 0x0000_0000; Type: Read)

Bit #	Name	R/W/C	Size (Bits)	Description
7:6	Reserved	N/A	2	Do Not Use
5	SOFTFAIL	R	1	1: All soft reset packets with retries have failed to get a GoodCRC acknowledge. This status is cleared when a START_TX, TXON or SEND_HARD_RESET is executed
4	RETRYFAIL	R	1	1: All packet retries have failed to get a GoodCRC acknowledge. This status is cleared when a START_TX, TXON or SEND_HARD_RESET is executed
3:2	POWER3:POWER2	R	2	Internal power state when logic internals needs to control the power state. POWER3 corresponds to PWR3 bit and POWER2 corresponds to PWR2 bit. The power state is the higher of both PWR[3:0] and {POWER3, POWER2, PWR[1:0]} so that if one is 03 and the other is F then the internal power state is F
1	SOFTRST	R	1	1: One of the packets received was a soft reset packet
0	HARDRST	R	1	1: Hard Reset PD ordered set has been received

Table 34. STATUS1A
(Address: 3Dh; Reset Value: 0x0000_0000; Type: Read)

Bit #	Name	R/W/C	Size (Bits)	Description
7:6	Reserved	N/A	2	Do Not Use
5:3	TOGSS3, TOGSS2, TOGSS1	R	3	000: Toggle logic running (processor has previously written TOGGLE=1) 001: Toggle functionality has settled to SRCon CC1 (STOP_SRC1 state) 010: Toggle functionality has settled to SRCon CC2 (STOP_SRC2 state) 101: Toggle functionality has settled to SNKon CC1 (STOP_SNK1 state) 110: Toggle functionality has settled to SNKon CC2 (STOP_SNK2 state) 111: Toggle functionality has detected AudioAccessory with vRa on both CC1 and CC2 (settles to STOP_SRC1 state) Otherwise: Not defined (do not interpret)
2	RXSOP2DB	R	1	1: Indicates the last packet placed in the RxFIFO is type SOP”_DEBUG (SOP double prime debug)
1	RXSOP1DB	R	1	1: Indicates the last packet placed in the RxFIFO is type SOP’_DEBUG (SOP prime debug)
0	RXSOP	R	1	1: Indicates the last packet placed in the RxFIFO is type SOP

Table 35. INTERRUPTA

(Address: 3Eh; Reset Value: 0x0000_0000; Type: Read/Clear)

Bit #	Name	R/W/C	Size (Bits)	Description
7	I_OCP_TEMP	R/C	1	1: Interrupt from either a OCP event on one of the VCONN switches or an over-temperature event
6	I_TOGDONE	R/C	1	1: Interrupt indicating the TOGGLE functionality was terminated because a device was detected
5	I_SOFTFAIL	R/C	1	1: Interrupt from automatic soft reset packets with retries have failed
4	I_RETRYFAIL	R/C	1	1: Interrupt from automatic packet retries have failed
3	I_HARDSENT	R/C	1	1: Interrupt from successfully sending a hard reset ordered set
2	I_TXSENT	R/C	1	1: Interrupt to alert that we sent a packet that was acknowledged with a GoodCRC response packet
1	I_SOFTRST	R/C	1	1: Received a soft reset packet
0	I_HARDRST	R/C	1	1: Received a hard reset ordered set

Table 36. INTERRUPTB

(Address: 3Fh; Reset Value: 0x0000_0000; Type: Read/Clear)

Bit #	Name	R/W/C	Size (Bits)	Description
7	Reserved	N/A	6	Do Not Use
0	I_GCRCSENT	R/C	1	1: Sent a GoodCRC acknowledge packet in response to an incoming packet that has the correct CRC value

Table 37. STATUS0
(Address: 40h; Reset Value: 0x0000_0000; Type: Read)

Bit #	Name	R/W/C	Size (Bits)	Description
7	VBUSOK	R	1	1: Interrupt occurs when VBUS transitions through vVBUSthr. This bit typically is used to recognize port partner during startup
6	ACTIVITY	R	1	1: Transitions are detected on the active CC* line. This bit goes high after a minimum of 3 CC transitions, and goes low with no Transitions **0: Inactive**
5	COMP	R	1	1: Measured CC* input is higher than reference level driven from the MDAC **0: Measured CC* input is lower than reference level driven from the MDAC**
4	CRC_CHK	R	1	1: Indicates the last received packet had the correct CRC. This bit remains set until the SOP of the next packet **0: Packet received for an enabled SOP* and CRC for the enabled packet received was incorrect**
3	ALERT	R	1	1: Alert software an error condition has occurred. An alert is caused by: TX_FULL: the transmit FIFO is full RX_FULL: the receive FIFO is full See **Status1** bits
2	WAKE	R	1	1: Voltage on CC indicated a device attempting to attach 0: WAKE either not enabled (WAKE_EN=0) or no device attached
1:0	BC_LVL[1:0]	R	2	Current voltage status of the measured CC pin interpreted as host current levels as follows: 00: < 200 mV 01: > 200 mV, < 660 mV 10: > 660 mV, < 1.23 V 11: > 1.23 V Note the software must measure these at an appropriate time, while there is no signaling activity on the selected CC line. BC_LVL is only defined when Measure block is on which is when register bits PWR[2]=1 and either MEAS_CC1=1 or MEAS_CC2=1

Table 38. STATUS1
(Address: 41h; Reset Value: 0x0010_1000; Type: Read)

Bit #	Name	R/W/C	Size (Bits)	Description
7	RXSOP2	R	1	1: Indicates the last packet placed in the RxFIFO is type SOP" (SOP double prime)
6	RXSOP1	R	1	1: Indicates the last packet placed in the RxFIFO is type SOP' (SOP prime)
5	RX_EMPTY	R	1	1: The receive FIFO is empty
4	RX_FULL	R	1	1: The receive FIFO is full
3	TX_EMPTY	R	1	1: The transmit FIFO is empty
2	TX_FULL	R	1	1: The transmit FIFO is full
1	OVRTEMP	R	1	1: Temperature of the device is too high
0	OCP	R	1	1: Indicates an over-current or short condition has occurred on the VCONN switch

Table 39. INTERRUPT
(Address: 42h; Reset Value: 0x0000_0000; Type: Read/Clear)

Bit #	Name	R/W/C	Size (Bits)	Description
7	I_VBUSOK	R/C	1	1: Interrupt occurs when VBUS transitions through 4.5 V. This bit typically is used to recognize port partner during startup
6	I_ACTIVITY	R/C	1	1: A change in the value of ACTIVITY of the CC bus has occurred
5	I_COMP_CHNG	R/C	1	1: A change in the value of COMP has occurred. Indicates selected CC line has tripped a threshold programmed into the MDAC
4	I_CRC_CHK	R/C	1	1: The value of CRC_CHK newly valid. I.e. The validity of the incoming packet has been checked
3	I_ALERT	R/C	1	1: Alert software an error condition has occurred. An alert is caused by: TX_FULL: the transmit FIFO is full RX_FULL: the receive FIFO is full See **Status1** bits
2	I_WAKE	R/C	1	1: Voltage on CC indicated a device attempting to attach. Software must then power up the clock and receiver blocks
1	I_COLLISION	R/C	1	1: When a transmit was attempted, activity was detected on the active CC line. Transmit is not done. The packet is received normally
0	I_BC_LVL	R/C	1	1: A change in host requested current level has occurred

Table 40. FIFOS
(Address: 43h; Reset Value: 0x0000_0000; Type: (see column below))

Bit #	Name	R/W/C	Size (Bits)	Description
7:0	TX/RX Token	Read or Write	8	Writing to this register writes a byte into the transmit FIFO. Reading from this register reads from the receive FIFO. Each byte is a coded token. Or a token followed by a fixed number of packed data byte (*see token coding in Table 41*)

软件模型

端口软件主要通过两种方式与端口芯片交互：

- I^2C寄存器
- 发送至FIFO寄存器或从FIFO寄存器接收的的8位数据令牌。
- 写入TxFIFO的所有保留位应当为0，且从RxFIFO读取的所有保留位应当被忽略。

传输数据令牌

传输数据令牌提供依次传输控制和传输逻辑数据。请注意，令牌代码及其等效的USB PD K-Code不相同。达到TX FIFO末尾时，将会一次性读取令牌。即，从TX FIFO读取下一个令牌之前，将会执行指定令牌操作。

令牌定义如下：

Table 41. TOKENS USED IN FIFO

Code	Name	Size (Bytes)	Description
101x−xxx1 (0xA1)	TXON	1	Alternative method for starting the transmitter with the TX−START bit. This is not a token written to the TxFIFO but a command much like TX_START but it is more convenient to write it while writing to the TxFIFO in one contiguous write operation. It is preferred that the TxFIFO is first written with data and then TXON or TX_START is executed. It is expected that A1h will be written for TXON not any other bits where x is non-zero such as B1h, BFh, etc
0x12	SOP1	1	When reaching the end of the FIFO causes a Sync−1 symbol to be transmitted
0x13	SOP2	1	When reaching the end of the FIFO causes a Sync−2 symbol to be transmitted
0x1B	SOP3	1	When reaching the end of the FIFO causes a Sync−3 symbol to be transmitted
0x15	RESET1	1	When reaching the end of the FIFO causes a RST−1 symbol to be transmitted
0x16	RESET2	1	When reaching the end of the FIFO causes a RST−2 symbol to be transmitted
0x80	PACKSYM	1+N	This data token must be immediately followed by a sequence of N packed data bytes. This token is defined by the 3 MSB's being set to 3'b100. The 5 LSB's are the number of packed bytes being sent. Note: N cannot be less than 2 since the minimum control packet has a header that is 2 bytes and N cannot be greater than 30 since the maximum data packet has 30 bytes (2 byte header + 7 data objects each having 4 bytes) Packed data bytes have two 4 bit data fields. The 4 LSB's are sent first, after 4b5b conversion etc in the chip
0xFF	JAM_CRC	1	Causes the CRC, calculated by the hardware, to be inserted into the transmit stream when this token reaches the end of the TX FIFO
0x14	EOP	1	Causes an EOP symbol to be sent when this token reaches the end of the TX FIFO
0xFE	TXOFF	1	Turn off the transmit driver. Typically the next symbol after EOP

接收数据令牌

接收数据令牌提供依次接收控制和接收逻辑数据。RxFIFO可接收与RxFIFO中字节数相同的数据包(80字节)。令牌定义如下：

Table 42. TOKENS USED IN RxFIFO

Code	Name	Size (Bytes)	Description
111b_bbbb	SOP	1	First byte of a received packet to indicate that the packet is an SOP packet ("b" is undefined and can be any bit)
110b_bbbb	SOP1	1	First byte of a received packet to indicate that the packet is an SOP' packet and occurs only if ENSOP1=1 ("b" is undefined and can be any bit)
101b_bbbb	SOP2	1	First byte of a received packet to indicate that the packet is an SOP" packet and occurs only if ENSOP2=1 ("b" is undefined and can be any bit)
100b_bbbb	SOP1DB	1	First byte of a received packet to indicate that the packet is an SOP'_DEBUG packet and occurs only if ENSOP1DB=1 ("b" is undefined and can be any bit)
011b_bbbb	SOP2DB	1	First byte of a received packet to indicate that the packet is an SOP"_DEBUG packet and occurs only if ENSOP2DB=1 ("b" is undefined and can be any bit)
010b_bbbb/ 001b_bbbb/ 000b_bbbb	Do Not Use	1	These can be used in future versions of this device and should not be relied on to be any special value. ("b" is undefined and can be any bit)

参考原理图

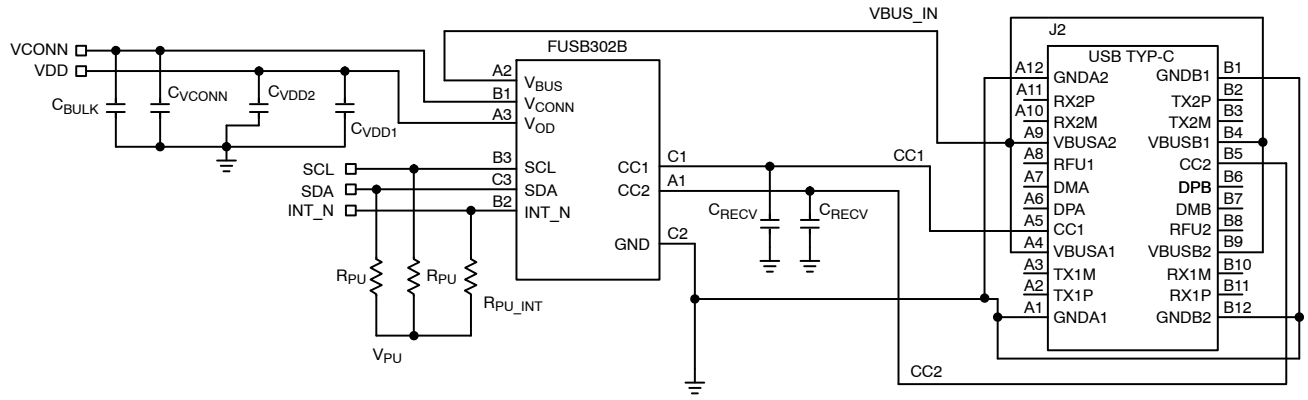


Figure 18. FUSB302/FUSB302B Reference Schematic Diagram

Table 43. RECOMMENDED COMPONENT VALUES FOR REFERENCE SCHEMATIC

Symbol	Parameter	Recommended Value			Unit
		Min	Typ	Max	
C_{RECV}	CC_X Receiver Capacitance	200	–	600	pF
C_{BULK}	VCONN Source Bulk Capacitance	10	–	220	μF
C_{VCONN}	VCONN Decoupling Capacitance	–	0.1	–	μF
C_{VDD1}	V_{DD} Decoupling Capacitance	–	0.1	–	μF
C_{VDD2}	V_{DD} Decoupling Capacitance	–	1.0	–	μF
R_{PU}	I^2C Pull-up Resistors	–	4.7	–	kΩ
R_{PU_INT}	INT_N Pull-up Resistor	1.0	4.7	–	kΩ
V_{PU}	I^2C Pull-up Voltage	1.71	–	V_{DD}	V

Table 44. PRODUCT-SPECIFIC DIMENSIONS

Product	D	E	X	Y
FUSB302BUCX	1.260 mm	1.215 mm	0.2075 mm	0.230 mm

下表列出了下页WLCSP封装图中的相关数据。

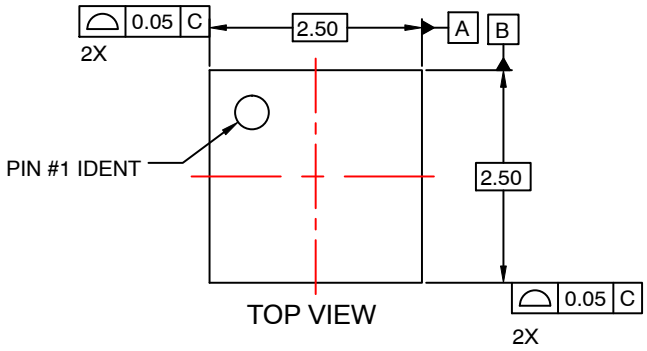
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

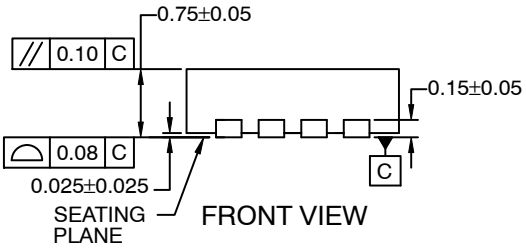
ON Semiconductor®

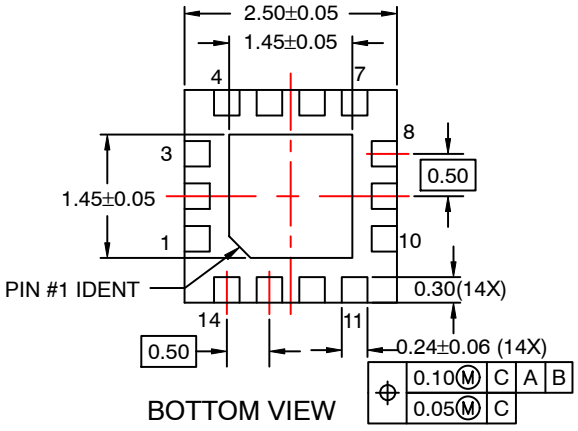
WQFN14 2.5x2.5, 0.5P
CASE 510BR
ISSUE O

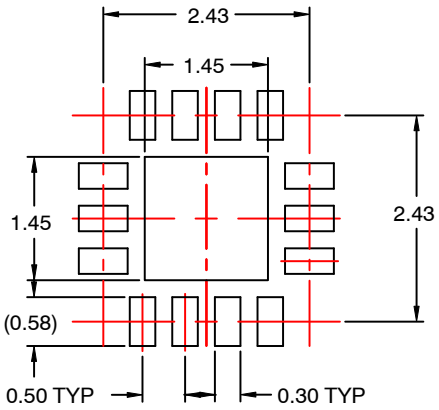
DATE 31 AUG 2016

SCALE 4:1









RECOMMENDED LAND PATTERN

NOTES:

A. NO JEDEC REGISTRATION.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.

D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.

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DESCRIPTION:	**WQFN14 2.5X2.5, 0.5P**	**PAGE 1 OF 1**

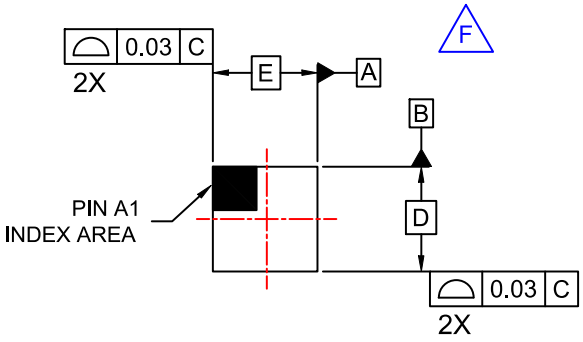
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

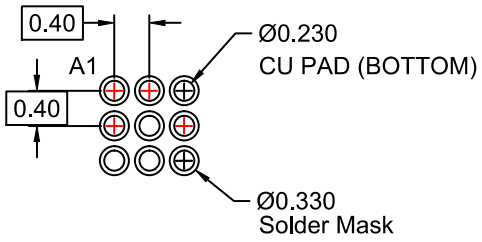
SCALE 5:1

WLCSP9 1.26x1.215x0.526
CASE 567TN
ISSUE O

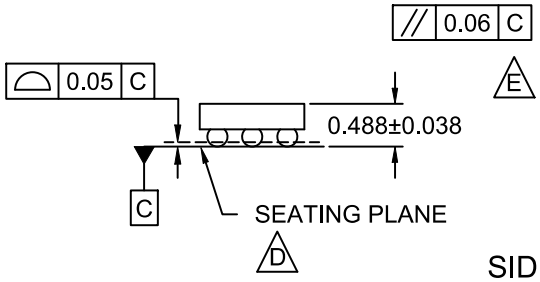
DATE 31 MAR 2017

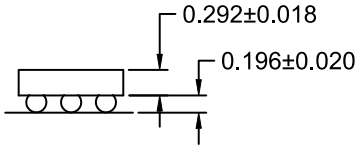


TOP VIEW

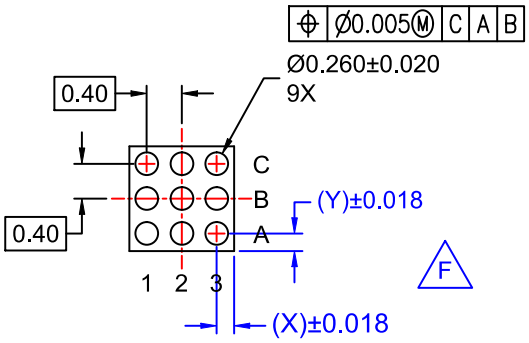


LAND PATTERN RECOMMENDATION
(NSMD PAD TYPE)





SIDE VIEWS



BOTTOM VIEW

NOTES:

A. NO JEDEC REGISTRATION APPLIES.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCE PER ASME Y14.5M, 2009.

D. DATUM C IS DEFINED BY THE SPHERICAL CROWNS OF THE BALLS.

E. PACKAGE NOMINAL HEIGHT IS 488 MICRONS ±38 MICRONS (450-526 MICRONS).

F. FOR DIMENSIONS D, E, X, AND Y SEE PRODUCT DATASHEET.

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