NCV8769

Ultra Low Iq 150 mA LDO Regulator with Reset and Early Warning

The NCV8769 is 150 mA LDO regulator with integrated reset and early warning functions dedicated for microprocessor applications. Its robustness allows NCV8769 to be used in severe automotive environments. Ultra low quiescent current as low as 25 μA typical for NCV8769 makes it suitable for applications permanently connected to battery requiring ultra low quiescent current with or without load. The NCV8769 contains protection functions as current limit, thermal shutdown and reverse output current protection.

Features

- Output Voltage Options: 5 V
- Output Voltage Accuracy: ±2%
- Output Current up to 150 mA
- Ultra Low Quiescent Current:
  - typ 25 μA for Adjustable Early Warning Threshold Option
- Very Low Dropout Voltage
- Microprocessor Compatible Control Functions:
  - Reset with Adjustable Power−on Delay
  - Early Warning
- Wide Input Voltage Operation Range: up to 40 V
- Protection Features:
  - Current Limitation
  - Thermal Shutdown
- These are Pb−Free Devices

Typical Applications

- Body Control Module
- Instruments and Clusters
- Occupant Protection and Comfort
- Powertrain

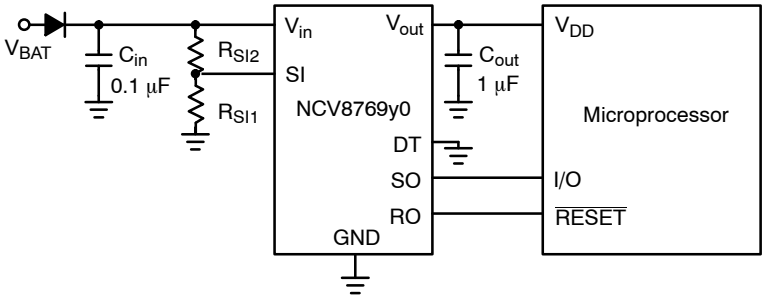

Figure 1. Application Circuit

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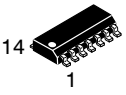
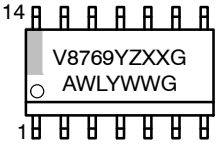
MARKING DIAGRAMS



SO−14
D SUFFIX
CASE 751A

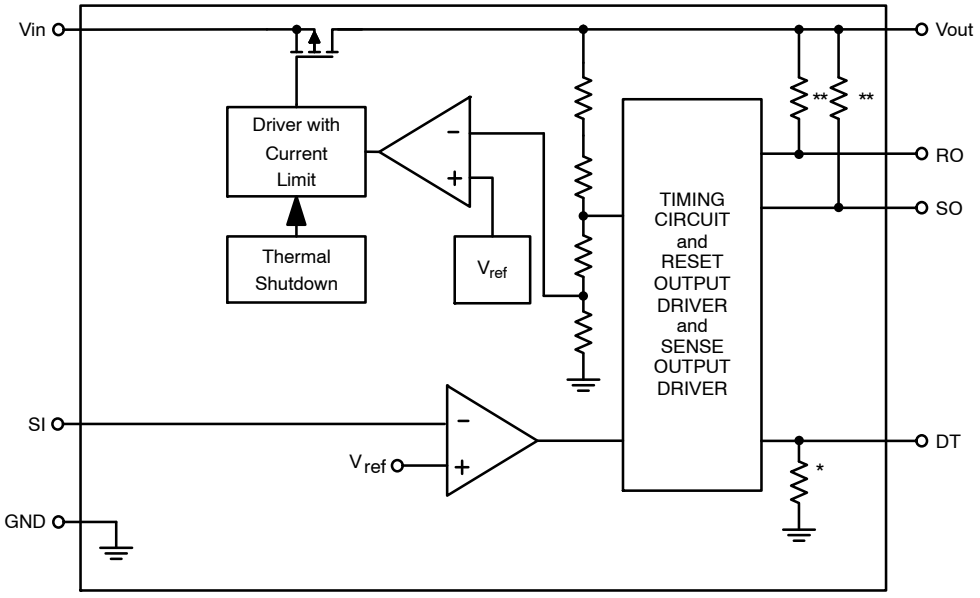


Y	= Timing and Reset Threshold Option*
Z	= Early Warning Option*
XX	= Voltage Option 5.0 V (XX = 50)
A	= Assembly Location
WL	= Wafer Lot
Y	= Year
WW	= Work Week
G	= Pb−Free Package

*See Application Information Section.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 13 of this data sheet.



*Pull−down Resistor (~150 kΩ) active only in Reset State.
** 5 V option only.

Figure 2. Simplified Block Diagram

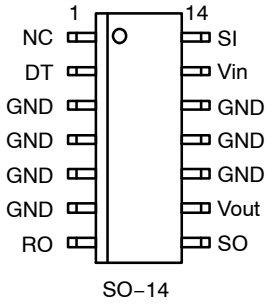


Figure 3. Pin Connections
(Top View)

PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Description
1	NC	Not connected
2	DT	Reset Delay Time Select. Short to GND or connect to V_{out} to select time.
3, 4, 5, 6, 10, 11, 12	GND	Power Supply Ground.
7	RO	Reset Output. 30 kΩ internal Pull−Up resistor connected to V_{out}. RO goes Low when V_{out} drops by more than 7% (typ.) from its nominal value.
8	SO	Early Warning Output. 30 kΩ internal Pull−Up resistor connected to V_{out}. It can be used to provide early warning of an impending reset condition. Leave open if not used.
9	V_{out}	Regulated Output Voltage. Connect 1 μF capacitor with ESR < 100 Ω to ground.
13	V_{in}	Positive Power Supply Input. Connect 0.1 μF capacitor to ground.
14	SI	Sense Input; If not used, connect to V_{out}. See Electrical Characteristics Table and Application Information sections for more information.

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Min	Max	Unit
Input Voltage DC (Note 1)	V_{in}	−0.3	40	V
Input Voltage Transient (Note 1)	V_{in}	–	45	V
Input Current	I_{in}	−5	–	mA
Output Voltage (Note 2)	V_{out}	−0.3	5.5	V
Output Current	I_{out}	−3	Current Limited	mA
DT (Reset Delay Time Select) Voltage	V_{DT}	−0.3	5.5	V
DT (Reset Delay Time Select) Current	I_{DT}	−1	1	mA
Reset Output Voltage	V_{RO}	−0.3	5.5	V
Reset Output Current	I_{RO}	−3	3	mA
Sense Input Voltage DC	V_{SI}	−0.3	40	V
Sense Input Voltage Transient	V_{SI}	–	45	V
Sense Input Current	I_{SI}	−1	1	mA
Sense Output Voltage	V_{SO}	−0.3	5.5	V
Sense Output Current	I_{SO}	−3	3	mA
Maximum Junction Temperature	$T_{J(max)}$	−40	150	°C
Storage Temperature	T_{STG}	−55	150	°C
ESD Capability, Human Body Model (Note 3)	ESD_{HBM}	−2	2	kV
ESD Capability, Machine Model (Note 3)	ESD_{MM}	−200	200	V
Lead Temperature Soldering Reflow (SMD Styles Only) (Note 4)	T_{SLD}	–	265 peak	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Refer to ELECTRICAL CHARACTERISTIS and APPLICATION INFORMATION for Safe Operating Area.
2. 5.5 or (V_{in} + 0.3 V), whichever is lower
3. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (EIA/JESD22−A114)
   ESD Machine Model tested per AEC−Q100−003 (EIA/JESD22−A115)
4. For information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Characteristics, SO−14 (Note 5) Thermal Resistance, Junction−to−Air (Note 6) Thermal Reference, Junction−to−Pin4 (Note 6)	 $R_{\theta JA}$ $\Psi_{\psi JP4}$	 94 18	°C/W

5. Refer to ELECTRICAL CHARACTERISTIS and APPLICATION INFORMATION for Safe Operating Area.
6. Values based on copper area of 645 mm^2 (or 1 in^2) of 1 oz copper thickness and FR4 PCB substrate.

OPERATING RANGES (Note 7)

Rating	Symbol	Min	Max	Unit
Input Voltage (Note 8)	V_{in}	5.5	40	V
Junction Temperature	T_J	−40	150	°C

7. Refer to ELECTRICAL CHARACTERISTIS and APPLICATION INFORMATION for Safe Operating Area.
8. Minimum V_{in} = 5.5 V or (V_{out} + V_{DO}), whichever is higher.

ELECTRICAL CHARACTERISTICS V_{in} = 13.2 V, V_{DT} = GND, V_{SI} = V_{out}, R_{SI1} & R_{SI2} not used, C_{in} = 0.1 μF, C_{out} = 1 μF, for typical values T_J = 25°C, for min/max values T_J = −40 °C to 150°C; unless otherwise noted. (Notes 9 and 10)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
REGULATOR OUTPUT						
Output Voltage (Accuracy %)	V_{in} = 5.6 V to 40 V, I_{out} = 0.1 mA to 100 mA V_{in} = 5.8 V to 16 V, I_{out} = 0.1 mA to 150 mA	V_{out}	4.9 4.9 (−2 %)	5.0 5.0	5.1 5.1 (+2%)	V
Output Voltage (Accuracy %)	T_J = −40°C to 125°C V_{in} = 5.8 V to 28 V, I_{out} = 0 mA to 150 mA	V_{out}	4.9 (−2 %)	5.0	5.1 (+2%)	V
Line Regulation	V_{in} = 6 V to 28 V, I_{out} = 5 mA	Reg_{line}	−20	0	20	mV
Load Regulation	I_{out} = 0.1 mA to 150 mA	Reg_{load}	−40	10	40	mV
Dropout Voltage (Note 11)	I_{out} = 100 mA I_{out} = 150 mA	V_{DO}	− −	225 300	450 600	mV
Output Capacitor for Stability (Note 12)	I_{out} = 0 mA to 150 mA	C_{out} ESR	1.0 0.01	− −	100 100	μF Ω
QUIESCENT CURRENTS						
Quiescent Current, $I_q = I_{in} - I_{out}$	I_{out} = 0.1 mA, T_J = 25°C I_{out} = 0.1 mA to 150 mA, $T_J \le$ 125°C	I_q	− −	25 −	31 33	μA
CURRENT LIMIT PROTECTION						
Current Limit	V_{out} = 0.96 x V_{out_nom}	I_{LIM}	205	−	525	mA
Short Circuit Current Limit	V_{out} = 0 V	I_{SC}	205	−	525	mA
PSRR						
Power Supply Ripple Rejection (Note 12)	f = 100 Hz, 0.5 V_{pp}	PSRR	−	60	−	dB
DT (Reset Delay Time Select)						
DT Threshold Voltage Logic Low Logic High		$V_{th(DT)}$	 − 2	 − −	 0.8 −	V
DT Input Current	V_{DT} = 5 V	I_{DT}	−	−	1	μA

9. Refer to ABSOLUTE MAXIMUM RATINGS and APPLICATION INFORMATION for Safe Operating Area.
10. Performance guaranteed over the indicated operating temperature range by design and/or characterization tested at $T_A \approx T_J$. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
11. Measured when output voltage falls 100 mV below the regulated voltage at V_{in} = 13.2 V.
12. Values based on design and/or characterization.
13. See APPLICATION INFORMATION section for Reset Thresholds and Reset Delay Time Options.

ELECTRICAL CHARACTERISTICS V_{in} = 13.2 V, V_{DT} = GND, $V_{SI} = V_{out}$, R_{SI1} & R_{SI2} not used, C_{in} = 0.1 μF, C_{out} = 1 μF, for typical values T_J = 25°C, for min/max values T_J = −40 °C to 150°C; unless otherwise noted. (Notes 9 and 10)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
RESET OUTPUT RO						
Output Voltage Reset Threshold (Note 13)	V_{out} decreasing V_{in} > 5.5 V	V_{RT}	90	93	96	%V_{out}
Reset Hysteresis		V_{RH}	–	2.0	–	%V_{out}
Maximum Reset Sink Current	V_{out} = 4.5 V, V_{RO} = 0.25 V	I_{ROmax}	1.75	–	–	mA
Reset Output Low Voltage	V_{out} > 1 V, I_{RO} < 200 μA	V_{ROL}	–	0.15	0.25	V
Reset Output High Voltage		V_{ROH}	4.5	–	–	V
Integrated Reset Pull Up Resistor		R_{RO}	15	30	50	kΩ
Reset Delay Time (Note 13)	DT connected to GND DT connected to V_{out}	t_{RD}	12.8 25.6	16 32	19.2 38.4	ms
Reset Reaction Time (see Figure 29)		t_{RR}	16	25	38	μs
EARLY WARNING (SI and SO)						
Sense Input Threshold (NCV8769y0) High Low		$V_{SI(th)}$	1.25 1.20	1.33 1.25	1.40 1.33	V
Sense Input Current (NCV8769y0)	V_{SI} = 5 V	I_{SI}	−1	0.1	1	μA
Integrated Sense Output Pull Up Resistor		R_{SO}	15	30	50	kΩ
Sense Output Low Voltage	V_{SI} < 1.2 V, I_{SO} < 200 μA, V_{out} > 1 V	V_{SOL}	–	0.15	0.25	V
Sense Output High Voltage		V_{SOH}	4.5	–	–	V
Maximum Sense Output Sink Current	V_{out} = 4.5 V, V_{SI} < 1.2 V, V_{SO} = 0.25 V	I_{SOmax}	1.75	–	–	mA
SI High to SO High Reaction Time	V_{SI} increasing	t_{PSOLH}	–	7	12	μs
SI Low to SO Low Reaction Time	V_{SI} decreasing	t_{PSOHL}	–	3.8	5.0	μs
THERMAL SHUTDOWN						
Thermal Shutdown Temperature (Note 12)		T_{SD}	150	175	195	°C
Thermal Shutdown Hysteresis (Note 12)		T_{SH}	–	25	–	°C

9. Refer to ABSOLUTE MAXIMUM RATINGS and APPLICATION INFORMATION for Safe Operating Area.
10. Performance guaranteed over the indicated operating temperature range by design and/or characterization tested at $T_A \approx T_J$. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
11. Measured when output voltage falls 100 mV below the regulated voltage at V_{in} = 13.2 V.
12. Values based on design and/or characterization.
13. See APPLICATION INFORMATION section for Reset Thresholds and Reset Delay Time Options.

TYPICAL CHARACTERISTICS

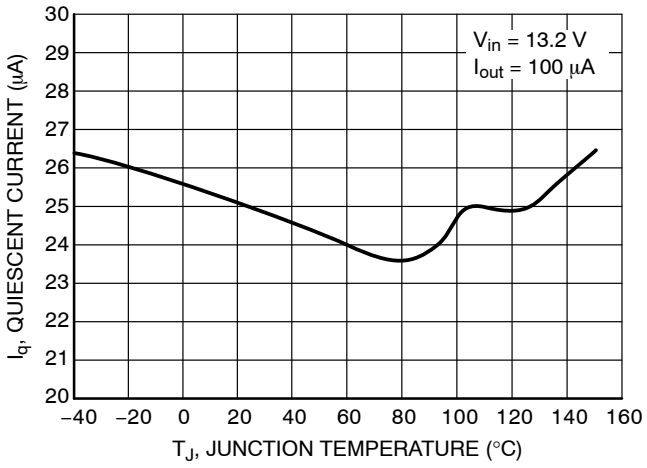


Figure 4. Quiescent Current vs. Temperature

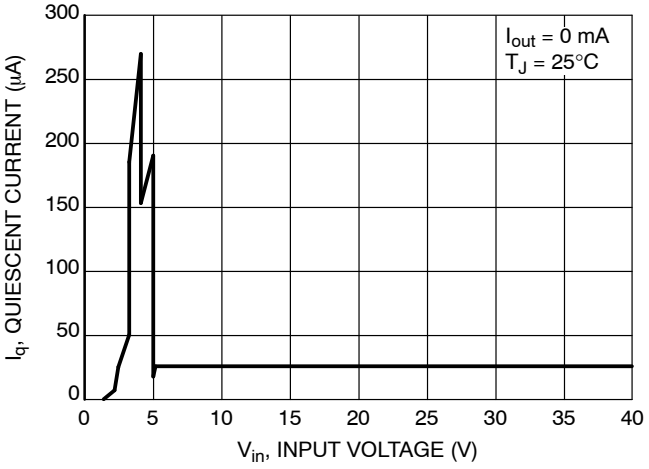


Figure 5. Quiescent Current vs. Input Voltage

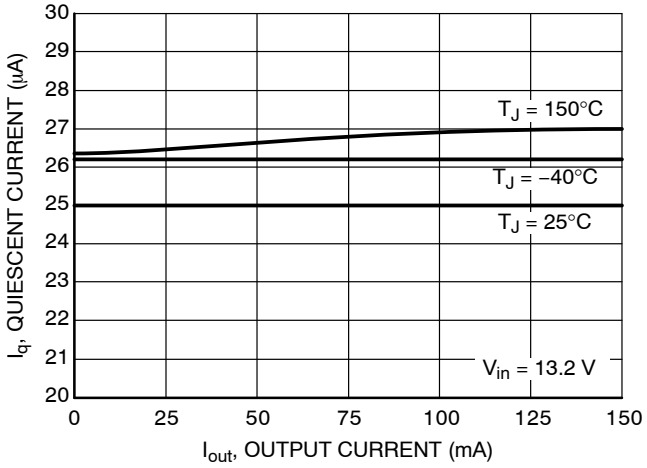


Figure 6. Quiescent Current vs. Output Current

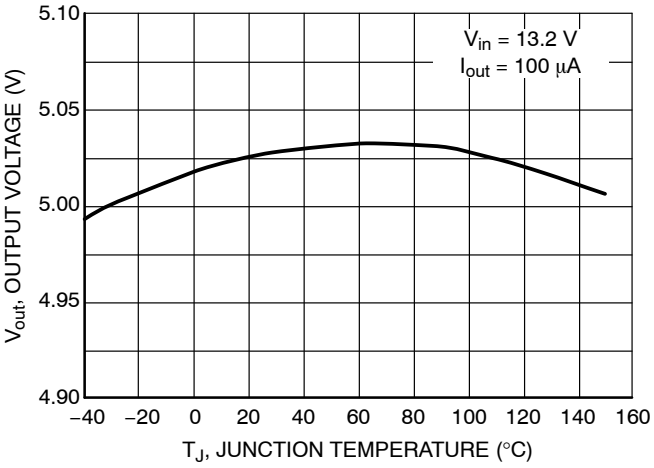


Figure 7. Output Voltage vs. Temperature

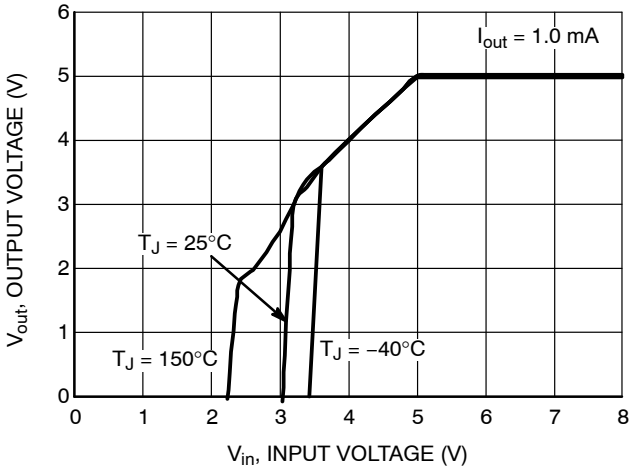


Figure 8. Output Voltage vs. Input Voltage

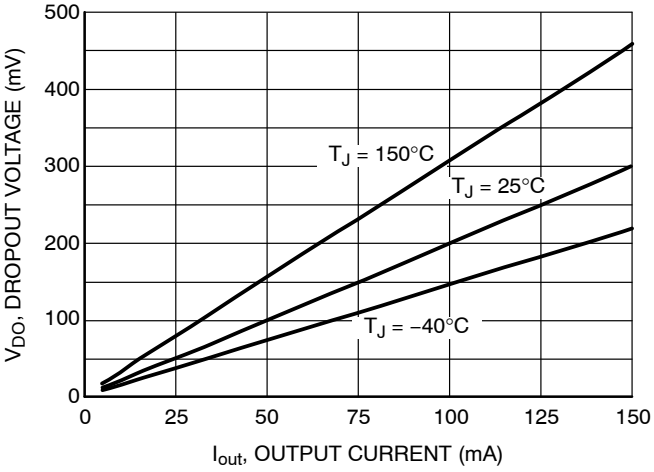


Figure 9. Dropout vs. Output Current

TYPICAL CHARACTERISTICS

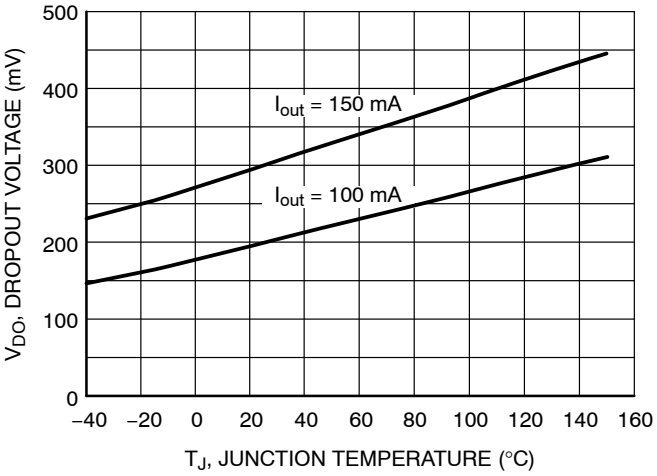


Figure 10. Dropout vs. Temperature

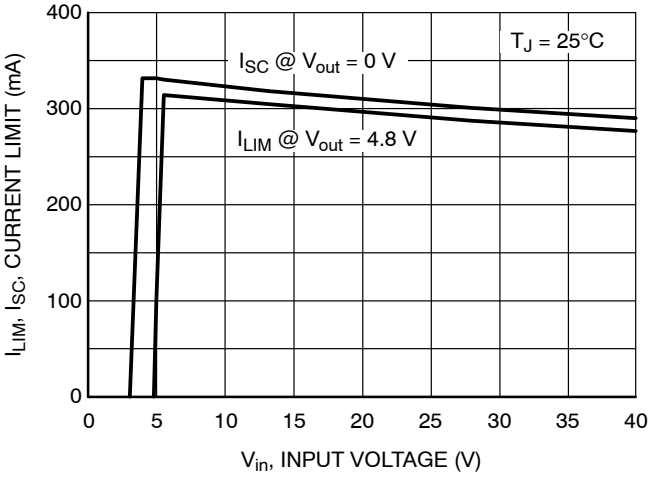


Figure 11. Output Current Limit vs. Input Voltage

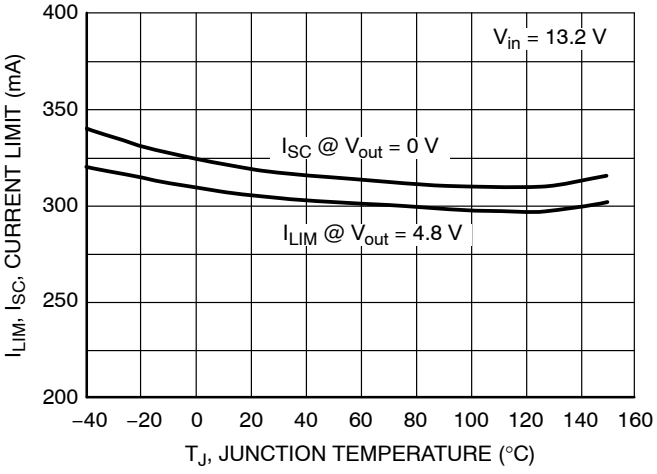


Figure 12. Output Current Limit vs. Temperature

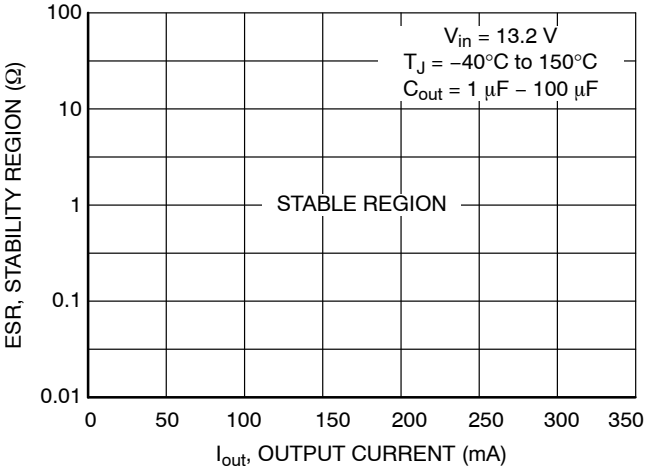


Figure 13. C_{out} ESR Stability vs. Output Current

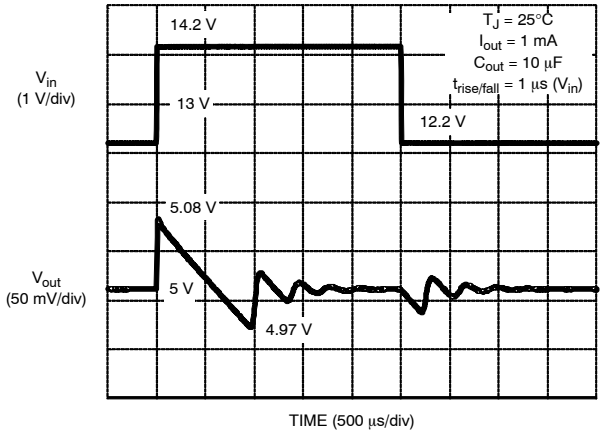


Figure 14. Line Transients

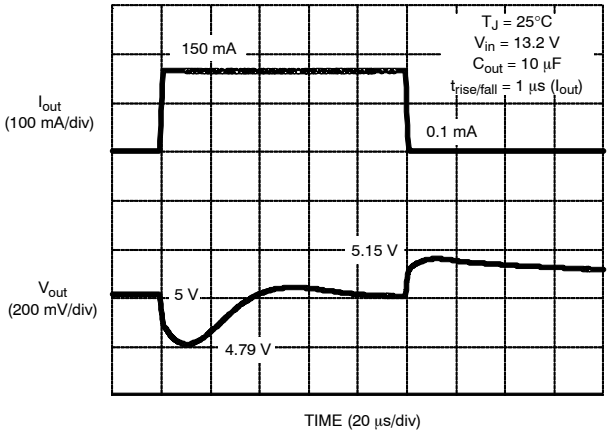


Figure 15. Load Transients

TYPICAL CHARACTERISTICS

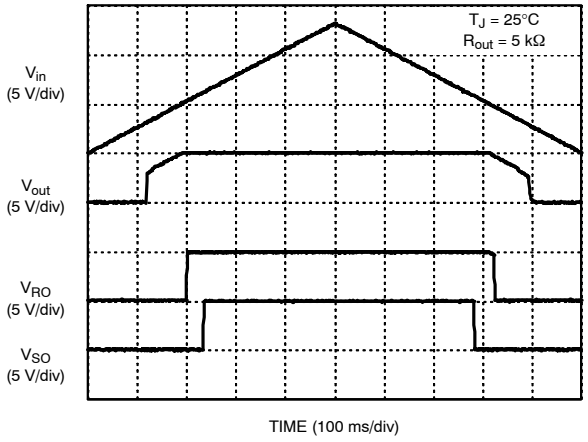


Figure 16. Power Up and Down Transient

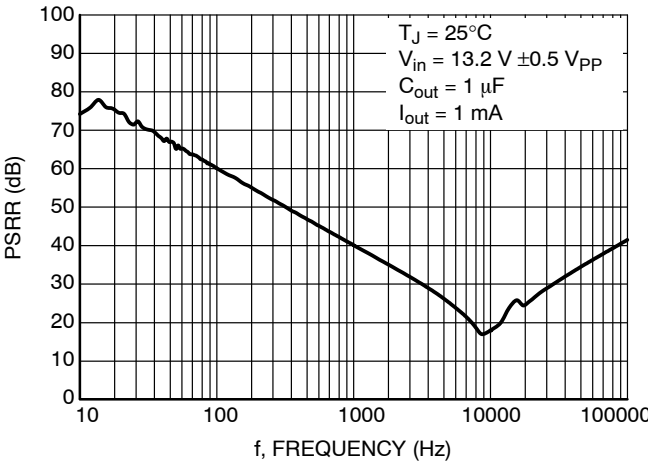


Figure 17. PSRR vs. Frequency

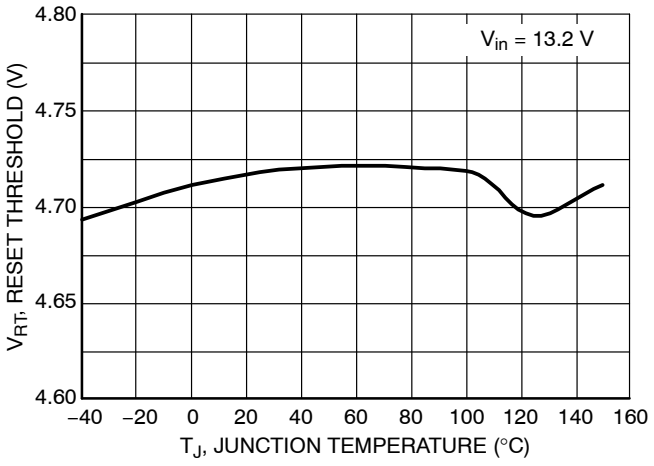


Figure 18. Reset Threshold vs. Temperature

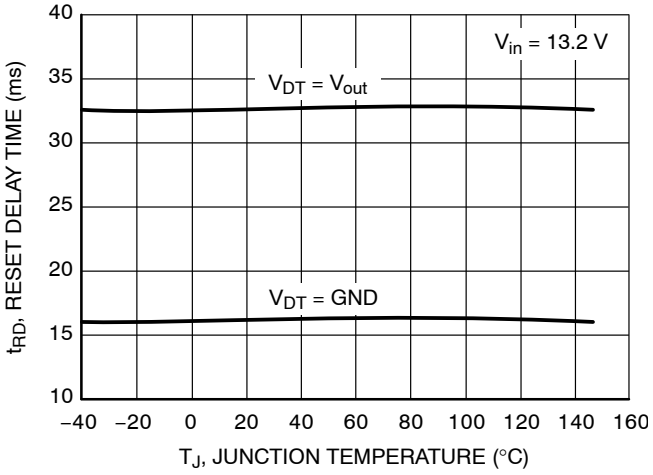


Figure 19. Reset Time vs. Temperature

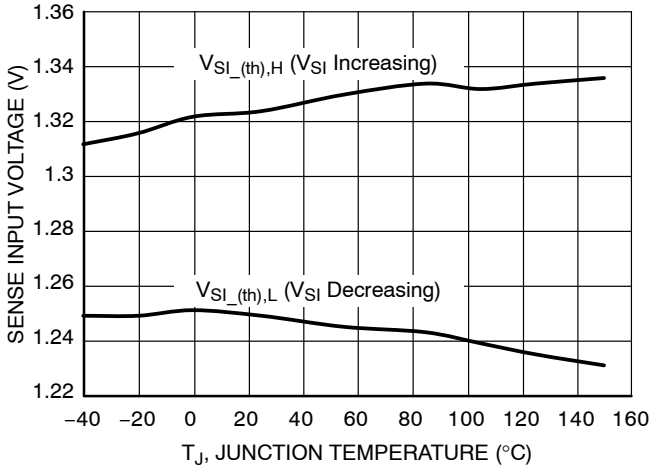


Figure 20. SI Threshold vs. Temperature

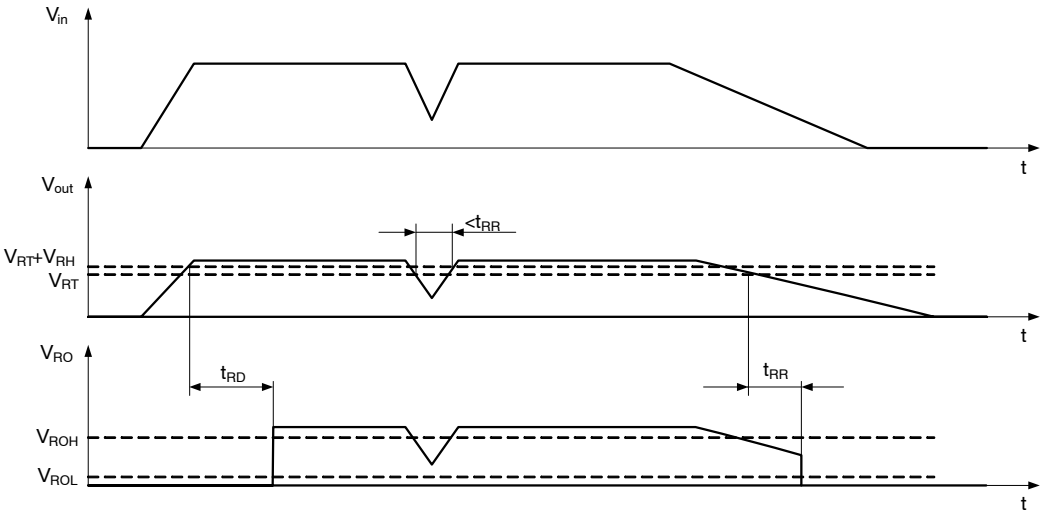


Figure 21. Reset Function and Timing Diagram

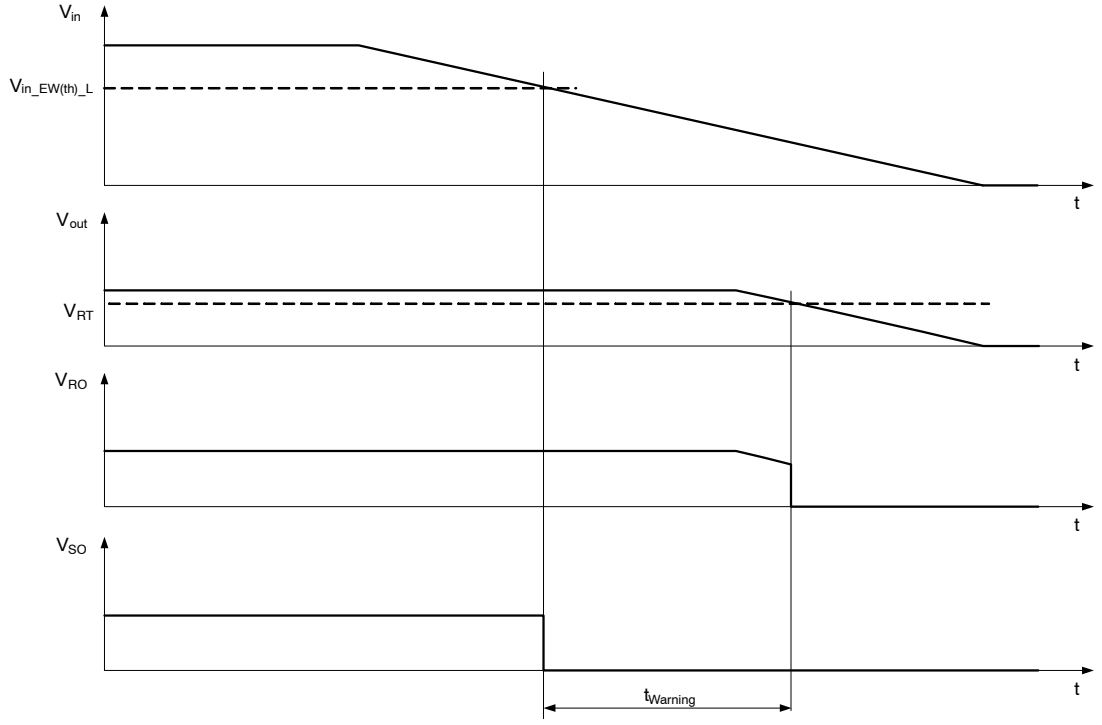


Figure 22. Input Voltage Early Warning Function Diagram

DEFINITIONS

General

All measurements are performed using short pulse low duty cycle techniques to maintain junction temperature as close as possible to ambient temperature.

Output Voltage

The output voltage parameter is defined for specific temperature, input voltage and output current values or specified over Line, Load and Temperature ranges.

Line Regulation

The change in output voltage for a change in input voltage measured for specific output current over operating ambient temperature range.

Load Regulation

The change in output voltage for a change in output current measured for specific input voltage over operating ambient temperature range.

Dropout Voltage

The input to output differential at which the regulator output no longer maintains regulation against further reductions in input voltage. It is measured when the output drops 100 mV below its nominal value. The junction temperature, load current, and minimum input supply requirements affect the dropout level.

Quiescent Current

Quiescent Current (I_q) is the difference between the input current (measured through the LDO input pin) and the output load current.

Current Limit and Short Circuit Current Limit

Current Limit is value of output current by which output voltage drops below 96% of its nominal value. It means that the device is capable to supply minimum 200 mA without sending Reset signal to microprocessor.

Short Circuit Current Limit is output current value measured with output of the regulator shorted to ground.

PSRR

Power Supply Rejection Ratio is defined as ratio of output voltage and input voltage ripple. It is measured in decibels (dB).

Line Transient Response

Typical output voltage overshoot and undershoot response when the input voltage is excited with a given slope.

Load Transient Response

Typical output voltage overshoot and undershoot response when the output current is excited with a given slope between low−load and high−load conditions.

Thermal Protection

Internal thermal shutdown circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When activated at typically 175°C, the regulator turns off. This feature is provided to prevent failures from accidental overheating.

Maximum Package Power Dissipation

The power dissipation level is maximum allowed power dissipation for particular package or power dissipation at which the junction temperature reaches its maximum operating value, whichever is lower.

APPLICATIONS INFORMATION

The NCV8769 regulator is self−protected with internal thermal shutdown and internal current limit. Typical characteristics are shown in Figures 4 to 22.

Input Decoupling (C_{in})

A ceramic or tantalum 0.1 μF capacitor is recommended and should be connected close to the NCV8769 package. Higher capacitance and lower ESR will improve the overall line and load transient response.

If extremely fast input voltage transients are expected then appropriate input filter must be used in order to decrease rising and/or falling edges below 50 V/μs for proper operation. The filter can be composed of several capacitors in parallel.

Output Decoupling (C_{out})

The NCV8769 is a stable component and does not require a minimum Equivalent Series Resistance (ESR) for the output capacitor. Stability region of ESR vs. Output Current is shown in Figure 13. The minimum output decoupling value is 1 μF and can be augmented to fulfill stringent load transient requirements. The regulator works with ceramic chip capacitors as well as tantalum devices. Larger values improve noise rejection and load transient response.

Reset Delay Time Select

Selection of the NCV8769yz devices and the state of the DT pin determines the available Reset Delay times. The part is designed for use with DT tied to ground or OUT, but may be controlled by any logic signal which provides a threshold between 0.8 V and 2 V. The default condition for an open DT pin is the slower Reset time (DT = GND condition). Times are in pairs and are highlighted in the chart below. Consult factory for availability. The Delay Time select (DT) pin is logic level controlled and provides Reset Delay time per the chart. Note the DT pin is sampled only when RO is low, and changes to the DT pin when RO is high will not effect the reset delay time.

Reset Operation

A reset signal is provided on the Reset Output (RO) pin to provide feedback to the microprocessor of an out of regulation condition. The timing diagram of reset function is shown in Figure 21. This is in the form of a logic signal on RO. Output voltage conditions below the RESET threshold cause RO to go low. The RO integrity is maintained down to V_{out} = 1.0 V. The Reset Output (RO) circuitry includes internal pull−up connected to the output (V_{out}) No external pull−up is necessary.

Reset signal is also generated in case when input voltage decreases below its minimum operating limit.

RESET DELAY AND RESET THRESHOLD OPTIONS

Part Number	DT = GND Reset Time	DT = V_{out} Reset Time	Reset Threshold
NCV87695z	16 ms	32 ms	93%

NOTE: The timing values can be selected from following list: 8, 16, 32, 64, 128 ms. The reset threshold values can be selected from the following list: 90% and 93%. Contact factory for other timing combinations not included in the table.

Sense Input (SI)/Sense Output (SO) Voltage Monitor

An on-chip comparator is available to provide early warning to the microprocessor of a possible reset signal. The reset signal typically turns the microprocessor off instantaneously. This can cause unpredictable results with the microprocessor. The signal received from the SO pin will allow the microprocessor time ($T_{WARNING}$) to complete its present task before shutting down. This function is performed by a comparator referenced to the band gap voltage. The actual trip point can be programmed externally using a resistor divider to the input monitor (SI). (See Figure 1) The values for R_{SI1} and R_{SI2} are selected for a typical threshold of 1.2 V on the SI pin according to Equations 1 and 2, where $V_{in\_EW(th)}$ is demanded value of input voltage at which Early Warning signal has to be generated. R_{SI2} is recommended to be selected in range of 100 kΩ to 1 MΩ. The higher are values of resistors R_{SI1} and R_{SI2} the lower is current flowing through the resistor divider, however this also increases a delay between Input voltage and SI input voltage caused by charging SI input capacitance with higher RC constant. The delay can be lowered by decreasing the resistors values with consequence of resistor divider current is increased.

$$V_{in\_EW(th)} = 1.25\left(1 + \frac{R_{SI1}}{R_{SI2}}\right) \quad \text{(eq. 1)}$$

$$R_{SI1} = R_{SI2}\left(\frac{V_{in\_EW(th)}}{1.2} - 1\right) \quad \text{(eq. 2)}$$

Sense Output

The Sense Output is from an open drain driver with an internal 30 kΩ pull up resistor to V_{out}. Figure 23 shows the SO Monitor timing waveforms as a result of the circuit depicted in Figure 1. If the input voltage decreases the output voltage decreases as well. If the SI input low threshold voltage is crossed it causes the voltage on the SO output goes low sending a warning signal to the microprocessor that a reset signal may occur in a short period of time. $T_{WARNING}$ is the time the microprocessor has to complete the function it is currently working on and get ready for the reset shutdown signal.

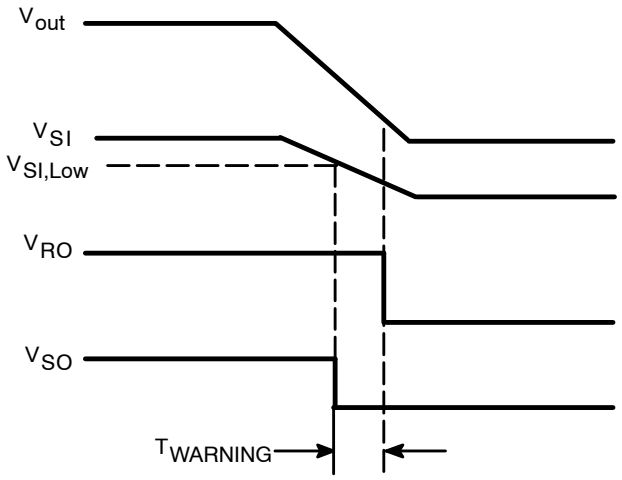


Figure 23. SO Warning Timing Diagram

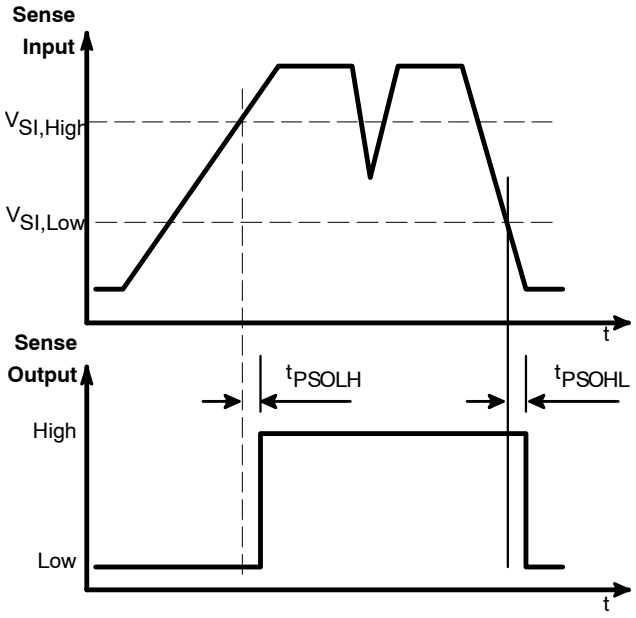


Figure 24. Sense Input to Sense Output Timing Diagram

Thermal Considerations

As power in the NCV8769 increases, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and the ambient temperature affect the rate of junction temperature rise for the part. When the NCV8769 has good thermal conductivity through the PCB, the junction temperature will be relatively low with high power applications. The maximum dissipation the NCV8769 can handle is given by:

$$P_{D(MAX)} = \frac{\left[T_{J(MAX)} - T_A\right]}{R_{\theta JA}} \quad \text{(eq. 3)}$$

Since T_J is not recommended to exceed 150°C, then the NCV8769 soldered on 645 mm^2, 1 oz copper area, FR4 can dissipate up to 1.33 W when the ambient temperature (T_A) is 25°C. See Figure 25 for R_{thJA} versus PCB area. The power dissipated by the NCV8769 can be calculated from the following equations:

$$P_D \approx V_{in}\left(I_q @ I_{out}\right) + I_{out}\left(V_{in} - V_{out}\right) \quad \text{(eq. 4)}$$

or

$$V_{in(MAX)} \approx \frac{P_{D(MAX)} + \left(V_{out} \times I_{out}\right)}{I_{out} + I_q} \quad \text{(eq. 5)}$$

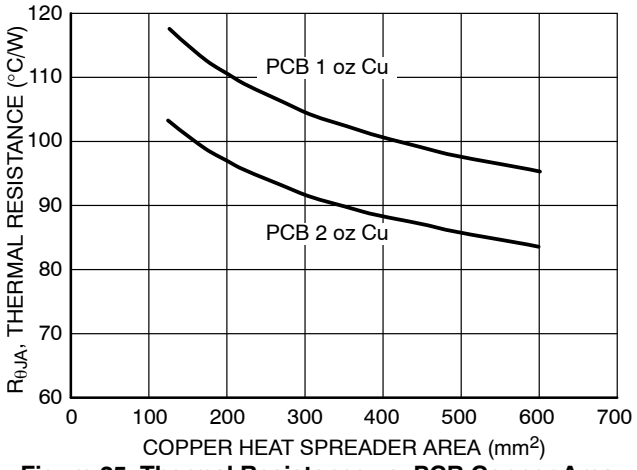


Figure 25. Thermal Resistance vs. PCB Copper Area

Hints

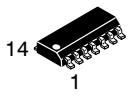
V_{in} and GND printed circuit board traces should be as wide as possible. When the impedance of these traces is high, there is a chance to pick up noise or cause the regulator to malfunction. Place external components, especially the output capacitor, as close as possible to the NCV8769 and make traces as short as possible.

ORDERING INFORMATION

Device	Output Voltage	Reset Delay Time DT = GND/V_{out}	Reset Threshold (Typ)	Marking	Package	Shipping†
NCV876950D250R2G	5.0 V	16/32 ms	93 %	V87695050G	SO−14 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D

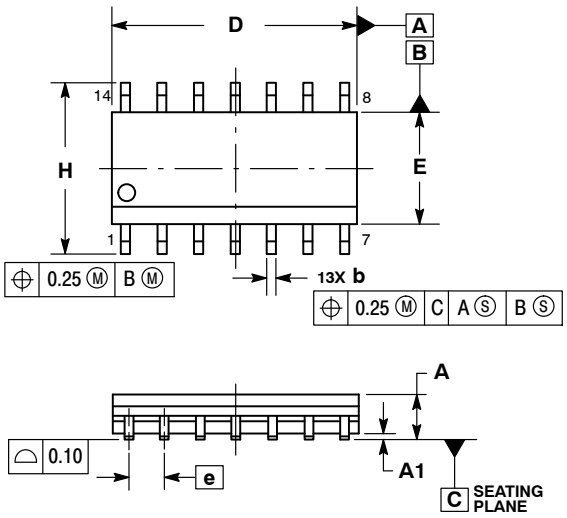
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

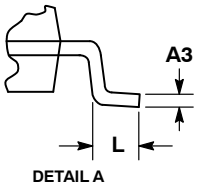


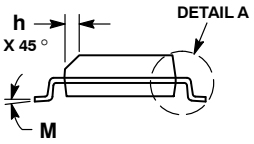
SCALE 1:1

SOIC−14 NB
CASE 751A−03
ISSUE L

DATE 03 FEB 2016



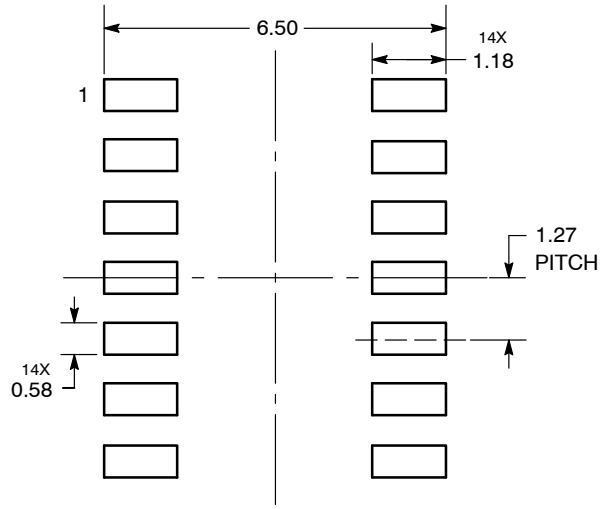




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0 °	7 °	0 °	7 °

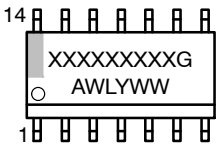
SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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DESCRIPTION:	**SOIC−14 NB**		**PAGE 1 OF 2**

SOIC−14
CASE 751A−03
ISSUE L

DATE 03 FEB 2016

STYLE 1:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. NO CONNECTION
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. NO CONNECTION
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 2:
CANCELLED

STYLE 3:
PIN 1. NO CONNECTION
2. ANODE
3. ANODE
4. NO CONNECTION
5. ANODE
6. NO CONNECTION
7. ANODE
8. ANODE
9. ANODE
10. NO CONNECTION
11. ANODE
12. ANODE
13. NO CONNECTION
14. COMMON CATHODE

STYLE 4:
PIN 1. NO CONNECTION
2. CATHODE
3. CATHODE
4. NO CONNECTION
5. CATHODE
6. NO CONNECTION
7. CATHODE
8. CATHODE
9. CATHODE
10. NO CONNECTION
11. CATHODE
12. CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 5:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. NO CONNECTION
7. COMMON ANODE
8. COMMON CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. ANODE/CATHODE
12. ANODE/CATHODE
13. NO CONNECTION
14. COMMON ANODE

STYLE 6:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. ANODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE

STYLE 7:
PIN 1. ANODE/CATHODE
2. COMMON ANODE
3. COMMON CATHODE
4. ANODE/CATHODE
5. ANODE/CATHODE
6. ANODE/CATHODE
7. ANODE/CATHODE
8. ANODE/CATHODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. COMMON CATHODE
12. COMMON ANODE
13. ANODE/CATHODE
14. ANODE/CATHODE

STYLE 8:
PIN 1. COMMON CATHODE
2. ANODE/CATHODE
3. ANODE/CATHODE
4. NO CONNECTION
5. ANODE/CATHODE
6. ANODE/CATHODE
7. COMMON ANODE
8. COMMON ANODE
9. ANODE/CATHODE
10. ANODE/CATHODE
11. NO CONNECTION
12. ANODE/CATHODE
13. ANODE/CATHODE
14. COMMON CATHODE

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