

NB3N2304NZ

3.3V 1:4 Clock Fanout Buffer

Description

The NB3N2304NZ is a low skew 1-to 4 clock fanout buffer, designed for high speed clock distribution such as in PCI-X applications. The NB3N2304NZ guarantees low output-to-output skew. Optimal design, layout and processing minimizes skew within a device and from device-to-device.

The Output Enable (OE) pin forces the outputs LOW when LOW.

Features

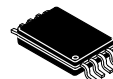
- Input/Output Clock Frequency up to 140 MHz
- Low Skew Outputs (100 ps)
- Output Enable
- Operating Range: $V_{DD} = 3.0\text{ V to }3.6\text{ V}$
- Ideal for PCI-X and networking clocks
- Packaged in 8-pin TSSOP, 4.4 mm x 3 mm
- Industrial Temperature Range
- These are Pb-Free Devices*



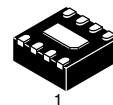
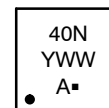
ON Semiconductor®

<http://onsemi.com>

MARKING DIAGRAM*



TSSOP-8
DT SUFFIX
CASE 948S



DFN8
MN SUFFIX
CASE 506AA



A = Assembly Location
Y = Year
WW = Work Week
M̄ = Date Code
▪ = Pb-Free Package

*For additional marking information, refer to Application Note AND8002/D.

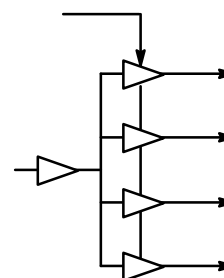


Figure 1. Simplified Logic Diagram

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NB3N2304NZ

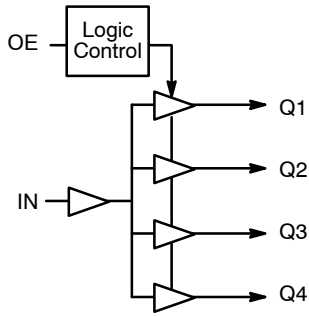


Figure 2. Block Diagram

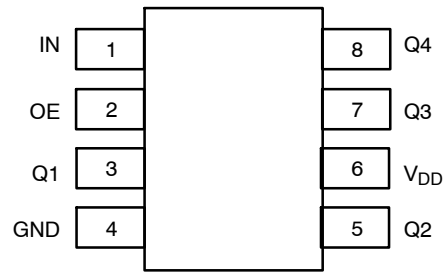


Figure 3. NB3N2304NZ Package Pinout (Top View)

Table 1. PIN DESCRIPTION

Pin #	Pin Name	Type	Description
1	IN	LVC MOS/LVTTL Input	Clock Input
2	OE	LVC MOS/LVTTL Input	Output Enable for the clock outputs. Outputs are enabled when forced HIGH. Outputs are forced to logic LOW when OE is forced LOW.
3	Q1	LVC MOS/LVTTL Output	Clock Output 1
4	GND	Power	Negative Supply Voltage; Connect to Ground, 0 V
5	Q2	(LV)CMOS/(LV)TTL Input	Clock Output 2
6	V _{DD}	Power	Positive Supply Voltage (3.0 V to 3.6 V)
7	Q3	(LV)CMOS/(LV)TTL Output	Clock Output 3
8	Q4	(LV)CMOS/(LV)TTL Input	Clock Output 4
-	EP	Thermal Exposed Pad	(DFN8 only) Thermal exposed pad must be connected to a sufficient thermal conduit. Electrically connect to the most negative supply (GND) or leave unconnected, floating open.

Table 2. OE, OUTPUT ENABLE FUNCTION TABLE

Inputs		Outputs
IN	OE	
L	L	L
H	L	L
L	H	L
H	H	H

NB3N2304NZ

Table 3. ATTRIBUTES

Characteristics		Value
ESD Protection	Human Body Model Machine Model	> 2kV > 200 V
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)	TSSOP-8 DFN-8	Level 3 Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V-O @ 0.125 in
Transistor Count		480 Devices
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

1. For additional information, see Application Note AND8003/D.

Table 4. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V _{DD}	Positive Power Supply	GND = 0 V		V _{DD} + 0.5V	V
V _I	Input Voltage			GND - 0.5 ≤ V _I ≤ V _{DD} + 0.5	V
T _A	Operating Temperature Range, Industrial			≥ -40 to ≤ +85	°C
T _{stg}	Storage Temperature Range			-65 to +150	°C
θ _{JA}	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm 0 lfpm 500 lfpm	TSSOP-8 TSSOP-8 DFN-8 DFN-8	143 103 129 84	°C/W
T _{SOL}	Wave Solder Pb-Free	(Note 2)		265	°C
θ _{JC}	Thermal Resistance (Junction-to-Case)	(Note 2)	DFN8	35 to 40	°C/W

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

2. JEDEC standard multilayer board – 2S2P (2 signal, 2 power)

NB3N2304NZ

Table 5. DC CHARACTERISTICS $V_{DD} = 3.0\text{ V to }3.6\text{ V}$, $GND = 0\text{ V}$, $T_A = -40^\circ\text{C to }+85^\circ\text{C}$

Symbol	Characteristic	Min	Typ	Max	Unit
I_{DD}	Power Supply Current @ 66.66 MHz, Unloaded Outputs		12	25	mA
V_{OH}	Output HIGH Voltage – $I_{OH} = -24\text{ mA}$ – $I_{OH} = -12\text{ mA}$	2.0 2.4			V
V_{OL}	Output LOW Voltage – $I_{OL} = 24\text{ mA}$ – $I_{OL} = 12\text{ mA}$			0.8 0.55	V
V_{IH}	Input HIGH Voltage, IN and OE (Note 3)	2.0			V
V_{IL}	Input LOW Voltage, IN and OE (Note 3)			0.8	V
I_{IH}	Input HIGH Current, $V_{IN} = V_{DD}$	-50		50	μA
I_{IL}	Input LOW Current, $V_{IN} = 0\text{ V}$	-100		100	μA
CIN	Input Capacitance, IN, OE		5	7	pF

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

3. IN input has a threshold voltage of $V_{DD}/2$.

Table 6. AC CHARACTERISTICS $V_{DD} = 3.0\text{ V to }3.6\text{ V}$, $GND = 0\text{ V}$, $T_A = -40^\circ\text{C to }+85^\circ\text{C}$ (Note 4) (Figure 4)

Symbol	Characteristic	Min	Typ	Max	Unit
f_{in}	Input Clock Frequency	DC		140	MHz
t_{DCskew}	Duty Cycle Skew = $t_2 \div t_1$ (Figure 4) Measured at 1.5 V	40	50	60	%
tr/tf	Output Rise and Fall Times; 0.8 V to 2.0 V $C_L = 25\text{ pF}$ $C_L = 10\text{ pF}$		0.9 0.6	1.5	ns
t_{pd}	Propagation Delay, IN-to-Qn (Note 5)	2.5	3.5	5	ns
t_{skew}	Output-to-Output Skew; (Note 5)			100	ps
t_{pu}	Powerup Time for V_{DD} to Reach Minimum Specified Voltage	0.05		50	ms

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

4. All outputs loaded equally with $C_L = 25\text{ pF}$ to GND. Duty cycle out = duty in. A $0.01\text{ }\mu\text{F}$ decoupling capacitor should be connected between V_{DD} and GND.

5. Measured on rising edges at $V_{DD} \div 2$; all outputs with equal loading.

NB3N2304NZ

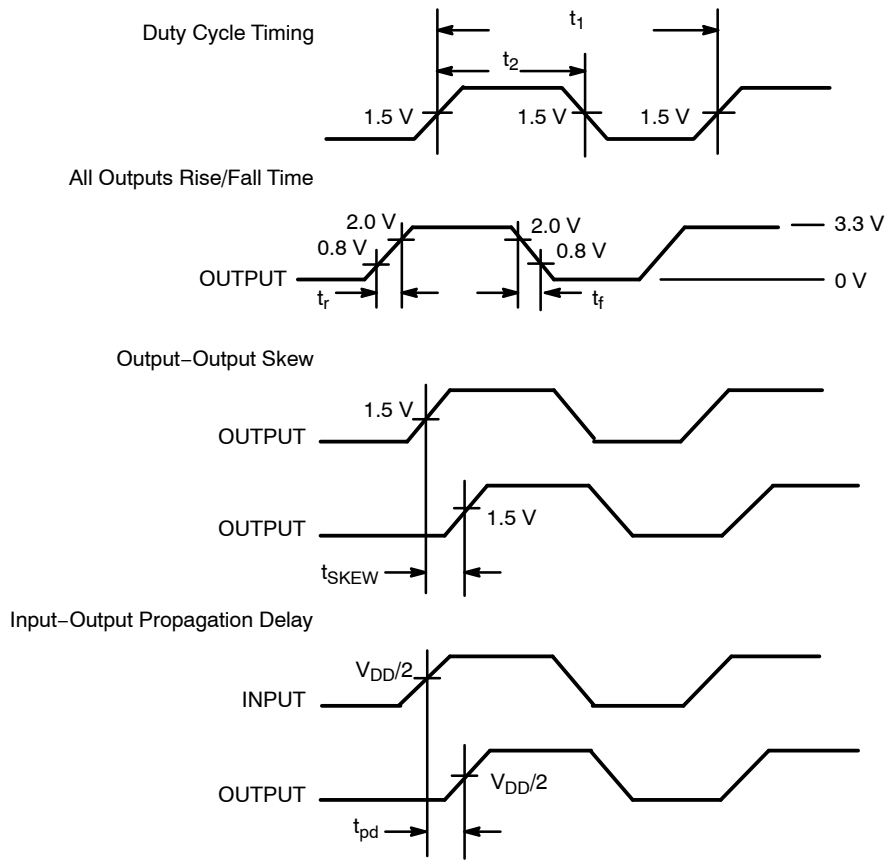


Figure 4. Switching Waveforms

ORDERING INFORMATION

Device	Package	Shipping [†]
NB3N2304NZDTG	TSSOP-8 (Pb-Free)	100 Units / Rail
NB3N2304NZDTR2G	TSSOP-8 (Pb-Free)	2500 / Tape & Reel
NB3N2304NZMNR4G*	DFN8 (Pb-Free)	1000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*Contact a sales representative.

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS



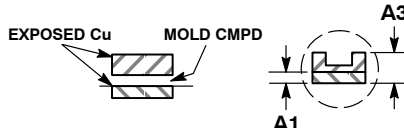
SCALE 4:1

DFN8 2x2, 0.5P
CASE 506AA
ISSUE F

DATE 04 MAY 2016



DETAIL A
OPTIONAL
CONSTRUCTIONS



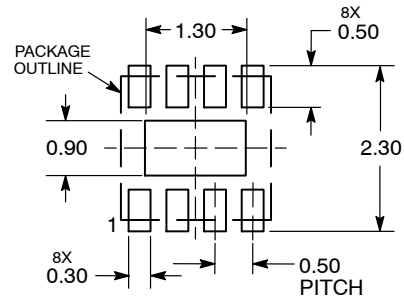
DETAIL B
ALTERNATE
CONSTRUCTIONS

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994 .
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS	
	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	2.00 BSC	
D2	1.10	1.30
E	2.00 BSC	
E2	0.70	0.90
e	0.50 BSC	
K	0.30 REF	
L	0.25	0.35
L1	---	0.10

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

GENERIC MARKING DIAGRAM*



- XX = Specific Device Code
- M = Date Code
- = Pb-Free Device

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

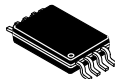
*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DOCUMENT NUMBER:	98AON18658D	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	DFN8, 2.0X2.0, 0.5MM PITCH	PAGE 1 OF 1

onsemi and ONSEMI are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

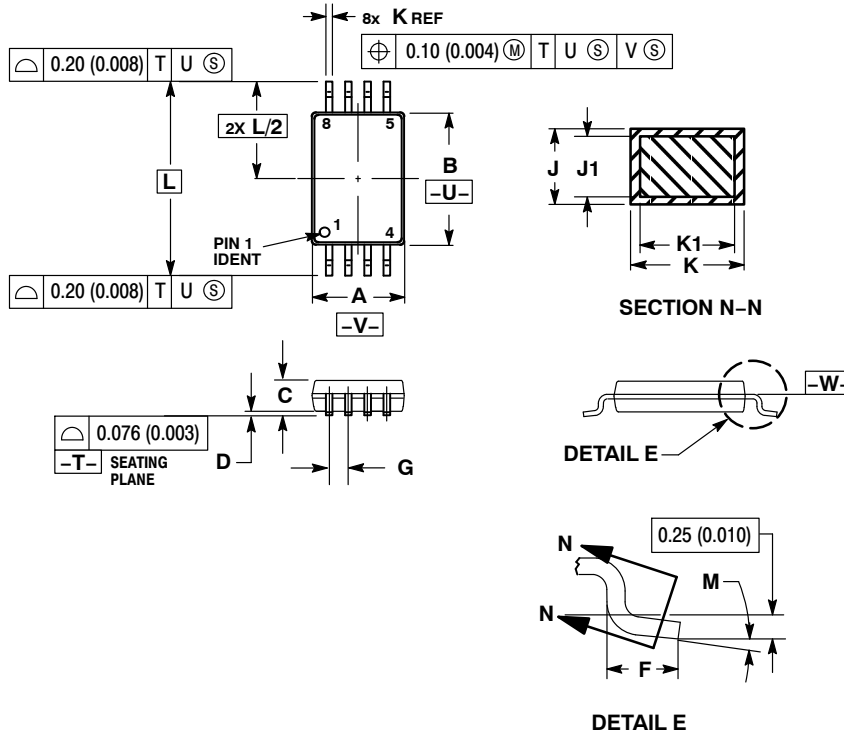
ON Semiconductor®



SCALE 2:1

TSSOP-8
CASE 948S-01
ISSUE C

DATE 20 JUN 2008

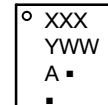


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	4.30	4.50	0.169	0.177
C	---	1.10	---	0.043
D	0.05	0.15	0.002	0.006
F	0.50	0.70	0.020	0.028
G	0.65 BSC		0.026 BSC	
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

GENERIC
MARKING DIAGRAM*



- XXX = Specific Device Code
- A = Assembly Location
- Y = Year
- WW = Work Week
- = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present.

DOCUMENT NUMBER:	98AON00697D	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
STATUS:	ON SEMICONDUCTOR STANDARD	
NEW STANDARD:		
DESCRIPTION:	TSSOP-8	PAGE 1 OF 2

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Email Requests to: orderlit@onsemi.com

onsemi Website: www.onsemi.com

TECHNICAL SUPPORT

North American Technical Support:

Voice Mail: 1 800-282-9855 Toll Free USA/Canada

Phone: 011 421 33 790 2910

Europe, Middle East and Africa Technical Support:

Phone: 00421 33 790 2910

For additional information, please contact your local Sales Representative