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4 Revision History

Changes from Revision I (January 2015) to Revision J (December 2022)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document.....	1
• Updated thermals for DB and PW package.....	5
Changes from Revision H (March 2005) to Revision I (January 2015)	Page
• Added <i>Applications</i> , <i>Device Information</i> table, <i>Pin Functions</i> table, <i>ESD Ratings</i> table, <i>Thermal Information</i> table, <i>Typical Characteristics</i> , <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section.....	1
• Deleted <i>Ordering Information</i> table.....	1

5 Pin Configuration and Functions

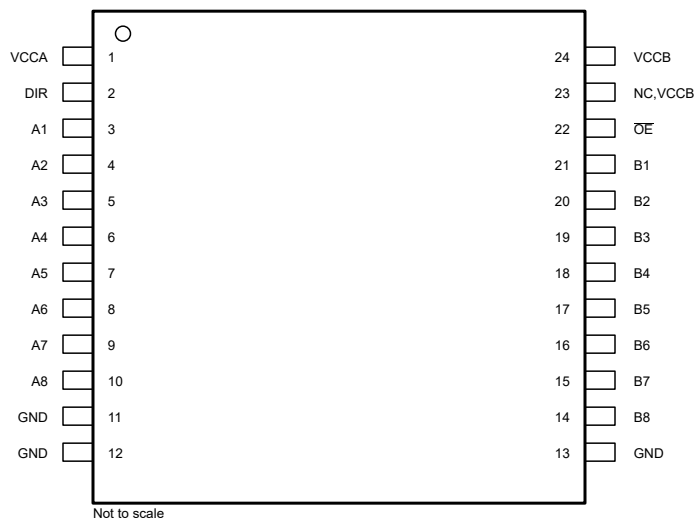


Figure 5-1. DB, DW, or PW Package, SOP, TSSOP, (Top View)

Table 5-1. Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
V _{CCA}	1	—	Power supply for side A
DIR	2	I	Direction control
A1	3	I/O	Transceiver I/O pin
A2	4	I/O	Transceiver I/O pin
A3	5	I/O	Transceiver I/O pin
A4	6	I/O	Transceiver I/O pin
A5	7	I/O	Transceiver I/O pin
A6	8	I/O	Transceiver I/O pin
A7	9	I/O	Transceiver I/O pin
A8	10	I/O	Transceiver I/O pin
GND	11	—	Ground
GND	12	—	Ground
GND	13	—	Ground
B8	14	I/O	Transceiver I/O pin
B7	15	I/O	Transceiver I/O pin
B6	16	I/O	Transceiver I/O pin
B5	17	I/O	Transceiver I/O pin
B4	18	I/O	Transceiver I/O pin
B3	19	I/O	Transceiver I/O pin
B2	20	I/O	Transceiver I/O pin
B1	21	I/O	Transceiver I/O pin
OE	22	I	Output Enable
V _{CCB}	23	—	Power supply for side B
V _{CCB}	24	—	Power supply for side B

(1) I = input, O = output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range for $V_{CCA} = 4.5\text{ V}$ to 5.5 V (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V_{CCA}	Supply voltage range		-0.5	6.5	V
V_I	Input voltage range	A port ⁽²⁾	-0.5	$V_{CCA} + 0.5$	V
		Control inputs	-0.5	6	
V_O	Output voltage range	A port ⁽²⁾	-0.5	$V_{CCA} + 0.5$	V
I_{IK}	Input clamp current	$V_I < 0$		-50	mA
I_{OK}	Output clamp current	$V_O < 0$		-50	mA
I_O	Continuous output current			±50	mA
	Continuous current through each V_{CCA} or GND			±100	mA
T_{stg}	Storage temperature range		-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under [Section 6.4](#) is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) This value is limited to 6 V maximum.

6.2 Absolute Maximum Ratings

over operating free-air temperature range for $V_{CCB} = 2.7\text{ V}$ to 3.6 V (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V_{CCB}	Supply voltage range		-0.5	4.6	V
V_I	Input voltage range	B port ⁽²⁾	-0.5	$V_{CCB} + 0.5$	V
V_O	Output voltage range	B port ⁽²⁾	-0.5	$V_{CCB} + 0.5$	V
I_{IK}	Input clamp current	$V_I < 0$		-50	mA
I_{OK}	Output clamp current	$V_O < 0$		-50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CCB} or GND			±100	mA
T_{stg}	Storage temperature range		-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under [Section 6.4](#) is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) This value is limited to 4.6 V maximum.

6.3 ESD Ratings

PARAMETER	DEFINITION	VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge		
	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	2000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.4 Recommended Operating Conditions

for $V_{CCA} = 4.5\text{ V to }5.5\text{ V}^{(1)}$

		MIN	MAX	UNIT
V_{CCA}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_{IA}	Input voltage	0	V_{CCA}	V
V_{OA}	Output voltage	0	V_{CCA}	V
I_{OH}	High-level output current		–24	mA
I_{OL}	Low-level output current		24	mA
T_A	Operating free-air temperature	–40	85	°C

- (1) All unused inputs of the device must be held at the associated V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

6.5 Recommended Operating Conditions

for $V_{CCB} = 2.7\text{ V to }3.6\text{ V}^{(1)}$

			MIN	MAX	UNIT
V_{CCB}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	$V_{CCB} = 2.7\text{ V to }3.6\text{ V}$	2		V
V_{IL}	Low-level input voltage	$V_{CCB} = 2.7\text{ V to }3.6\text{ V}$		0.8	V
V_{IB}	Input voltage		0	V_{CCB}	V
V_{OB}	Output voltage		0	V_{CCB}	V
I_{OH}	High-level output current	$V_{CCB} = 2.7\text{ V}$		–12	mA
		$V_{CCB} = 3\text{ V}$		–24	
I_{OL}	Low-level output current	$V_{CCB} = 2.7\text{ V}$		12	mA
		$V_{CCB} = 3\text{ V}$		24	
T_A	Operating free-air temperature		–40	85	°C

- (1) All unused inputs of the device must be held at the associated V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

6.6 Thermal Information

THERMAL METRIC ⁽¹⁾		SN74LVC4245A		UNIT
		DB	PW	
		24 PINS		
R _{θJA}	Junction-to-ambient thermal resistance	90.7	100.6	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	51.9	44.7	°C/W
R _{θJB}	Junction-to-board thermal resistance	49.7	55.8	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	18.8	6.8	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	49.3	55.4	°C/W

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

6.7 Electrical Characteristics

over recommended operating free-air temperature range for $V_{CCA} = 4.5\text{ V}$ to 5.5 V (unless otherwise noted)⁽¹⁾

PARAMETER		TEST CONDITIONS	V_{CCA}	MIN	TYP ⁽²⁾	MAX	UNIT
V_{OH}		$I_{OH} = -100\text{ }\mu\text{A}$	4.5 V	4.3			V
			5.5 V	5.3			
		$I_{OH} = -24\text{ mA}$	4.5 V	3.7			
			5.5 V	4.7			
V_{OL}		$I_{OL} = 100\text{ }\mu\text{A}$	4.5 V			0.2	V
			5.5 V			0.2	
		$I_{OL} = 24\text{ mA}$	4.5 V			0.55	
			5.5 V			0.55	
I_I	Control inputs	$V_I = V_{CCA}$ or GND	5.5 V			± 1	μA
I_{OZ} ⁽³⁾	A port	$V_O = V_{CCA}$ or GND	5.5 V			± 5	μA
I_{CCA}		$V_I = V_{CCA}$ or GND, $I_O = 0$	5.5 V			80	μA
ΔI_{CCA} ⁽⁴⁾		One input at 3.4 V, Other inputs at V_{CCA} or GND	5.5 V			1.5	mA
C_i	Control inputs	$V_I = V_{CCA}$ or GND	Open		5		pF
C_{io}	A port	$V_O = V_{CCA}$ or GND	5 V		11		pF

(1) $V_{CCB} = 2.7\text{ V}$ to 3.6 V .

(2) All typical values are measured at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

(3) For I/O ports, the parameter I_{OZ} includes the input leakage current.

(4) This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or the associated V_{CC} .

6.8 Electrical Characteristics

over recommended operating free-air temperature range for $V_{CCB} = 2.7\text{ V}$ to 3.6 V (unless otherwise noted)⁽¹⁾

PARAMETER		TEST CONDITIONS	V_{CCB}	MIN	TYP ⁽⁴⁾	MAX	UNIT
V_{OH}		$I_{OH} = -100\text{ }\mu\text{A}$	2.7 V to 3.6 V	$V_{CC} - 0.2$			V
			2.7 V	2.2			
		$I_{OH} = -12\text{ mA}$	3 V	2.4			
			3 V	2			
V_{OL}		$I_{OL} = 100\text{ }\mu\text{A}$	2.7 V to 3.6 V			0.2	V
		$I_{OL} = 12\text{ mA}$	2.7 V			0.4	
		$I_{OL} = 24\text{ mA}$	3 V			0.55	
I_{OZ} ⁽²⁾	B port	$V_O = V_{CCB}$ or GND	3.6 V			± 5	μA
I_{CCB}		$V_I = V_{CCB}$ or GND, $I_O = 0$	3.6 V			50	μA
ΔI_{CCB} ⁽³⁾		One input at $V_{CCB} - 0.6\text{ V}$, Other inputs at V_{CCB} or GND	2.7 V to 3.6 V			0.5	mA
C_{io}	B port	$V_O = V_{CCB}$ or GND	3.3 V		11		pF

(1) $V_{CCA} = 5\text{ V} \pm 0.5\text{ V}$.

(2) For I/O ports, the parameter I_{OZ} includes the input leakage current.

(3) This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or the associated V_{CC} .

(4) All typical values are measured at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

6.9 Switching Characteristics

over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figure 7-1 and Figure 7-2)

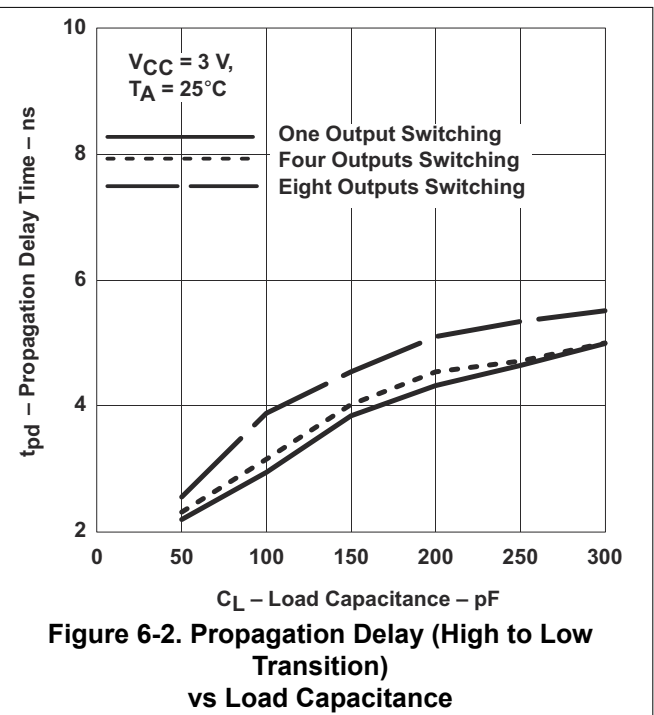
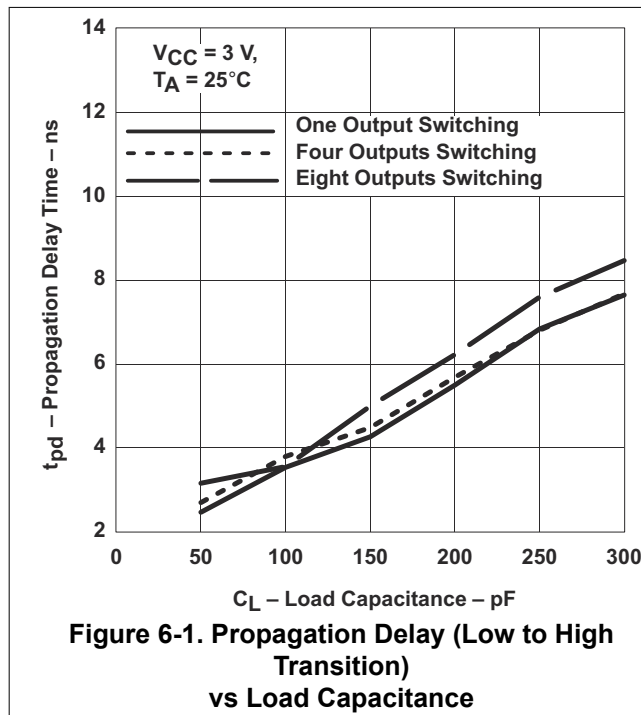
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCA} = 5\text{ V} \pm 0.5\text{ V}$, $V_{CCB} = 2.7\text{ V to } 3.6\text{ V}$		UNIT
			MIN	MAX	
t_{PHL}	A	B	1	6.3	ns
t_{PLH}			1	6.7	
t_{PHL}	B	A	1	6.1	ns
t_{PLH}			1	5	
t_{PZL}	\overline{OE}	A	1	9	ns
t_{PZH}			1	10	
t_{PZL}	\overline{OE}	B	1	10.3	ns
t_{PZH}			1	9.8	
t_{PLZ}	\overline{OE}	A	1	7	ns
t_{PHZ}			1	5.8	
t_{PLZ}	\overline{OE}	B	1	7.7	ns
t_{PHZ}			1	7.8	

6.10 Operating Characteristics

$V_{CCA} = 4.5\text{ V to } 5.5\text{ V}$, $V_{CCB} = 2.7\text{ V to } 3.6\text{ V}$, $T_A = 25^\circ\text{C}$

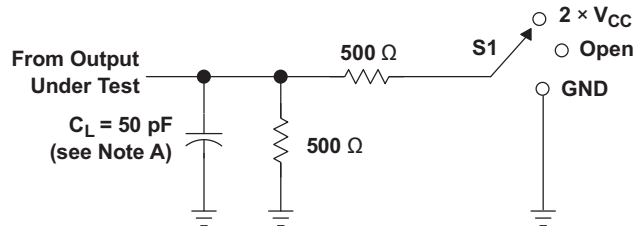
PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	$C_L = 0$, $f = 10\text{ MHz}$	39.5	pF
		Outputs disabled		5	

6.11 Typical Characteristics



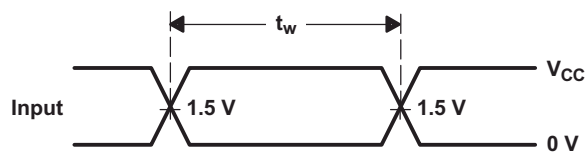
7 Parameter Measurement Information

7.1 A Port

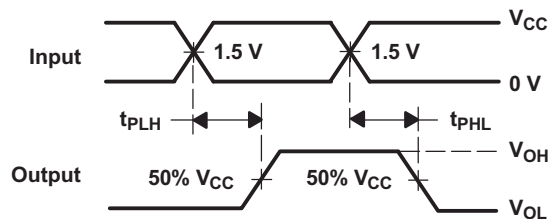


LOAD CIRCUIT

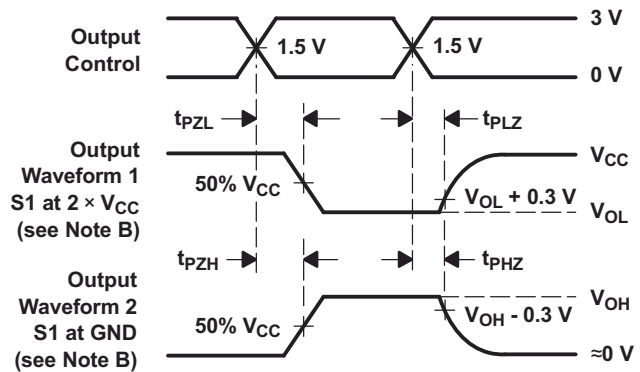
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
NONINVERTING OUTPUTS

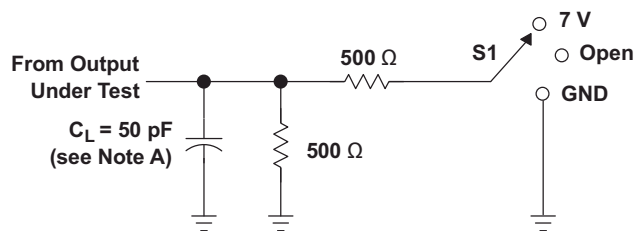


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
 D. The outputs are measured one at a time, with one transition per measurement.
 E. All parameters and waveforms are not applicable to all devices.

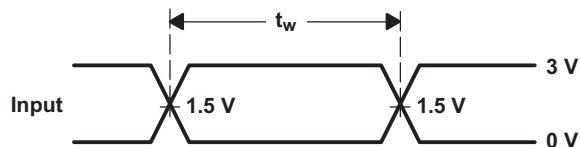
Figure 7-1. Load Circuit and Voltage Waveforms

7.2 B Port

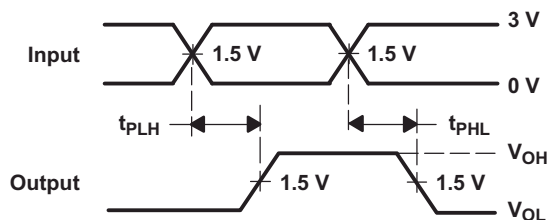


LOAD CIRCUIT

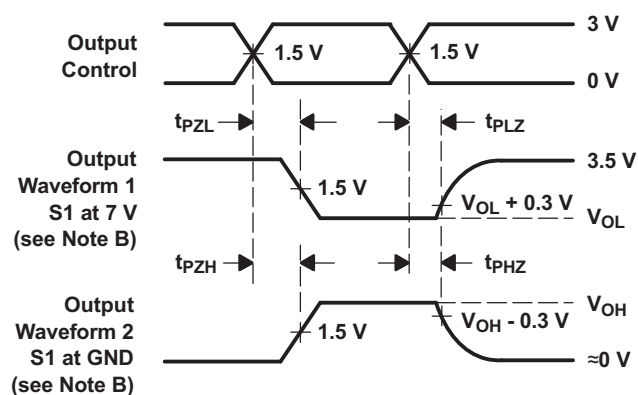
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

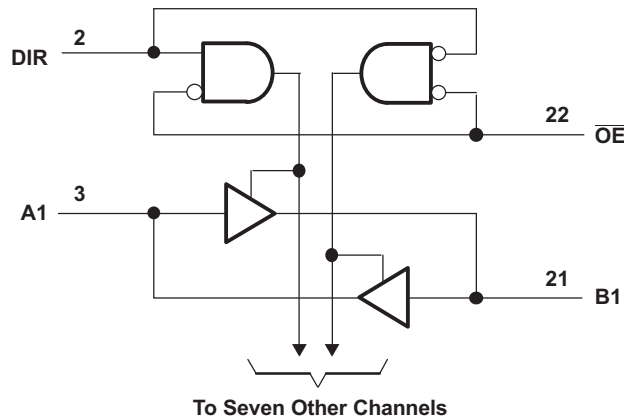
Figure 7-2. Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

SN74LVC4245A is an 8-bit (octal) noninverting bus transceiver contains two separate supply rails; B port has V_{CCB} , which is set at 3.3 V, and A port has V_{CCA} , which is set at 5 V. This allows for translation from a 3.3-V to a 5-V environment, and vice versa, designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable (\overline{OE}) input can be used to disable the device so the buses are effectively isolated. The control circuitry (DIR, \overline{OE}) is powered by V_{CCA} .

8.2 Functional Block Diagram



8.3 Feature Description

- 24 mA drive at 3-V supply
 - Good for heavier loads and longer traces
- Low V_{IH}
 - Allows 3.3-V to 5-V translation

8.4 Device Functional Modes

Table 8-1. Function Table

INPUTS		OPERATION
\overline{OE}	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The SN74LVC4245A device pinout allows the designer to switch to a normal all-3.3-V or all-5-V 20-pin '245 device without board re-layout. The designer uses the data paths for pins 2–11 and 14–23 of the SN74LVC4245A to align with the conventional SN74LVC4245 device's pinout. SN74LVC4245A is a high drive CMOS device that can be used for a multitude of bus interface type applications where output drive or PCB trace length is a concern.

9.2 Typical Application

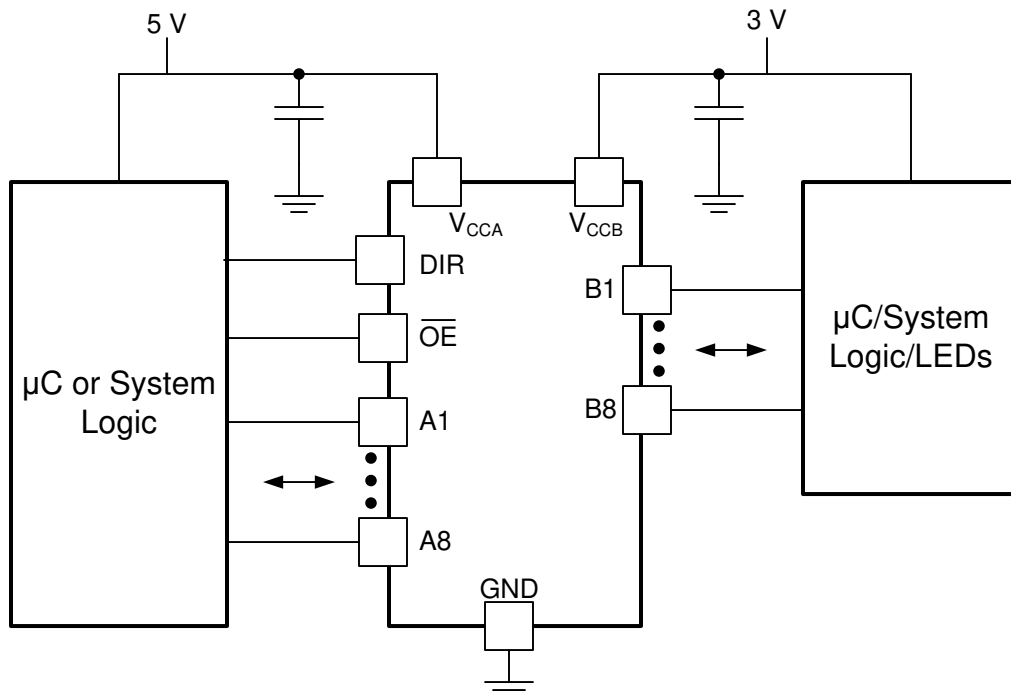


Figure 9-1. Typical Application Schematic

9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so routing and load conditions should be considered to prevent ringing.

9.2.2 Detailed Design Procedure

1. Recommended Input Conditions:
 - For rise time and fall time specifications, see $(\Delta t/\Delta V)$ in the [Section 6.4](#) table.
 - For specified high and low levels, see $(V_{IH}$ and $V_{IL})$ in the [Section 6.4](#) table.
2. Recommend Output Conditions:
 - Load currents should not exceed $(I_O \text{ max})$ per output and should not exceed (Continuous current through V_{CC} or GND) total current for the part. These limits are located in the [Section 6.1](#) table.
 - Outputs should not be pulled above V_{CC} .
 - Series resistors on the output may be used if the user desires to slow the output edge signal or limit the output current.

9.2.3 Application Curves

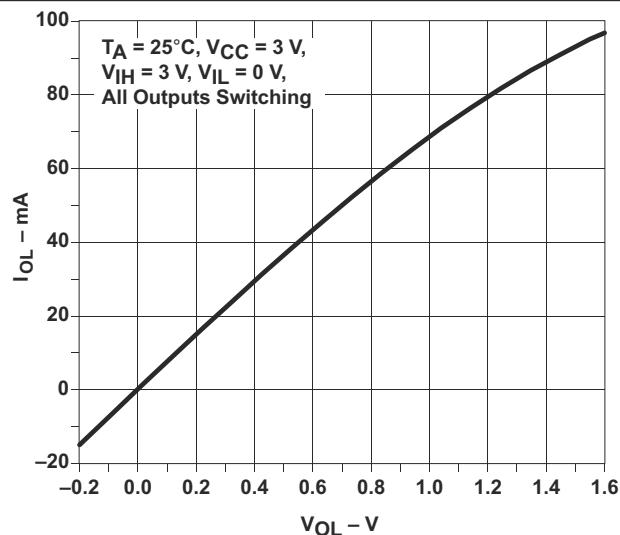


Figure 9-2. Output Drive Current (I_{OL}) vs LOW-level Output Voltage (V_{OL})

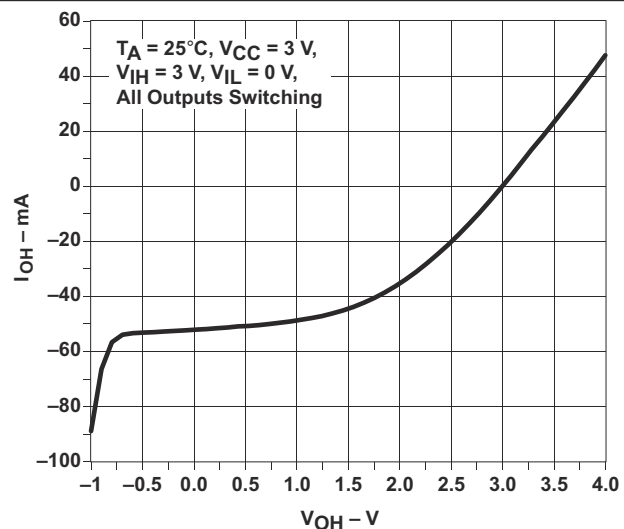


Figure 9-3. Output Drive Current (I_{OH}) vs HIGH-level Output Voltage (V_{OH})

10 Power Supply Recommendations

10.1 Power-Up Consideration

TI level-translation devices offer an opportunity for successful mixed-voltage signal design. A proper power-up sequence always should be followed to avoid excessive supply current, bus contention, oscillations, or other anomalies caused by improperly biased device terminals. Take these precautions to guard against such power-up problems:

1. Connect ground before any supply voltage is applied.
2. Power up the control side of the device (V_{CCA} for all four of these devices).
3. Tie \overline{OE} to V_{CCA} with a pullup resistor so that it ramps with V_{CCA} .
4. Depending on the direction of the data path, DIR can be high or low. If DIR high is needed (A data to B bus), ramp it with V_{CCA} . Otherwise, keep DIR low.

For more information, refer to the [Voltage-Level-Translation Devices](#) application note.

11 Layout

11.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in [Figure 11-1](#) are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} , whichever makes more sense or is more convenient.

11.2 Layout Example

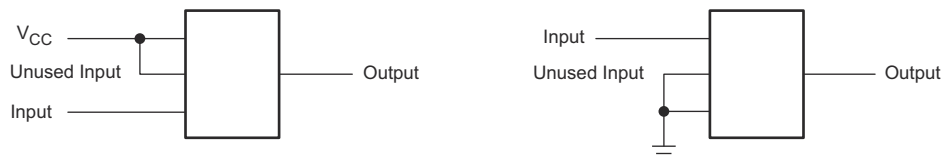


Figure 11-1. Layout Diagram

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [Voltage-Level-Translation Devices application note](#)

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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