Self-Protected Low Side Driver with Temperature and Current Limit

65 V, 7.0 A, Single N-Channel

NCV8406A, NCV8406B

NCV8406A/B is a three terminal protected Low-Side Smart Discrete device. The protection features include overcurrent, overtemperature, ESD and integrated Drain-to-Gate clamping for overvoltage protection. This device offers protection and is suitable for harsh automotive environments.

Features

- Short Circuit Protection
- Thermal Shutdown with Automatic Restart
- Over Voltage Protection
- Integrated Clamp for Inductive Switching
- ESD Protection
- dV/dt Robustness
- Analog Drive Capability (Logic Level Input)
- These Devices are Faster than the Rest of the NCV Devices
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

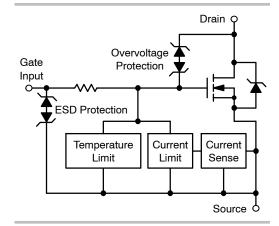
- Switch a Variety of Resistive, Inductive and Capacitive Loads
- Can Replace Electromechanical Relays and Discrete Circuits
- Automotive / Industrial

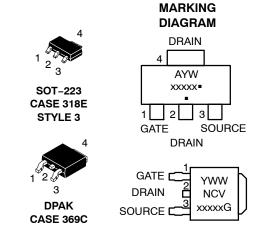


ON Semiconductor®

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V _{DSS} (Clamped)	R _{DS(on)} TYP	I _D TYP (Limited)
65 V	210 m Ω	7.0 A





A = Assembly Location

Y = Year W, WW = Work Week

1

xxxxx = 8406A or 8406B
G or = = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 10 of this data sheet.

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage Internally Clamped	V _{DSS}	60	Vdc
Gate-to-Source Voltage	V_{GS}	±14	Vdc
Drain Current Continuous	I _D	Internally Limited	
Total Power Dissipation – SOT–223 Version @ T _A = 25°C (Note 1) @ T _A = 25°C (Note 2)	P _D	1.25 1.81	W
Total Power Dissipation – DPAK Version @ T _A = 25°C (Note 1) @ T _A = 25°C (Note 2)	P _D	1.31 2.31	W
Thermal Resistance – SOT–223 Version Junction–to–Soldering Point Junction–to–Ambient (Note 1) Junction–to–Ambient (Note 2)	R _{θJS} R _{θJA} R _{θJA}	7.0 100 69	°C/W
Thermal Resistance – DPAK Version Junction-to-Soldering Point Junction-to-Ambient (Note 1) Junction-to-Ambient (Note 2)	R _θ Js R _θ JA R _θ JA	1.0 95 54	°C/W
Single Pulse Inductive Load Switching Energy (Starting $T_J = 25^{\circ}C$, $V_{DD} = 50$ Vdc, $V_{GS} = 5.0$ Vdc, $I_L = 2.1$ Apk, $L = 50$ mH, $R_G = 25~\Omega$)	E _{AS}	110	mJ
Load Dump Voltage (VGS = 0 and 10 V, RI = 2 Ω , RL = 7 Ω , td = 400 ms)	V_{LD}	75	V
Operating Junction Temperature Range	TJ	-40 to 150	°C
Storage Temperature Range	T _{stg}	-55 to 150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface mounted onto minimum pad size (100 sq/mm) FR4 PCB, 1 oz cu.

2. Mounted onto 1" square pad size (700 sq/mm) FR4 PCB, 1 oz cu.

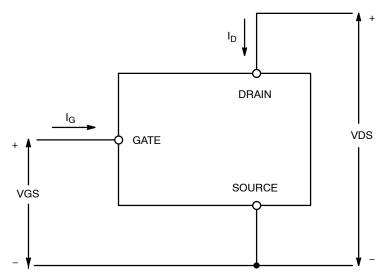


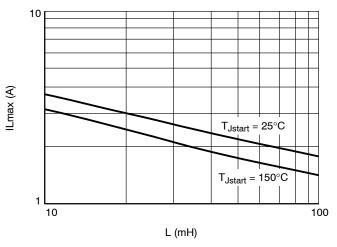
Figure 1. Voltage and Current Convention

$\textbf{MOSFET ELECTRICAL CHARACTERISTICS} \ (T_J = 25^{\circ}\text{C unless otherwise noted})$

Characteristic			Min	Тур	Max	Unit
OFF CHARACTERISTICS		<u></u>	ı			.1
Drain-to-Source Clamped Breakdown Voltage ($V_{GS} = 0 \text{ V}, I_D = 2 \text{ mA}$)			60	65	70	V
Zero Gate Voltage Drain Current (V _{DS} = 52 V, V _{GS} = 0 V)			_	22	100	μΑ
Gate Input Current (V _{GS} = 5.0 V, V _{DS} = 0 V)			-	30	100	μΑ
ON CHARACTERISTICS						
Gate Threshold Voltage ($V_{DS} = V_{GS}, I_D = 150 \mu A$) Threshold Temperature Coeffi	cient	V _{GS(th)}	1.2 -	1.66 4.0	2.0 _	V -mV/°C
Static Drain-to-Source On-Resistance (Note 3) ($V_{\rm GS}$ = 10 V, $I_{\rm D}$ = 2.0 A, $T_{\rm J}$ @ 25°C)			_	185	210	mΩ
Static Drain-to-Source On-Resistance (Note 3) ($V_{GS} = 5.0 \text{ V}$, $I_D = 2.0 \text{ A}$, $T_J @ 25^{\circ}\text{C}$) ($V_{GS} = 5.0 \text{ V}$, $I_D = 2.0 \text{ A}$, $T_J @ 150^{\circ}\text{C}$)			- -	210 445	240 520	mΩ
Source-Drain Forward On Voltage (I _S = 7.0 A, V _{GS} = 0 V)			_	0.9	1.1	V
SWITCHING CHARACTERIS	TICS (Note 6)	•		•		
Turn-on Delay Time	$R_L = 6.6~\Omega, V_{in} = ~0~to~10~V, \ V_{DD} = 13.8~V, I_D = 2.0~A, ~10\%~V_{in}~to~10\%~I_D$	td _(on)	_	127	-	ns
Turn-on Rise Time	R_L = 6.6 Ω , V_{in} = 0 to 10 V, V_{DD} = 13.8 V, I_D = 2.0 A, 10% I_D to 90% I_D	t _{rise}	-	486	-	ns
Turn-off Delay Time	$R_L = 6.6~\Omega, V_{in} = ~0~to~10~V, \ V_{DD} = 13.8~V, I_D = 2.0~A, 90\%~V_{in}~to~90\%~I_D$	td _(off)	_	1600	_	ns
Turn-off Fall Time	$R_L = 6.6 \ \Omega, \ V_{in} = 0 \ to \ 10 \ V, \ V_{DD} = 13.8 \ V, \ I_D = 2.0 \ A, \ 90\% \ I_D \ to \ 10\% \ I_D$	t _{fall}	-	692	-	ns
Slew Rate ON	$R_L = 6.6~\Omega, V_{in} = ~0~to~10~V, \ V_{DD} = 13.8~V, I_D = 2.0~A, 70\%~to~50\%~V_{DD}$	dV _{DS} /dT _{on}	_	79	-	V/μs
Slew Rate OFF	R_L = 6.6 Ω , V_{in} = 0 to 10 V, V_{DD} = 13.8 V, I_D = 2.0 A, 50% to 70% V_{DD}	dV _{DS} /dT _{off}	-	27	-	V/μs
SELF PROTECTION CHARAC	CTERISTICS (Note 4)					
Current Limit	$\begin{split} &V_{DS} = 10 \text{ V, } V_{GS} = 5.0 \text{ V, } T_J = 25^{\circ}\text{C (Note 5)} \\ &V_{DS} = 10 \text{ V, } V_{GS} = 5.0 \text{ V, } T_J = 150^{\circ}\text{C (Notes 5, 6)} \\ &V_{DS} = 10 \text{ V, } V_{GS} = 10 \text{ V, } T_J = 25^{\circ}\text{C (Notes 5)} \end{split}$	I _{LIM}	5.0 3.5 6.5	7.0 4.5 8.5	9.5 6.0 10.5	А
Temperature Limit (Turn-off)	V _{GS} = 5.0 V (Note 6)	T _{LIM(off)}	150	180	200	°C
Thermal Hysteresis	V _{GS} = 5.0 V	$\Delta T_{LIM(on)}$	-	10	-	°C
Temperature Limit (Turn-off)	Turn-off) V _{GS} = 10 V (Note 6)		150	180	200	°C
Thermal Hysteresis	V _{GS} = 10 V	$\Delta T_{LIM(on)}$	-	20	-	°C
Input Current during $V_{DS} = 0 \text{ V}, V_{GS} = 5.0 \text{ V}, T_J = T_J > T_{\text{(fault)}} \text{ (Note 6)}$ Thermal Fault $V_{DS} = 0 \text{ V}, V_{GS} = 10 \text{ V}, T_J = T_J > T_{\text{(fault)}} \text{ (Note 6)}$		I _{g(fault)}	- -	5.9 12.3	-	mA
ESD ELECTRICAL CHARACT	ERISTICS	•	<u>-</u>	-	<u>-</u>	-
Electro-Static Discharge Capability Human Body Model (HBM) Machine Model (MM)		ESD	6000 500	_ _	_ _	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions. 3. Pulse Test: Pulse Width \leq 300 μ s, Duty Cycle \leq 2%.

- 4. Fault conditions are viewed as beyond the normal operating range of the part.
- Current limit measured at 380 μs after gate pulse.
 Not subject to production test.



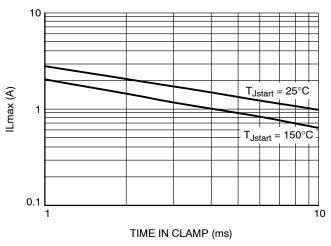
1000 T_{Jstart} = 25°C

T_{Jstart} = 150°C

T_{Jstart} = 150°C

Figure 2. Single Pulse Maximum Switch-off Current vs. Load Inductance

Figure 3. Single-Pulse Maximum Switching Energy vs. Load Inductance



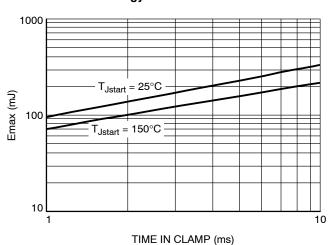
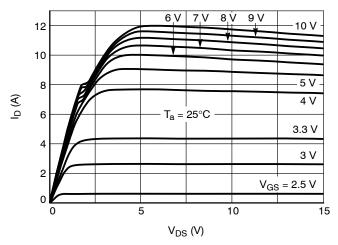


Figure 4. Single Pulse Maximum Inductive Switch-off Current vs. Time in Clamp

Figure 5. Single-Pulse Maximum Inductive Switching Energy vs. Time in Clamp



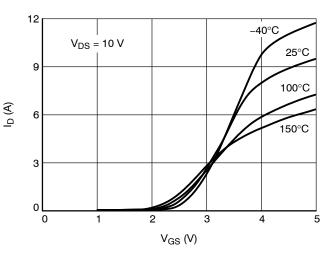


Figure 6. On-state Output Characteristics

Figure 7. Transfer Characteristics

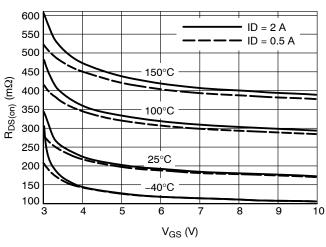


Figure 8. R_{DS(on)} vs. Gate-Source Voltage

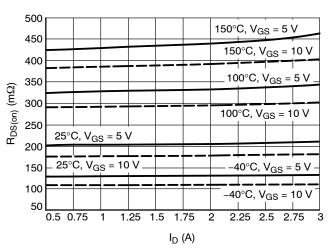


Figure 9. R_{DS(on)} vs. Drain Current

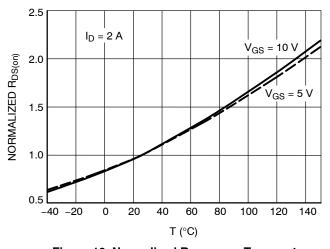


Figure 10. Normalized $R_{DS(on)}$ vs. Temperature

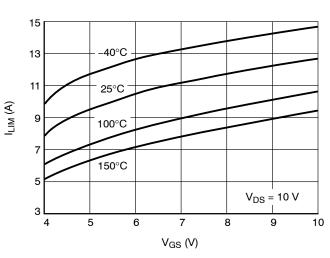


Figure 11. Current Limit vs. Gate-Source Voltage

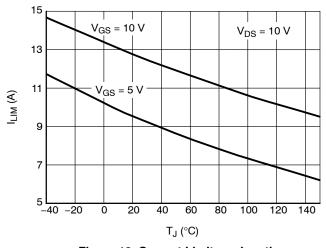


Figure 12. Current Limit vs. Junction Temperature

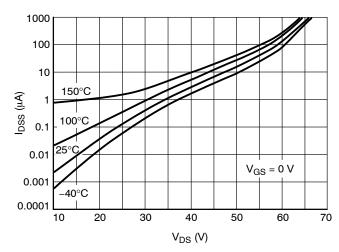
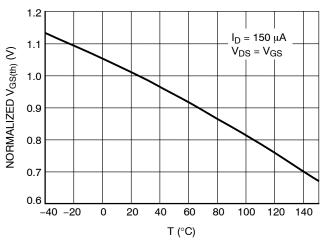


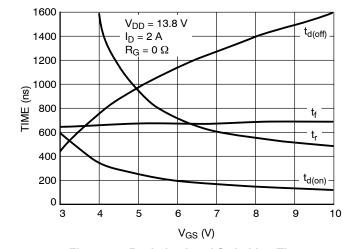
Figure 13. Drain-to-Source Leakage Current



1100 1000 -40°C 900 V_{SD} (mV) 25°C 800 100°C 700 150°C 600 $V_{GS} = 0 V$ 500 2 3 4 5 6 8 I_S (A)

Figure 14. Normalized Threshold Voltage vs. Temperature

Figure 15. Source-Drain Diode Forward Characteristics



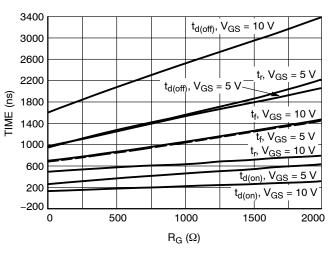


Figure 16. Resistive Load Switching Time vs.
Gate-Source Voltage

Figure 17. Resistive Load Switching Time vs.
Gate Resistance

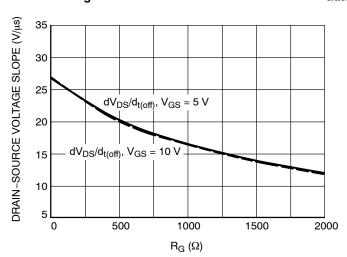


Figure 18. Drain-Source Voltage Slope during Turn On and Turn Off vs. Gate Resistance

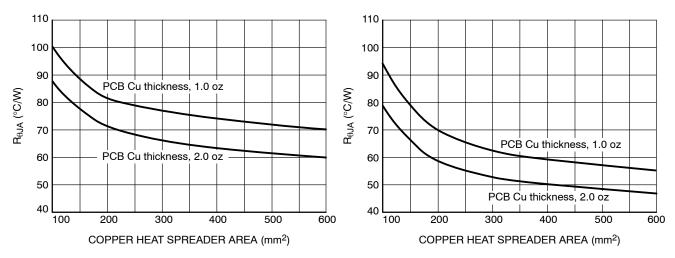


Figure 19. $R_{\theta JA}$ vs. Copper Area – SOT–223

Figure 20. $R_{\theta JA}$ vs. Copper Area – DPAK

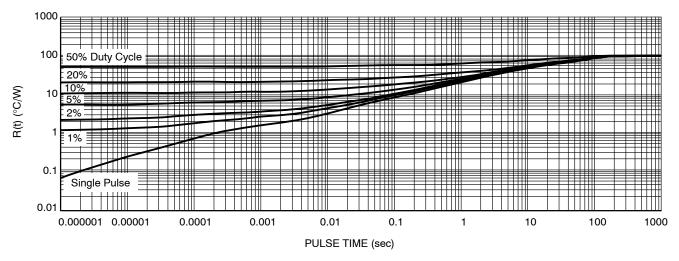


Figure 21. Transient Thermal Resistance - SOT-223 Version

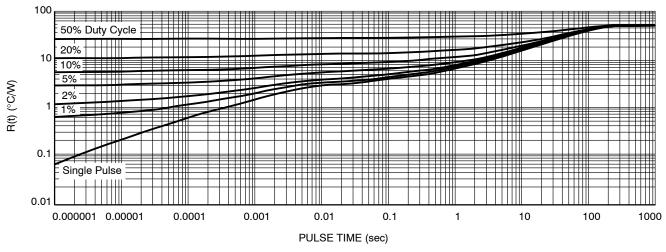


Figure 22. Transient Thermal Resistance - DPAK Version

TEST CIRCUITS AND WAVEFORMS

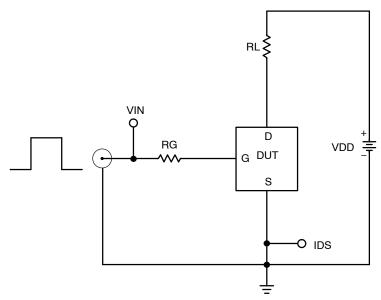


Figure 23. Resistive Load Switching Test Circuit

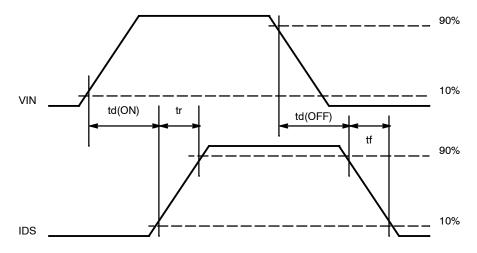


Figure 24. Resistive Load Switching Waveforms

TEST CIRCUITS AND WAVEFORMS

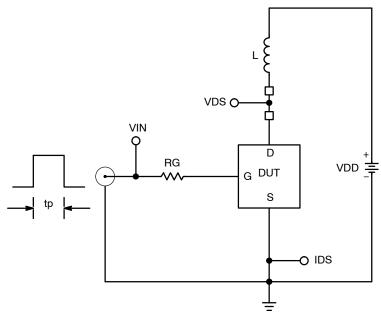


Figure 25. Inductive Load Switching Test Circuit

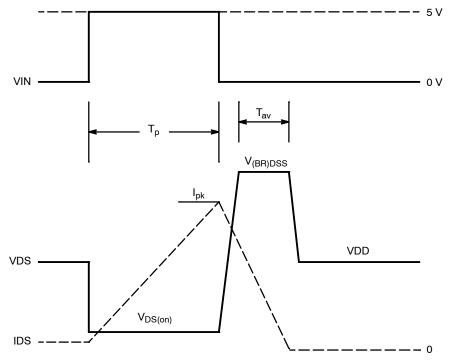


Figure 26. Inductive Load Switching Waveforms

ORDERING INFORMATION

Device	Package	Shipping [†]
NCV8406ASTT1G	SOT-223 (Pb-Free)	1000 / Tape & Reel
NCV8406ASTT3G	SOT-223 (Pb-Free)	4000 / Tape & Reel
NCV8406ADTRKG	DPAK (Pb-Free)	2500 / Tape & Reel
NCV8406BDTRKG	DPAK (Pb-Free)	2500 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



DPAK (SINGLE GAUGE) CASE 369C **ISSUE F** SCALE 1:1 Α <-b3 В L3 Z ۩ **DETAIL A** Ш NOTE 7 C → **BOTTOM VIEW** h2 e SIDE VIEW ⊕ 0.005 (0.13) M C **TOP VIEW** Z H L2 GAUGE C SEATING PLANE

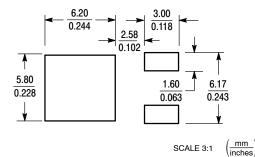


STYLE 6: STYLE 7: STYLE 8: STYLE 9: STYLE 10: PIN 1. MT1 2. MT2 PIN 1. GATE 2. COLLECTOR PIN 1. N/C 2. CATHODE PIN 1. ANODE 2. CATHODE PIN 1. CATHODE 2. ANODE 3. GATE 4. MT2 3. EMITTER 4. COLLECTOR 3. ANODE 4. CATHODE 3. RESISTOR ADJUST 4. CATHODE 3. CATHODE 4. ANODE

SOLDERING FOOTPRINT*

Α1

DETAIL A ROTATED 90° CW



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DATE 21 JUL 2015

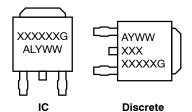
NOTES:

- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 CONTROLLING DIMENSION: INCHES.
- 3. THERMAL PAD CONTOUR OPTIONAL WITHIN DI-
- MENSIONS b3, L3 and Z.
 4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
 5. DIMENSIONS D AND E ARE DETERMINED AT THE
- OUTERMOST EXTREMES OF THE PLASTIC BODY.

 6. DATUMS A AND B ARE DETERMINED AT DATUM
- 7. OPTIONAL MOLD FEATURE.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
Α	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.028	0.045	0.72	1.14
b3	0.180	0.215	4.57	5.46
С	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
Е	0.250	0.265	6.35	6.73
е	0.090 BSC		2.29 BSC	
Н	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.114 REF		2.90	REF
L2	0.020 BSC		0.51	BSC
L3	0.035	0.050	0.89	1.27
L4		0.040		1.01
Z	0.155		3.93	

GENERIC MARKING DIAGRAM*



XXXXXX = Device Code = Assembly Location Α L = Wafer Lot Υ = Year WW = Work Week = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	DPAK (SINGLE GAUGE)		PAGE 1 OF 1	

BOTTOM VIEW

ALTERNATE CONSTRUCTIONS

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