T31A

Smart Video Application Processor

Data Sheet

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北京君正集成电路股份有限公司
Ingenic Semiconductor Co.,Ltd.

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1 Overview

T31A is a smart video application processor targeting for video devices like mobile camera, security survey, video talking, video analysis and so on. This SoC introduces a kind of innovative architecture to fulfill both high performance computing and high quality image and video encoding requirements addressed by video devices. T31A provides high-speed CPU computing power, excellent image signal process, fluent 2048x2048 resolution video recording.

The CPU (Central Processing Unit) core, equipped with 32kB instruction and 32kB data L1 cache, and 128kB L2 cache, operating at 1.5GHz, and full feature MMU function performs OS related tasks. At the heart of the CPU core is XBurst® processor engine. XBurst® is an industry leading microprocessor core which delivers superior high performance and best-in-class low power consumption. A hardware floating-point unit which compatible with IEEE754 is also included.

The VPU (Video Processing Unit) core is a video encoder engine designed to process video streams using the HEVC(ISO/IEC 23008-2 High Efficiency Video Coding) and AVC(ISO/IEC 14496-10 Advanced Video Coding) standards. It also supports still picture encoding using the JPEG standard(ITU T.81). Together with the on chip video accelerating engine and post image processing unit, T31A delivers high video performance. The maximum resolution of 2592x2048 in the format of AVC are supported in encoding. up to 40Mbit/s, 2592x1920@25fps.

The ISP (Image signal processor) core supports excellent image process with the image from raw sensors. It supports DVP,BT and MIPI interface. With the functions, such as 3A, 2D and 3D denoise, WDR/HDR, lens shading, it can supply maximum resolution 2592x2048 resolution image for view or encoding to store or transfer.

For more quickly and easily to use T31A, 1G bit DDR3L is integrated on chip.

On-chip modules such as audio CODEC, multi-channel SAR-ADC controller and camera interface offer designers a economical suite of peripherals for video application. WLAN, Bluetooth and expansion options are supported through high-speed SPI and MMC/SD/SDIO host controllers. Other peripherals such as USB OTG, MAC, UART and SPI as well as general system resources provide enough computing and connectivity capability for many applications.

1.1 Block Diagram

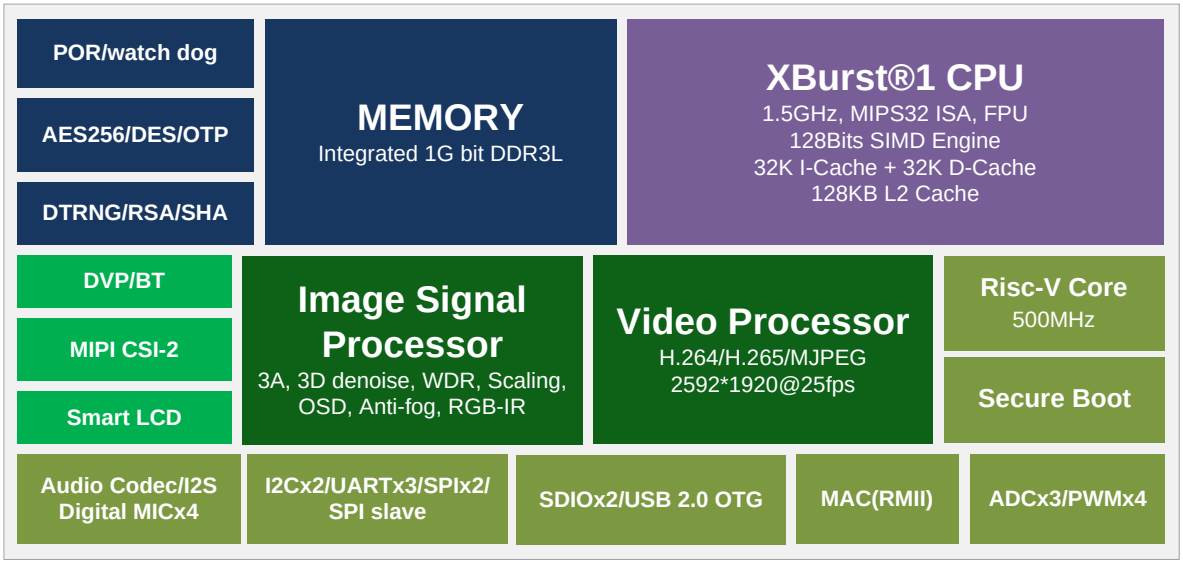


Figure 1-1 T31A Diagram

1.2 Features

1.2.1 CPU

- XBurst®-1 core
  - XBurst® FPU instruction set supporting both single and double floating point format which are IEEE754 compatible
  - XBurst® 9-stage pipeline micro-architecture, the operating frequency is 1.5GHz
- MMU
  - 32-entry joint-TLB
  - 8 entry instruction TLB
  - 8 entry data TLB
- L1 Cache
  - 32kB instruction cache
  - 32kB data cache
- Hardware debug support
- 16kB tight coupled memory
- L2 Cache
  - 128kB unify cache

1.2.2 Video Processor Unit

- Support DVT HEVC/AVC/JPEG Encoder
- Support HEVC up to 20Mbit/s and AVC up to 40Mbit/s, maximum frame rate is 1920x1080@60fps or 2592x1900@25fps

- maximum size up to 2592x4096 resolution

1.2.3 Image Signal Processor

- Dynamic/Static Defect Pixel Correction
- Green Equalization
- Black Level Correction
- Lens Shading Correction
- 3A(Auto Exposure/Auto White Balance/Auto Focus)
- Support Statistical Information Output(3A)
- Adaptive Dynamic Range Compression
- Demosaic
- Sharpen
- Bayer Denoise
- 2D/3D Denosie
- Color Noise Suppression
- Lens Distortion Correction
- 2D Color Correction
- 3D Color Correction
- Gamma Correction
- Defog, WDR
- 3 Independent Image Scaler and Output
- Crop, Mirror and Flip
- Support Maximum Resolution:2592x2048

1.2.4 Smart LCD Controller

- Basic Features
  - Display size up to 800x600@60Hz,24BPP
  - Smart LCD interface 6800(type A) and 8080(type B)
- Colors Supports
  - Support up to 16,777,216 (16M) colors
- Panel Supports
  - transmit 565 by two cycle via SLCD 8bit data interface
  - transmit 888 by three cycle via SLCD 8bit data interface
  - Supports different size of display panel
  - Supports internal DMA operation and direct write register operation

1.2.5 Video input

- Support 8/10/12 bit RGB Bayer input
- Support DVP, BT1120(serial mode)/BT656/BT601 and MIPI CSI(2 lane up to 1.5Gbps)
- Support maximum: 2592x1900@25fps

- Support single-sensor input

1.2.6 Audio System

- Integrated Audio codec
  - 24 bits DAC with 93dB SNR
  - 24 bits ADC with 92dB SNR
  - Support signal-ended and differential microphone input and line input
  - Automatic Level Control (ALC) for smooth audio recording
  - Pure logic process: no need for mixed signal layers and less mask cost
  - Programmable input and output analog gains
  - Digital interpolation and decimation filter integrated
  - Sampling rate 8K/12K/16K/24K/32/44.1K/48K/96K
- Low power DMIC Controller
  - 16bit data interface and 20bit precision internal controller
  - SNR:90dB,THD:-90dB@FS -20dB
  - Linear high pass filter include. Attenuation:-2.9dB@100Hz,22dB@27Hz,-36dB@10Hz
  - Low power voice trigger when waiting to start talking
  - 1/2/3/4 channel digital MIC support
  - Support voice data pre-fetch when trigger enable and the data interface disable, but do not increase the power dissipation
  - Sample frequency supported:8k,16k
- I2S Interface
  - Support standard interface protocol

1.2.7 Memory Interface

- Integrated 1G bit DDR3L on chip
- Static memory interface
  - Support 6 external chip selection CS6~1#. Each bank can be configured separately
  - The size and base address of static memory banks are programmable
  - Direct interface to 8-bit bus width external memory interface devices or external static memory to each bank. Read/Write strobe setup time and hold time periods can be programmed and inserted in an access cycle to enable connection to low-speed memory
  - Wait insertion by WAIT pin
  - Automatic wait cycle insertion to prevent data bus collisions in case of consecutive memory accesses to different banks, or a read access followed by a write access to the same bank

1.2.8 System Functions

- Clock generation and power management
  - On-chip 12/24/27/50MHZ oscillator circuit

- One three-chip phase-locked loops (PLL) with programmable multiplier
- CCLK, HHCLK, H2CLK, PCLK, H0CLK, DDR_CLK, VPU_CLK frequency can be changed separately for software by setting registers
- SSI clock supports 50M clock
- MSC clock supports 100M clock
- Functional-unit clock gating
- Shut down power supply for P0, ISP, VPU, IPU

- Timer and counter unit with PWM output and/or input edge counter
  - Provide four separate channels, six of them have input signal transition edge counter
  - 16-bit A counter and 16-bit B counter with auto-reload function every channel
  - Support interrupt generation when the A counter underflow
  - Three clock sources: RTCLK (real time clock), EXCLK (external clock input), PCLK (APB Bus clock) selected with 1, 4, 16, 64, 256 and 1024 clock dividing selected
  - Every channel has PWM output
- OS timer controller
  - 64-bit counter and 32-bit compare register
  - Support interrupt generation when the counter matches the compare register
  - Two clock sources: RTCLK (real time clock), HCLK (system bus clock) selected with 1, 4, 16, 64, 256 and 1024 clock dividing selected
- Interrupt controller
  - Total 64 interrupt sources
  - Each interrupt source can be independently enabled
  - Priority mechanism to indicate highest priority interrupt
  - All the registers are accessed by CPU
  - Unmasked interrupts can wake up the chip in sleep mode
  - Another set of source, mask and pending registers to serve for PDMA
- Watchdog timer
  - Generates WDT reset
  - A 16-bit Data register and a 16-bit counter
  - Counter clock uses the input clock selected by software
- PCLK, EXTAL and RTCCLK can be used as the clock for counter
- The division ratio of the clock can be set to 1, 4, 16, 64, 256 and 1024 by software
- Direct memory access controllers
  - Support up to 32 independent DMA channels
  - Descriptor or No-Descriptor Transfer mode compatible with previous JZ SoC
  - Transfer data units: 1-byte, 2-byte, 4-byte, 16-byte, 32-byte, 64-byte, 128-byte
  - Transfer number of data unit: 1 ~ 2^{24} - 1
  - Independent source and destination port width: 8-bit, 16-bit, 32-bit
  - Fixed three priorities of channel groups: 0~3, highest; 4~11: mid; 12~31: lowest
  - An extra INTC IRQ can be bound to one programmable DMA channel
- SAR A/D Controller
  - three Channels
  - Resolution: 10-bit

- Integral nonlinearity: ±1 LSB
- Differential nonlinearity: ±0.5 LSB
- Resolution/speed: up to 2MSPS
- Max Frequency: 24MHz
- Low power dissipation: 1.5mW(worst)
- Support multi-touch detect
- Support write control command by software
- Single-end and Differential Conversion Mode
- Support external touch screen controller
- Pin Description

- OTP Slave Interface
  - Total 1024 bits. Lower 192bits are read only, other higher bits are read-able and write-able

1.2.9 Peripherals

- General-Purpose I/O ports
  - Each port can be configured as an input, an output or an alternate function port
  - Each port can be configured as an interrupt source of low/high level or rising/falling edge triggering. Every interrupt source can be masked independently
  - Each port has an internal pull-up or pull-down resistor connected. The pull-up/down resistor can be disabled
  - GPIO output 3 interrupts, each interrupt corresponds to the group, to INTC

- SMB Controller
  - Two-wire SMB serial interface – consists of a serial data line (SDA) and a serial clock (SCL)
  - Two speeds
    - Standard mode (100 Kb/s)
    - Fast mode (400 Kb/s)
  - Device clock is identical with pclk
  - Programmable SCL generator
  - Master or slave SMB operation
  - 7-bit addressing/10-bit addressing
  - 16-level transmit and receive FIFOs
  - Interrupt operation
  - The number of devices that you can connect to the same SMB-bus is limited only by the maximum bus capacitance of 400pF
  - APB interface
  - 2 independent SMB channels (SMB0, SMB1)

- One High Speed Synchronous serial interfaces (SFC)
  - 3 protocols support: National’s Microwire, TI’s SSP, and Motorola’s SPI

- transmit-only or receive-only operation
- MSB first for command and data transfer, and LSB first for address transfer
- 64 entries x 32 bits wide data FIFO
- one device select
- Configurable sampling point for reception
- Configurable timing parameters: t_{SLCH}, t_{CHSH} and t_{SHSL}
- Configurable flash address wide are supported
- 7 transfer formats: Standard SPI, Dual-Output/Dual-Input SPI, Quad-Output/Quad-Input SPI, Dual-I/O SPI, Quad-I/O SPI, Full Dual-I/O SPI, Full Quad-I/O SPI
- two data transfer mode: slave mode and DMA mode
- Configurable 6 phases for software flow

- Two Normal Speed Synchronous serial interfaces (SSI0, SSI1)
  - 3 protocols support: National's Microwire, TI's SSP, and Motorola's SPI
  - Full-duplex or transmit-only or receive-only operation
  - Programmable transfer order: MSB first or LSB first
  - 128 entries deep x 32 bits wide transmit and receive data FIFOs
  - Configurable normal transfer mode or Interval transfer mode
  - Programmable clock phase and polarity for Motorola's SSI format
  - Two slave select signal (SSI_CE0_ / SSI_CE1_) supporting up to 2 slave devices
  - Back-to-back character transmission/reception mode
  - Loop back mode for testing

- Three UARTs (UART0, UART1, UART2)
  - Full-duplex operation
  - 5-, 6-, 7- or 8-bit characters with optional no parity or even or odd parity and with 1, 1½, or 2 stop bits
  - 64x8 bit transmit FIFO and 64x11bit receive FIFO
  - Independently controlled transmit, receive (data ready or timeout), line status interrupts
  - Internal diagnostic capability Loopback control and break, parity, overrun and framing-error is provided
  - Separate DMA requests for transmit and receive data services in FIFO mode
  - Supports modem flow control by software or hardware
  - Slow infrared asynchronous interface that conforms to IrDA specification

- Two MMC/SD/SDIO controllers (MSC0, MSC1)
  - Fully compatible with the MMC System Specification version 4.2
  - Support SD Specification 3.0
  - Support SD I/O Specification 1.0 with 1 command channel and 4 data channels
  - Consumer Electronics Advanced Transport Architecture (CE-ATA – version 1.1)
  - Maximum data rate is 50MBps
  - Support MMC data width 1bit and 4bit
  - Built-in programmable frequency divider for MMC/SD bus

- Built-in Special Descriptor DMA
- Maskable hardware interrupt for SDIO interrupt, internal status and FIFO status
- 128 x 32 built-in data FIFO
- Multi-SD function support including multiple I/O and combined I/O and memory
- IRQ supported enable card to interrupt MMC/SD controller
- Single or multi block access to the card including erase operation
- Stream access to the MMC card
- Supports SDIO read wait, interrupt detection during 1-bit or 4-bit access
- Supports CE-ATA digital protocol commands
- Support Command Completion Signal and interrupt to CPU
- Command Completion Signal disable feature
- The maximum block length is 4096bytes

- USB 2.0 OTG interface
  - Complies with the USB 2.0 standard for high-speed (480 Mbps) functions and with the On-The-Go supplement to the USB 2.0 specification
  - Operates either as the function controller of a high- /full-speed USB peripheral or as the host/peripheral in point-to-point or multi-point communications with other USB functions
  - Supports Session Request Protocol (SRP) and Host Negotiation Protocol (HNP)
  - UTMI+ Level 3 Transceiver Interface
  - Soft connect/disconnect
  - 16 Endpoints
  - Dedicate FIFO
  - Supports control, interrupt, ISO and bulk transfer

- Ethernet Media Access controller and interface
  - 10, 100Mbps data transfer rates with the following PHY interfaces:
    - RMII interface to communicate with an external Fast Ethernet PHY
  - Full-duplex operation:
    - IEEE 802.3x flow control automatic transmission of zero-quanta Pause frame on flow control input de-assertion
    - forwarding of received Pause frames to the user application
  - Half-duplex operation:
  - CSMA/CD Protocol support
  - Frame bursting and frame extension in 100 Mbps half-duplex operation
  - Preamble and start of frame data (SFD) insertion in Transmit path
  - Preamble and SFD deletion in the Receive path
  - Automatic CRC and pad generation controllable on a per-frame basis
  - Automatic Pad and CRC Stripping options for receive frames
  - Flexible address filtering modes, such as:
    - Up to 31 additional 48-bit perfect (DA) address filters with masks for each byte
    - 64-bit Hash filter for multicast and unicast (DA) addresses
    - Option to pass all multicast addressed frames

  - Promiscuous mode to pass all frames without any filtering for network monitoring
  - Pass all incoming packets (as per filter) with a status report
- Support Standard or Jumbo Ethernet frames with up to 2 KB of size
- IEEE 802.1Q VLAN tag detection for reception frames
- MDIO master interface for PHY device configuration and management
- CRC replacement, Source Address field insertion or replacement, and VLAN insertion, replacement, and deletion in transmitted frames with per-frame control
- Programmable watchdog timeout limit in the receive path
- Detect remote wake-up frames and AMD magic packets

- Digital True Random Number Generator（DTRNG）
  - Pure digital logic circuits
  - True random number
  - Interrupt mode and no interrupt mode

1.2.10 Bootrom

16kB Boot ROM memory

1.3 Characteristic

Item	Characteristic
Process Technology	22nm CMOS low power
Power supply voltage	General purpose I/O: 1.5~3.6V DDR I/O: 1.35V(DDR3L) ± 0.1V EFUSE programming: 1.8V ± 10% Analog power supply 1: 1.8V ± 10% Analog power supply 2: 3.3V ± 10% Core: 0.8V ± 0.1V
Package	BGA192
Operating frequency	1.5GHz

2 Packaging and Pinout Information

2.1 Overview

T31A processor is offered in BGA192, show in Figure 2-1. The T31A pin to ball assignment is show in Figure 2-2. The detailed pin description is listed in Table 2-1 ~ Table 2-16.

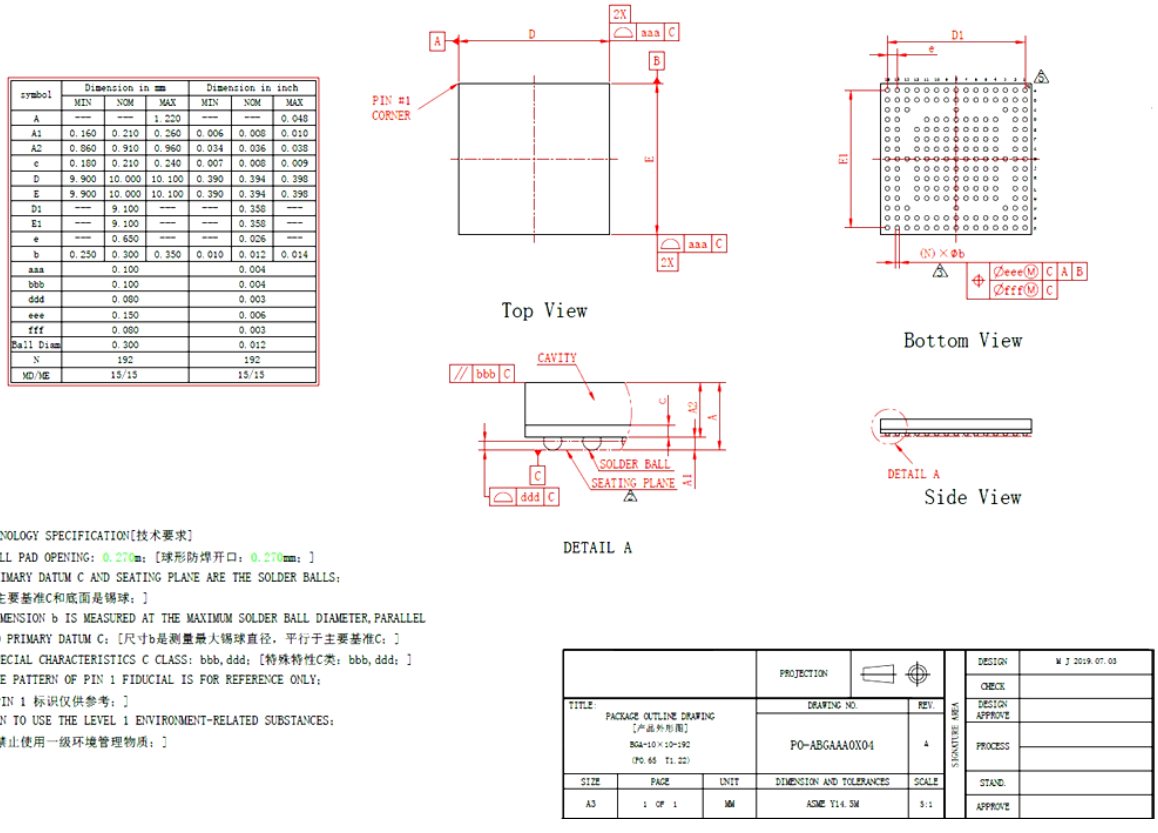
2.2 Solder Process

T31A package is lead-free. It's reflow profile follows the IPC/JEDEC lead-free reflow profile as contained in J-STD-020C.

2.3 Moisture Sensitivity Level

T31A package moisture sensitivity is level 3.

2.4 T31A Package



symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.220	---	---	0.048
A1	0.160	0.210	0.260	0.006	0.008	0.010
A2	0.860	0.910	0.960	0.034	0.036	0.038
c	0.180	0.210	0.240	0.007	0.008	0.009
D	9.900	10.000	10.100	0.390	0.394	0.398
E	9.900	10.000	10.100	0.390	0.394	0.398
D1	---	9.100	---	---	0.358	---
E1	---	9.100	---	---	0.358	---
e	---	0.650	---	---	0.026	---
b	0.250	0.300	0.350	0.010	0.012	0.014
aaa	0.100			0.004		
bbb	0.100			0.004		
ddd	0.080			0.003		
eee	0.150			0.006		
fff	0.080			0.003		
Ball Diam	0.300			0.012		
N	192			192		
MD/ME	15/15			15/15		

Figure 2-1 T31A package outline drawing

T31 Ball Assignment Ver1.4

BGA192, 10mm X 10mm X 1.22mm, 0.65pitch, top view

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	0
A		OSC_CTL	VDDIO_OSC	EXCLK_I	PWM0_SSI1_DT_PB17	SMB1_SCK_SSI1_CLK_PB26	DRV_VBUS_PWM2_SSI1_DT_PB27	SSI1_CLK_DMIC_DAT0_PB29	DDRPLL_VCCA	DDRPLL_VCCD	UART1_TXD_TCK_PB23	UART0_TXD_TDO_SLCD_RDY_PB22	UART0_RTS_I2S_DAC_BCLK_SLCD_DC_PB21	BOOT_SEL1_PC01	GMAC_TXD1_MSC1_D3_I2S_DAC_MCLK_SLCD_D7_PB14	GMAC_PHY_CLK_SLCD_D1_PB07	A
B		PLL_VDDHV	PLL_VDD	EXCLK_O	PWM1_SSI1_DR_PB18	SMB1_SDA_SSI1_CE0_PB25	PWM3_SSI1_DR_DMIC_CLK_PB28	GPIO_PB31	SSI1_CE0_DMIC_DAT1_PB30	UART1_RXD_TMS_PB24	UART0_RXD_TDI_PB19	UART0_CTS_I2S_ADC_BCLK_SLCD_CS_PB20	BOOT_SEL0_PC00	GMAC_TXEN_MSC1_CLK_I2S_ADC_MCLK_SLCD_D2_PB08	GMAC_TXD0_MSC1_D2_I2S_ADC_LRCK_SLCD_D6_PB13	GMAC_TXCLK_SLCD_D0_PB06	B
C		POR_CTL	PLL_VSS	VDDIO0					DDRPLL_VSSA					VDDIO1	GMAC_RXD1_SLCD_TE_PB16	GMAC_RXD0_I2S_DAC_LRCK_SLCD_WR_PB15	C
D		WAIT_PWM1_PA22	PPRST_		DDR_VREF	VDDMEM	VDDMEM	VDDMEM	VDDMEM	VDDMEM	VDDMEM	VDDMEM			GMAC_RXDV_MSC1_CMD_I2S_SDTI_SLCD_D3_PB09	GMAC_MDCK_MSC1_D0_I2S_SDTO_SLCD_D4_PB10	D
E		SD7_SMB0_SCK_PA13	SA2_PA18		DDRVDD	DDRVDD	DDRVDD	DDRVDD	DDRVDD	DDRVDD	DDRVDD	DDRVDD	DDR_ZQ		GMAC_MDIO_MSC1_D1_SLCD_D5_PB11	MSC0_D2_PB02	E
F		RD_DVP_VSYNC_SMB1_SCK_MSC1_CMD_PA17	SD6_SMB0_SDA_PA12		VSSIO_OSC	VSS	VSS	VSS	VSS	VSS	VSS	VSS	TRST		MSC0_D3_PB03	MSC0_CMD_SSI_SLV_CE0_PB05	F
G		SA1_DVP_MCLK_PA15	CS2_DVP_HSYNC_SMB1_SDA_MSC1_CLK_PA16		EFUSE_AVD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS		MSC0_CLK_SSI_SLV_CLK_PB04	MSC0_D0_SSI_SLV_DT_PB00	G
H		SD5_DVP_D11_UART2_RXD_MSC1_D3_PA11	SA0_DVP_PCLK_PWM0_PA14	SD4_DVP_D10_UART2_TXD_MSC1_D2_PA10	TEST_TE	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	MSC0_D1_SSI_SLV_DR_PB01	SFC_CLK_PA27	SFC_GPC_PA25	H
J		SD3_DVP_D9_UART2_RTS_MSC1_D1_PA09	SD2_DVP_D8_UART2_CTS_MSC1_D0_PA08		VDD	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD		SFC_CE1_PA26	SFC_DT_PA23	J
K		SD1_DVP_D7_UART1_RXD_PA07	SD0_DVP_D6_UART1_TXD_PA06		VDD	VDD	VDD	VSS	VSS	VSS	VSS	VSS	VDD		SFC_CE0_PA28	SFC_DR_PA24	K
L		DVP_D5_MIPI_DATAN0	DVP_D4_MIPI_DATAP0		VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VDD		CODEC_AVDD	HPOUTL	L
M		DVP_D3_MIPI_CLKN	DVP_D2_MIPI_CLKP		MIPI_AVSS	ADC_AVSS	USB_AVSS	VDD	VDD	VDD	VDD	VDD	CODEC_AVSS		MICLN	VCM	M
N		DVP_D1_MIPI_DATAN1	DVP_D0_MIPI_DATAP1	MIPI_AVD18					MSC1_CMD_SSI_SLV_CE0_PC03					VDDIO2	MICBIAS	MICLP	N
P		MIPI_AVD08	ADC_AUX0	ADC_VREF	USB0PN	USB_AVD33	USB0ID	USB_AVD08	MSC1_D0_SSI_SLV_DT_PC04	MSC1_D2_PC06	SSI0_DR_UART2_CTS_I2S_DAC_MCLK_PC11	SSI0_DT_UART2_RTS_I2S_ADC_MCLK_PC12	SSI0_GPC_UART0_TXD_SMB1_SDA_PC08	UART0_RTS_I2S_DAC_BCLK_PC16	PWM1_I2S_SDTO_PC18	PWM2_I2S_ADC_BCLK_PC19	P
R		ADC_AUX1	ADC_AUX2	ADC_AVDD	USB0PP	USB_AVD18	VBUS	MSC1_D1_SSI_SLV_DR_PC05	MSC1_CLK_SSI_SLV_CLK_PC02	MSC1_D3_PC07	SSI0_CE0_DMIC_DAT1_UART2_RXD_PC14	SSI0_CE1_UART0_RXD_SMB1_SCK_PC09	SSI0_CLK_DMIC_DAT0_UART2_TXD_PC13	PWM3_DMIC_CLK_I2S_ADC_LRCK_PC20	UART0_CTS_I2S_DAC_LRCK_PC15	PWM0_I2S_SDTI_PC17	R
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	

Figure 2-2 T31A pin to ball assignment

2.5 Pin Description

2.5.1 Static Memory/DVP/I2Cx/UARTx/PWMx/MSC1

Table 2-1 Static Memory/DVP/I2Cx/UARTx/PWMx/MSC1 Pins(13)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
SD0 DVP_D6 UART1_TXD PA06	IO I O IO	K2	2mA	SD0: Static memory data bus bit 0 DVP_D6:DVP data bit 6 UART1_TXD: UART1 data transmit PA06: GPIO group A bit 06	VDDIO0
SD1 DVP_D7 UART1_RXD PA07	IO I I IO	K1	2mA	SD1: Static memory data bus bit 1 DVP_D7:DVP data bit 7 UART1_RXD: UART 1 receive data PA07: GPIO group A bit 07	VDDIO0
SD2 DVP_D8 UART2_CTS MSC1_D0 PA08	IO I IO I IO	J2	2mA	SD2: Static memory data bus bit 2 DVP_D8:DVP data bit 8 UART2_CTS: UART2 clear-to-send handshaking MSC1_D0: MSC (MMC/SD) 1 data bit 0 PA08: GPIO group A bit 08	VDDIO0
SD3 DVP_D9 UART2_RTS MSC1_D1 PA09	IO I O IO IO	J1	2mA	SD3: Static memory data bus bit 3 DVP_D9:DVP data bit 9 UART2_RTS: UART2 request-to-send handshaking MSC1_D1: MSC (MMC/SD) 1 data bit 1 PA09: GPIO group A bit 09	VDDIO0
SD4 DVP_D10 UART2_TXD MSC1_D2 PA10	IO I O IO IO	H3	2mA	SD4: Static memory data bus bit 4 DVP_D10:DVP data bit 10 UART2_TXD: UART2 data transmit MSC1_D2: MSC (MMC/SD) 1 data bit 2 PA10: GPIO group A bit 10	VDDIO0
SD5 DVP_D11 UART2_RXD MSC1_D3 PA11	IO I I IO IO	H1	2mA PU-rst*	SD5: Static memory data bus bit 5 DVP_D11:DVP data bit 11 UART2_RXD: UART2 data receive MSC1_D3: MSC (MMC/SD) 1 data bit 3 PA11: GPIO group A bit 11	VDDIO0
SD6 SMB0_SDA PA12	IO IO IO	F2	2mA PU-rst	SD6: Static memory data bus bit 6 SMB0_SDA: I2C 0 serial data PA12: GPIO group A bit 12	VDDIO0
SD7 SMB0_SCK PA13	IO O IO	E1	2mA PU-rst	SD7: Static memory data bus bit 7 SMB0_SCK: I2C 0 serial clock PA13: GPIO group A bit 13	VDDIO0
SA0 DVP_PCLK PWM0 PA14	O I O IO	H2	2mA	SA0: Static memory address bus bit 0 DVP_PCLK: camera sensor pixel clock input PWM0: PWM channel 0 output PA14: GPIO group A bit 14	VDDIO0
SA1 DVP_MCLK PA15	O O IO	G1	2mA SR-rst*	SA1: Static memory address bus bit 1 DVP_MCLK: DVP main clock output PA15: GPIO group A bit 15	VDDIO0

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
CS2 DVP_HSYNC SMB1_SDA MSC1_CLK PA16	O I IO O IO	G2	2mA PU-rst	CS2: Static memory chip 2 select DVP_HSYNC: DVP horizontal sync SMB1_SDA: I2C 1 serial data MSC1_CLK: MSC (MMC/SD) 1 clock output PA16: GPIO group A bit 16	VDDIO0
RD DVP_VSYNC SMB1_SCK MSC1_CMD PA17	O I O IO IO	F1	2mA PU-rst	RD: Static memory read signal DVP_VSYNC: DVP vertical sync SMB1_SCK: I2C 1 serial clock MSC1_CMD: MSC (MMC/SD) 1 command PA17: GPIO group A bit 17	VDDIO0
SA02 PA18	O IO	E2	2mA	SA2: Static memory address bus bit 2 PA18: GPIO group A bit 18	VDDIO0
WAIT PWM1 PA22	I O IO	D1	2mA PU-rst SR-rst	WAIT: Slow static memory/device wait signal PWM1: PWM channel 1 output signal PA22: GPIO group A bit 22	VDDIO0

2.5.2 SFC

Table 2-2 SFC Pins(6)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
SFC_DT PA23	IO IO	J15	8mA PU-rst SMT-rst	SFC_DT: high speed ssi transmit data PA23: GPIO group A bit 23	VDDIO1
SFC_DR PA24	IO IO	K15	8mA PU-rst	SFC_DR: high speed ssi receive data PA24: GPIO group A bit 24	VDDIO1
SFC_GPC PA25	IO IO	H15	8mA PU-rst	SFC_GPC: high speed ssi general-purpose control PA25: GPIO group A bit 25	VDDIO1
SFC_CE1 PA26	IO IO	J14	8mA PU-rst	SFC_CE1: high speed ssi chip 1 select PA26: GPIO group A bit 26	VDDIO1
SFC_CLK PA27	O IO	H14	8mA PU-rst	SFC_CLK: high speed ssi clock PA27: GPIO group A bit 27	VDDIO1
SFC_CE0 PA28	O IO	K14	8mA PU-rst	SFC_CE0: high speed ssi chip 0 select PA28: GPIO group A bit 28	VDDIO1

2.5.3 MSC0/GMAC/PWMx/UARTx/I2C1/SSI1/SSI_SLV/JTAG/SLCD/DMIC/I2S

Table 2-3 MSC0/GMAC/PWMx/UARTx/I2C1/SSI1/SSI_SLV//JTAG/SLCD/DMIC/I2S Pins (30)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
MSC0_D0 SSI_SLV_DT PB00	IO O IO	G15	2mA	MSC0_D0: MSC (MMC/SD) 0 data bit 0 SSI_SLV_DT: ssi slave transmit data PB00: GPIO group B bit 00	VDDIO1
MSC0_D1 SSI_SLV_DR PB01	IO I IO	H13	2mA	MSC0_D1: MSC (MMC/SD) 0 data bit 1 SSI_SLV_DR: ssi slave receive data PB01: GPIO group B bit 01	VDDIO1

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
MSC0_D2 PB02	IO IO	E15	2mA	MSC0_D2: MSC (MMC/SD) 0 data bit 2 PB02: GPIO group B bit 02	VDDIO1
MSC0_D3 PB03	IO IO	F14	2mA	MSC0_D3: MSC (MMC/SD) 0 data bit 3 PB03: GPIO group B bit 03	VDDIO1
MSC0_CLK SSI_SLV_CLK PB04	O I IO	G14	2mA	MSC0_CLK: MSC (MMC/SD) 0 clock output SSI_SLV_CLK: ssi slave clock PB04: GPIO group B bit 04	VDDIO1
MSC0_CMD SSI_SLV_CE0 PB05	IO I IO	F15	2mA PU-rst	MSC0_CMD: MSC (MMC/SD) 0 command SSI_SLV_CE0: ssi slave chip 0 select PB05: GPIO group B bit 05	VDDIO1
GMAC_TXCLK SLCD_D0 PB06	I O IO	B15	2mA	GMAC_TXCLK: gmac transmitting clock SLCD_D0: smart lcd data output bit 0 PB06: GPIO group B bit 06	VDDIO1
GMAC_PHY_CLK SLCD_D1 PB07	O O IO	A15	2mA	GMAC_PHY_CLK: gmac phy clock SLCD_D1: smart lcd data output bit 1 PB07: GPIO group B bit 07	VDDIO1
GMAC_TXEN MSC1_CLK I2S_ADC_MCLK SLCD_D2 PB08	O O O O IO	B13	2mA	GMAC_TXEN: gmac transmitting enable MSC1_CLK: MSC (MMC/SD) 1 clock output I2S_ADC_MCLK: I2S system clock SLCD_D2: smart lcd data output bit 2 PB08: GPIO group B bit 08	VDDIO1
GMAC_RXDV MSC1_CMD I2S_SDTI SLCD_D3 PB09	I IO I O IO	D14	2mA	GMAC_RXDV: gmac receive data valid MSC1_CMD: MSC (MMC/SD) 1 command I2S_SDTI:I2S serial data input signal SLCD_D3: smart lcd data output bit 3 PB09: GPIO group B bit 09.	VDDIO1
GMAC_MDCK I2S_SDTO SLCD_D4 MSC1_D0 PB10	O IO O IO IO	D15	2mA PD-rst	GMAC_MDCK: gmac manage data clock I2S_SDTO: I2S serial data output signal SLCD_D4: smart lcd data output bit 4 MSC1_D0: MSC (MMC/SD) 1 data bit 0 PB10: GPIO group B bit 10.	VDDIO1
GMAC_MDIO MSC1_D1 SLCD_D5 PB11	IO IO O IO	E14	2mA PU-rst	GMAC_MDIO: gmac MDIO which is clocked by MDC MSC1_D1: MSC (MMC/SD) 1 data bit 1 SLCD_D5: smart lcd data output bit 5 PB11: GPIO group B bit 11.	VDDIO1
GMAC_TXD0 MSC1_D2 I2S_ADC_LRCK SLCD_D6 PB13	O IO O O IO	B14	2mA	GMAC_TXD0: gmac transmit data bit 0 MSC1_D2: MSC (MMC/SD) 1 data bit 2 I2S_ADC_LRCK: I2S ADC left/right clock SLCD_D6: smart lcd data output bit 6 PB13: GPIO group B bit 13.	VDDIO1
GMAC_TXD1 MSC1_D3 I2S_DAC_MCLK SLCD_D7 PB14	O IO O O IO	A14	2mA PU-rst	GMAC_TXD1: gmac transmit data bit 1 MSC1_D3: MSC (MMC/SD) 1 data bit 3 I2S_DAC_MCLK: I2S system clock SLCD_D7: smart lcd data output bit 7 PB14: GPIO group B bit 14.	VDDIO1
GMAC_RXD0 I2S_DAC_LRCK SLCD_WR PB15	I O O IO	C15	2mA	GMAC_RXD0: gmac receive data bit 0 I2S_DAC_LRCK: I2S DAC left/right clock SLCD_WR: smart lcd write data control PB15: GPIO group B bit 15.	VDDIO1

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
GMAC_RXD1 SLCD_TE PB16	I O IO	C14	2mA PU-rst	GMAC_RXD1: gmac receive data bit 1 SLCD_TE: smart lcd crack control PB16: GPIO group B bit 16.	VDDIO1
PWM0 SSI1_DT PB17	O O IO	A4	2mA PD-rst	PWM0: PWM channel 0 output SSI1_DT: normal speed ssi 1 transmit data PB17: GPIO group B bit 17.	VDDIO1
PWM1 SSI1_DR PB18	O I IO	B4	mA PD-rst	PWM1: PWM channel 1 output SSI1_DR: normal speed ssi 1 receive data PB18: GPIO group B bit 18.	VDDIO1
UART0_RXD TDI PB19	I I IO	B10	2mA PU-rst	UART0_RXD: UART 0 data receive TDI: JTAG data input PB19: GPIO group B bit 19	VDDIO1
UART0_CTS I2S_ADC_BCLK SLCD_CS PB20	I IO O IO	B11	2mA	UART0_CTS: UART 0 clear-to-send handshaking I2S_ADC_BCLK: I2S ADC bit clock SLCD_CS: smart lcd chip select PB20: GPIO group B bit 20	VDDIO1
UART0_RTS I2S_DAC_BCLK SLCD_DC PB21	O IO O IO	A12	2mA	UART0_RTS: UART 0 request-to-send handshaking I2S_DAC_BCLK: I2S DAC bit clock SLCD_DC: smart lcd cmd/data identify PB21: GPIO group B bit 21	VDDIO1
UART0_TXD TDO SLCD_RDY PB22	O O O IO	A11	2mA	UART0_TXD: UART 0 data transmit TDO: JTAG data output SLCD_RDY: smart lcd work status PB22: GPIO group B bit 22	VDDIO1
UART1_TXD TCK PB23	O I IO	A10	2mA	UART1_TXD: UART 1 transmit data TCK: JTAG clock input PB23: GPIO group B bit 23	VDDIO1
UART1_RXD TMS PB24	I I IO	B9	2mA PU-rst	UART1_RXD: UART 1 receive data TMS: JTAG mode select PB24: GPIO group B bit 24	VDDIO1
SMB1_SDA SSI1_CE0 PB25	IO O IO	B5	2mA PU-rst	SMB1_SDA: I2C 1 serial data SSI1_CE0: normal speed ssi 1 chip 0 select PB25: GPIO group B bit 25	VDDIO1
SMB1_SCK SSI1_CLK PB26	O O IO	A5	2mA PU-rst	SMB1_SCK: I2C 1 serial clock SSI1_CLK: normal speed ssi 1 clock PB26: GPIO group B bit 26	VDDIO1
DRV_VBUS PWM2 SSI1_DT PB27	O O O IO	A6	2mA PD-rst	DRV_VBUS:USB-5V control signal PWM2: PWM channel 2 output SSI1_DT: normal speed ssi 1 transmit data PB27: GPIO group B bit 27	VDDIO1
PWM3 SSI1_DR DMIC_CLK PB28	O I O IO	B6	2mA PD-rst	PWM3: PWM channel 3 output SSI1_DR: normal speed ssi 1 data receive DMIC_CLK: digital microphone clock output PB28: GPIO group B bit 28	VDDIO1
SSI1_CLK DMIC_DAT0 PB29	O I IO	A7	2mA PU-rst	SSI1_CLK: normal speed ssi 1 clock DMIC_DAT0: digital microphone data bit 0 PB29: GPIO group B bit 29	VDDIO1
SSI1_CE0	O	B8	2mA	SSI1_CE0: normal speed ssi 1 chip 0 select	VDDIO1

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
DMIC_DAT1 PB30	I IO		PU-rst	DMIC_DAT1: digital microphone data bit 1 PB30: GPIO group B bit 30	

2.5.4 MSC1/SSI1/SSI_SLV/I2S/DMIC/UARTx/PWMx

Table 2-4 MSC1/SSI1/SSI_SLV/I2S/DMIC/UARTx/PWMx Pins (18)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
MSC1_CLK SSI_SLV_CLK PC02	O I IO	R8	2mA	MSC1_CLK: MSC (MMC/SD) 1 clock output SSI_SLV_CLK: ssi slave clock PC02: GPIO group C bit 02	VDDIO2
MSC1_CMD SSI_SLV_CE0 PC03	IO I IO	N8	2mA PU-rst	MSC1_CMD: MSC (MMC/SD) 1 command SSI_SLV_CE0: ssi slave chip 0 select PC03: GPIO group C bit 03	VDDIO2
MSC1_D0 SSI_SLV_DT PC04	IO O IO	P8	2mA	MSC1_D0: MSC (MMC/SD) 1 data bit 0 SSI_SLV_DT: ssi slave transmit data PC04: GPIO group C bit 04	VDDIO2
MSC1_D1 SSI_SLV_DR PC05	IO I IO	R7	2mA	MSC1_D1: MSC (MMC/SD) 1 data bit 1 SSI_SLV_DR: ssi slave receive data PC05: GPIO group C bit 05	VDDIO2
MSC1_D2 PC06	IO IO	P9	2mA	MSC1_D2: MSC (MMC/SD) 1 data bit 2 PC06: GPIO group C bit 06	VDDIO2
MSC1_D3 PC07	IO IO	R9	2mA	MSC1_D3: MSC (MMC/SD) 1 data bit 3 PC07: GPIO group C bit 07	VDDIO2
SSI0_GPC UART0_TXD SMB1_SDA PC08	O O IO IO	P12	2mA PU-rst	SSI0_GPC: normal speed ssi 0 general-purpose control UART0_TXD: UART 0 data transmit SMB1_SDA: I2C 1 serial data PC08: GPIO group C bit 08	VDDIO2
SSI0_CE1 UART0_RXD SMB1_SCK PC09	O I O IO	R11	2mA PU-rst	SSI0_CE1:normal speed ssi 0 chip 1 select UART0_RXD: UART 1 receive data SMB1_SCK: I2C 1 serial clock PC09: GPIO group C bit 09	VDDIO2
SSI0_DR UART2_CTS I2S_DAC_MCLK PC11	I I O IO	P10	2mA	SSI0_DR: normal speed ssi 0 receive data UART2_CTS: UART 2 clear-to-send handshaking I2S_DAC_MCLK: I2S DAC system clock PC11: GPIO group C bit 11	VDDIO2
SSI0_DT UART2_RTS I2S_ADC_MCLK PC12	O O O IO	P11	2mA	SSI0_DT: normal speed ssi 0 transmit data UART2_RTS: UART 2 request-to-send handshaking I2S_ADC_MCLK: I2S ADC system clock PC12: GPIO group C bit 12	VDDIO2
SSI0_CLK DMIC_DAT0 UART2_TXD PC13	O I O IO	R12	2mA	SSI0_CLK: normal speed ssi 0 clock DMIC_DAT0: digital microphone data bit 0 UART2_TXD: UART 2 transmit data PC13: GPIO group C bit 13	VDDIO2
SSI0_CE0	O	R10	2mA	SSI0_CE0: normal speed ssi 0 chip 0 select	VDDIO2

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
DMIC_DAT1 UART2_RXD PC14	I I IO		PU-rst	DMIC_DAT1: digital microphone data bit 1 UART2_RXD: UART 2 receive data PC14: GPIO group C bit 14	
UART0_CTS I2S_DAC_LRCK PC15	I IO IO	R14	2mA	UART0_CTS: UART 0 Clear-to-Send handshaking signal I2S_DAC_LRCK: I2S DAC left/right clock PC15: GPIO group C bit 15	VDDIO2
UART0_RTS I2S_DAC_BCLK PC16	O IO IO	P13	2mA	UART0_RTS: UART 0 Request-to-Send handshaking signal I2S_DAC_BCLK: I2S DAC bit clock PC16: GPIO group C bit 16	VDDIO2
PWM0 I2S_SDTI PC17	O I IO	R15	2mA SMT-rst PD-rst	PWM0: PWM channel 0 output I2S_SDTI: I2S serial data input signal PC17: GPIO group C bit 17	VDDIO2
PWM1 I2S_SDTO PC18	O O IO	P14	2mA SMT-rst PD-rst	PWM1: PWM channel 1 output I2S_SDTO: I2S serial data output signal PC18: GPIO group C bit 18	VDDIO2
PWM2 I2S_ADC_BCLK PC19	O IO IO	P15	2mA SMT-rst	PWM2: PWM channel 2 output I2S_ADC_BCLK: I2S ADC bit clock PC19: GPIO group C bit 19	VDDIO2
PWM3 DMIC_CLK I2S_ADC_LRCK PC20	O O IO IO	R13	2mA SMT-rst	PWM3: PWM channel 3 output DMIC_CLK: digital microphone clock output I2S_ADC_LRCK: I2S ADC left/right clock PC20: GPIO group C bit 20	VDDIO2

2.5.5 GPIO

Table 2-5 GPIO Pins (1)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
PB31	IO	B7	2mA PD-rst	PB31: GPIO group B bit 31	VDDIO1

2.5.6 System Control

Table 2-6 System Control Pins(4)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
TRST	I	F12	2mA SMT PD	TRST: JTAG reset	VDDIO0
PPRST_	I	D2	2mA SMT	PPRST_: RTC power on reset and RESET-KEY reset input	VDDIO0
TEST_TE	I	H4	2mA SMT PD	TEST_TE: Manufacture test enable, program readable	VDDIO0

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
OSC_CTL	I	A1	2mA SMT PD	OSC_CTL: Oscillator bypass control	VDDIO0
POR_CTL	I	C1	2mA PU	POR_CTL: Power-on-Reset model bypass control	VDDIO0

Table 2-7 Boot Select Pins(2)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
(BOOT_SEL0) PC00	I IO	B12	2mA PU-rst	It is taken as BOOT select bit 0 by Boot ROM code PC00: GPIO group C bit 00	VDDIO1
(BOOT_SEL1) PC01	I IO	A13	2mA PD-rst	It is taken as BOOT select bit 1 by Boot ROM code PC01: GPIO group C bit 01	VDDIO1

2.5.7 Digital IO/core power/ground

Table 2-8 IO/Core power supplies Pins (59)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
VDDIO0	P	C3	-	VDDIO0: IO digital power for DVP power domain, 1.8V	-
VDDIO1	P	C13	-	VDDIO1: IO digital power for normal function Pad power domain, 1.8V/3.3V	-
VDDIO2	P	N13	-	VDDIO2: IO digital power for normal function Pad power domain, 1.8V/3.3V	-
VDD	P	J4,J12,K4,K5,K6,K12,L4,L5,L6,L7,L8,L9,L10,L11,L12,M7,M8,M9,M10,M11	-	VDD: CORE digital power, 0.8V	-
VSS	P	F5,F6,F7,F8,F9,F10,F11,G5,G6,G7,G8,G9,G10,G11,G12,H5,H6,H7,H8,H9,H10,H11,H12,J5,J6,J7,J8,J9,J10,J11,K7,K8,K9,K10,K11	-	VSS: IO digital ground for none DRAM and CORE digital ground, 0V	-

2.5.8 DDR power/ground

Table 2-9 DDR power/ground supplies Pins (20)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
DDR_VREF	P	D4	-	DDR_VREF: DDR reference voltage, (VREF = VDDMEM/2)	-
DDR_ZQ	AIO	E12	-	DDR_ZQ: DDR3 External reference which is connected to a 240Ω resister to VSS.	-
VDDMEM	P	D5,D6,D7,D8, D9,D10,D11	-	VDDMEM: DDR PHY supply(1.35V for DDR3L)	-
DDRVDD	P	E4,D5,D6,D7, D8,D9,D10,D11	-	DDRVDD: DDR3L KGD 1.35V supply	-
DDR_PLLVCCD	P	A9	-	DDR_PLLVCCD: DDR PLL power supply for digital	-
DDR_PLLVCCA	P	A8	-	DDR_PLLVCCA: DDR PLL power supply for analog	-
DDRPLL_VSSA	P	C8	-	DDRPLL_VSSA: DDR PLL analog ground	-

2.5.9 Analog - USB 2.0 OTG

Table 2-10 USB 2.0 OTG (8)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
USB0PP	AIO	R4	-	USB0PP: USB2.0 positive data line	USB_AVD33
USB0PN	AIO	P4	-	USB0PN: USB2.0 negative data line	USB_AVD33
USB0ID	AI	P6	-	USB0ID: Used to identify the device attached to the PHY. The state of the pin is one if: high impedance(>1MΩ) or low impedance(<10Ω to ground).	USB_AVD18
VBUS	AIO	R6	-	VBUS: The VBUS power supply can be used for a combination of functions. In the case of powered devices, it is used for signaling to detect which device is connected. No charge pumps inside PHY, so no supplying capability by default. The PHY supports the VBUS divided to 3/5(default) off chip or not	USB_AVD18
USB_AVD33	P	P5	-	USB_VCC33: This is the analog supply that is used to support 3.3V signaling. This supply has both integrated IO pads and associated ESD. The expectation is that this supply is unique to the USB PHY. The PHY provides two pins for this power supply, but they can often be bonded out to a single package pin if the parasitic are low enough to support the current draw.	-
USB_AVD18	P	R5	-	USB_VCC18: This is the analog supply that is used to support 1.8V signaling. This supply has both integrated IO pads.	-
USB_AVD08	P	P7	-	USB_AVD08: This is the analog supply that is used to support 0.8V circuits within the PHY. This supply has both integrated IO pads and	-

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
				associated ESD. As this includes power supplied to the PLL and HS driver, the supply needs to be fairly quiet. The PHY provides two pins for this power supply, but they can often be bonded out to a single pin if the parasitic are low enough to support the current draw.	
USB_AVSS	P	M6	-	USB_AVS: This is the analog ground. This ground has both integrated IO pads and associated ESD. It is potentially sinking all the current accumulated for the PHY. The PHY provides two pins for this ground, but they can often be bonded out to a single pin if the ground lift can be kept less than 10mV	-

2.5.10 Analog - MIPI and DVP

Table 2-11 MIPI CSI and DVP(9)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
DVP_D5 MIPI_DATAN0	AIO	L1	-	DVP_D5: In TTL model is DVP input data bit 5 MIPI_DATAN0: In MIPI model is data lane 0 serial signal	MIPI_AVD_18
DVP_D4 MIPI_DATAP0	AIO	L2	-	DVP_D4: In TTL model is DVP input data bit 4 MIPI_DATAP0: In MIPI model is data lane 0 serial signal	MIPI_AVD18
DVP_D3 MIPI_CLKN	AIO	M1	-	DVP_D3: In TTL model is DVP input data bit 3 MIPI_CLKN: In MIPI model is clock lane serial signal	MIPI_AVD18
DVP_D2 MIPI_CLKP	AIO	M2	-	DVP_D2: In TTL model is DVP input data bit 2 MIPI_CLKP: In MIPI model is clock lane serial signal	MIPI_AVD18
DVP_D1 MIPI_DATAN1	AIO	N1	-	DVP_D1:In TTL model is DVP input data bit 1 MIPI_DATAN1: In MIPI model is data lane 1 serial signal	MIPI_AVD18
DVP_D0 MIPI_DATAP1	AIO	N2	-	DVP_D0：In TTL model is DVP input data bit 0 MIPI_DATAP1: In MIPI model is data lane 1 serial signal	MIPI_AVD18
MIPI_AVD08	P	P1	-	MIPI_AVD08: PHY analog power, 0.8V	-
MIPI_AVD18	P	N3	-	MIPI_AVD18: PHY analog power, 1.8V	-
MIPI_AVSS	P	M4	-	MIPI_AVSS: PHY analog ground	-

NOTES:

1. DVP_Dx signals can input form this Pad when configure the MIPI PHY to TTL model

2.5.11 Analog - SARADC

Table 2-12 SARADC Pins (6)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
ADC_AUX0	AI	P2	-	AUX0: SARADC channel 0 input	ADC_AVDD
ADC_AUX1	AI	R1	-	AUX1: SARADC channel 1 input	ADC_AVDD
ADC_AUX2	AI	R2	-	AUX2: SARADC channel 2 input	ADC_AVDD
ADC_VREF	P	P3	-	ADC_VREF: Voltage reference input, 0.5* ADC_AVDD~0.99* ADC_AVDD	-
ADC_AVDD	P	R3	-	ADC_AVDD: SARADC analog power, 1.8 V	-
ADC_AVSS	P	M5	-	ADC_AVSS: analog ground	-

2.5.12 Analog - CODEC

Table 2-13 CODEC Pins (7)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
MICP	AI	N15	-	MICP: differential microphone input	CODEC_AVDD
MICN	AI	M14	-	MICN: differential microphone input	CODEC_AVDD
MICBIAS	AO	N14	-	MICBIAS: Microphone bias output	CODEC_AVDD
VCM	AO	M15	-	VCM: Reference voltage output	CODEC_AVDD
HPOUT	AO	L15	-	HPOUT: headphone output	CODEC_AVDD
CODEC_AVDD	P	L14	-	CODEC_AVDD:1.8V analog supply	-
CODEC_AVSS	P	M12	-	CODEC_AVSS: analog ground	-

2.5.13 Analog - EFUSE

Table 2-14 EFUSE Pins (1)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
EFUSE_AVD	P	G4	-	EFUSE: EFUSE programming power, 0V/1.8V	-

2.5.14 Analog - CLOCK/PLL

Table 2-15 CLOCK/PLL Pins (5)

Pin Names	IO	Loc	IO Cell Char.	Pin Description	Power
EXCLK_XI	AI	A3	2~30 MHz Oscillator, OSC on/off	EXCLK_XI: external oscillator clock input or external 24MHz clock input	VDDIO_OSC
EXCLK_XO	AO	B3		EXCLK_XO: external oscillator clock output	VDDIO_OSC
VDDIO_OSC	P	A2	-	VDDIO_OSC: Oscillator power supply, 1.8V	-
VSSIO_OSC	P	F4	-	VSSIO_OSC: Oscillator ground	-
PLL_VDDHV	P	B1	-	PLL_VDDHV:PLL analog supply power 1.8V	-
PLL_VDD	P	B2	-	PLL_VDD: PLL digital supply power 0.8V	-
PLL_VSS	P	C2	-	PLL_VSS: PLL 0V supply and substrate connection	-

NOTES:

1 All GPIO are programmable with multi-voltage (1.8V, 3.3V) general purpose, bi-directional I/O buffer with a selectable LVCMOS input or LVCMOS Schmitt trigger input and programmable pull-up / pull-down. In the full-drive mode, this buffer can operate in excess of 100MHz frequency with 15pF external load and 125 MHz with 10pF load, but actual frequency is load and system dependent. A maximum of 200 MHz can be achieved under small capacitive loads.

2 The meaning of phases in IO cell characteristics are:

- 2/8mA out: The IO cell's output driving strength is about 2/8mA.
- PU: The IO cell contains a pull-up resistor and fixed pull up.
- PD: The IO cell contains a pull-down resistor and fixed pull down.
- PU-rst: The IO cell during reset and after the pull up function is enabled.
- PD-rst: The IO cell during reset and after the pull down function is enabled.
- SMT: The IO cell is Schmitt trigger input and fixed.
- SMT-rst: The IO cell during reset and after the Schmitt trigger input function is enabled.
- SR-rst: The IO cell during reset and after the slew-rate function select fast mode.

3 Electrical Specifications

3.1 Absolute Maximum Ratings

The absolute maximum ratings for the processors are listed in Table 3-1. Do not exceed these parameters or the part may be damaged permanently. Operation at absolute maximum ratings is not guaranteed.

Table 3-1 Absolute Maximum Ratings

Parameter	Min	Max	Unit
Storage Temperature	-65	150	°C
Operation Temperature	-40	125	°C
VDDMEM power supplies voltage	-0.1	1.98	V
DDRVDD power supplies voltage	-0.1	1.98	V
DDR_PLLVCCA power supplies voltage	-0.1	1.98	V
DDR_PLLVCCD power supplies voltage	-0.1	0.88	V
VDDIO0 power supplies voltage	-0.5	1.98	V
VDDIO1 power supplies voltage	-0.5	3.63	V
VDDIO2 power supplies voltage	-0.5	3.63	V
VDD power supplies voltage	-0.2	0.96	V
PLL_VDDHV power supplies voltage	-0.1	1.98	V
EFUSE_AVD power supplies voltage	-0.1	1.98	V
USB_AVD33 power supplies voltage	-0.1	3.63	V
USB_AVD18 power supplies voltage	-0.1	1.98	V
USB_AVD08 power supplies voltage	-0.1	0.88	V
ADC_AVDD power supplies voltage	-0.1	1.98	V
CODEC_AVDD power supplies voltage	-0.1	1.98	V
Maximum ESD stress voltage, Human Body Model; Any pin to any supply pin, either polarity, or Any pin to all non-supply pins together, either polarity. Three stresses maximum.	-	2000	V

3.2 Recommended operating conditions

Table 3-2 Recommended operating conditions for power supplies

Symbol	Description	Min	Typical	Max	Unit
VDDMEM	VDD PHY voltage for SSTL18 (DDR2)	1.35	1.35	1.98	V
DDRVDD	DDR KGD power supplies voltage	1.35	1.35	1.98	V
DDRPLL_VCCA	DDR PLL analog supplies voltage	1.62	1.8	1.98	V
DDRPLL_VCCD	DDR PLL digital supplies voltage	0.72	0.8	0.88	V

VDDIO0	GPIO power domain 0 supplies voltage	1.62	1.8	1.98	V
VDDIO1	GPIO power domain 1 supplies voltage	1.5	3.3	3.63	V
VDDIO2	GPIO power domain 2 supplies voltage	1.5	3.3	3.63	V
VDD	VDD core supplies voltage	0.72	0.8	0.88	V
PLL_VDDHV	APLL, MPLL and VPLL analog voltage	1.62	1.8	1.98	V
PLL_VDD	APLL, MPLL and VPLL digital voltage	0.72	0.8	0.88	V
VDDIO_OSC	Oscillator supplies voltage	1.62	1.8	1.98	V
EFUSE_AVD	EFUSE program supplies voltage	1.62	1.8	1.98	V
USB_AVD33	USB PHY VCCA3P3 analog voltage	3.0	3.3	3.6	V
USB_AVD18	USB PHY VCC18 analog voltage	1.62	1.8	1.98	V
USB_AVD08	USB PHY core analog voltage	0.72	0.8	0.88	V
ADC_AVDD	SARADC analog voltage	1.62	1.8	1.98	V
CODEC_AVDD	CODEC analog voltage	1.62	1.8	1.98	V
MIPI_AVD08	MIPI analog voltage	0.72	0.8	0.88	V
MIPI_AVD18	MIPI analog voltage	1.62	1.8	1.98	V

Table 3-3 Recommended operating conditions for VDDIO0/VDDIO1/VDDIO2 supplied pins

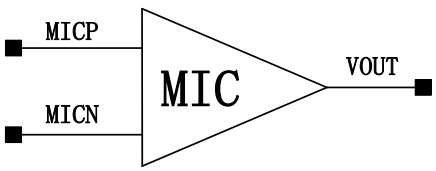
Symbol	Parameter	Min	Typical	Max	Unit
V_{IH18}	Input high voltage for 1.8V I/O application	*0.65	-	+0.3	V
V_{IL18}	Input low voltage for 1.8V I/O application	-0.3	-	*0.35	V
V_{IH25}	Input high voltage for 2.5V I/O application	1.7	-	+0.3	V
V_{IL25}	Input low voltage for 2.5V I/O application	-0.3	-	0.7	V
V_{IH33}	Input high voltage for 3.3V I/O application	2	-	+0.3	V
V_{IL33}	Input low voltage for 3.3V I/O application	-0.3	-	0.8	V

Table 3-4 Recommended operating conditions for others

Symbol	Description	Min	Typical	Max	Unit
T_A	Ambient temperature	-20	25	+85	°C
TJ	Junction temperature	-40	25	+125	°C

3.3 Audio codec

3.3.1 Microphone input



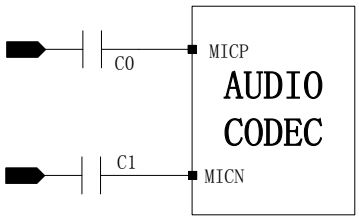
There are two inputs channels named left ADC channel and right ADC channel. In the each channel,

there are one inputs which are configured as differential input by the microphone PGA(MICL).

The signal of microphone output should be input to AUDIO CODEC through DC-blocking capacitor, as shown in following figure. The capacitance and input resistance form a high pass filter. For example, when the gain of the MIC module is 20dB, the input resistance is 45KΩ and 0.1uF DC-blocking capacitor is used, the lower cut-off frequency is:

$$f = \frac{1}{2\pi RC} = \frac{1}{2\pi \times 45 \times 10^{3} \times 0.1 \times 10^{-6}} = 35.4Hz$$

The capacitance of the DC-blocking capacitor should be determined by the minimum input impedance and application requirements.



If the output of microphone is single-ended, the AUDIO ADC input should be connected as following figure.

Microphone PGA has four gains to amplify the input signal, that is, 0dB, 20dB, 30dB and 40dB.

3.3.2 ALC

Automatic Level Control (ALC) function is included to adjust the signal level, which is input into ADC. ALC will measure the signal magnitude and compare it to defined threshold. Then it will adjust the ALC controlled PAG (ALC_L and ALC_R) gain according to the comparison result.

The programmable gain range of ALC controlled PAG is from -18dB to +28.5dB. The tuning step is 1.5dB.

3.3.3 Headphone output

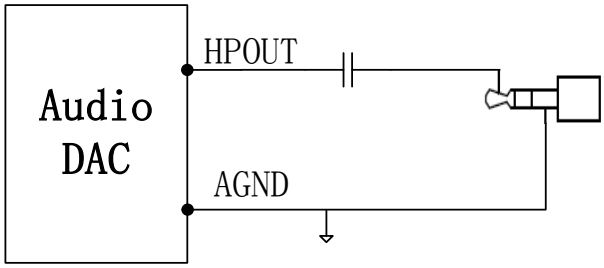
Audio codec DAC output can drive 16Ω or 32Ω headphone load through DC-blocking capacitor.

In the configuration using DC-blocking capacitor, shown in following figure, the headphone ground is connected to the real ground. The capacitance and the load resistance determine the lower cut-off frequency. For instance, if 16Ω headphone and 100uF DC-blocking capacitor are used, the lower

cut-off frequency is

$$f = \frac{1}{2\pi RC} = \frac{1}{2\pi \times 16 \times 100 \times 10^{-6}} = 99.5Hz$$

The DC-blocking capacitor can be increased to lower the cut-off frequency for better bass response.



The headphone driver chooses DAC output as input. It has a gain rang from -39dB to +6dB with a tuning step of 1.5dB.

3.3.4 Microphone bias

Microphone bias output is used to bias external microphones. The bias voltage can varies from 0.8*CODEC_AVDD to 0.975* CODEC_AVDD with a step of 0.025* CODEC_AVDD.

3.4 Power On, Reset and BOOT

3.4.1 Power-On Timing

The external voltage regulator and other power-on devices must provide the T31A processor with a specific sequence of power and resets to ensure proper operation. Figure 3-2 shows this sequence and Table 3-5 gives the timing parameters. Following are the name of the power.

- AVDAUD: PLL_VDDHV, VDDIO_OSC
- VDD08: all 0.8V power supplies, include VDD
- VDD: all other digital IO, include DDR power supplies: VDDMEM, DDRVDD,VDDIO0, VDDIO1,VDDIO2
- AVD: all other analog power supplies: ADC_AVDD, USB_AVD33, USB_AVD18, CODEC_AVDD, MIPI_AVD08, MIPI_AVD18

Table 3-5 Power-On Timing Parameters

Symbol	Parameter	Min	Max	Unit
t_{R_VDD}	VDD rise time[1]	0	5	ms
t_{R_VDD08}	VDD08 rise time[1]	0	5	ms
t_{D_VDD08}	Delay between VDD arriving 50% (or 90%) to VDD08 arriving 50% (or 90%)	–1	1	ms
t_{R_AVDAUD}	AVDAUD rise time[1]	0	5	ms

t_{D_AVDAUD}	Delay between VDD10 arriving 50% (or 90%) to AVDAUD arriving 50% (or 90%)	0.01	1	ms
t_{R_AVD}	AVD rise time[1]	0	5	ms
t_{D_AVDA}	Delay between VDD arriving 50% to AVD arriving 50%	-1	1	ms
$t_{D\_PPRST\_}$	Delay between VDDAUD stable and PPRST_ deasserted	TBD[3]	–	ms[2]

NOTES:

- The power rise time is defined as 10% to 90%.
- The PPRST_ must be kept at least 100us. After PPRST_ is deasserted, the corresponding chip reset will be extended at least 40ms.

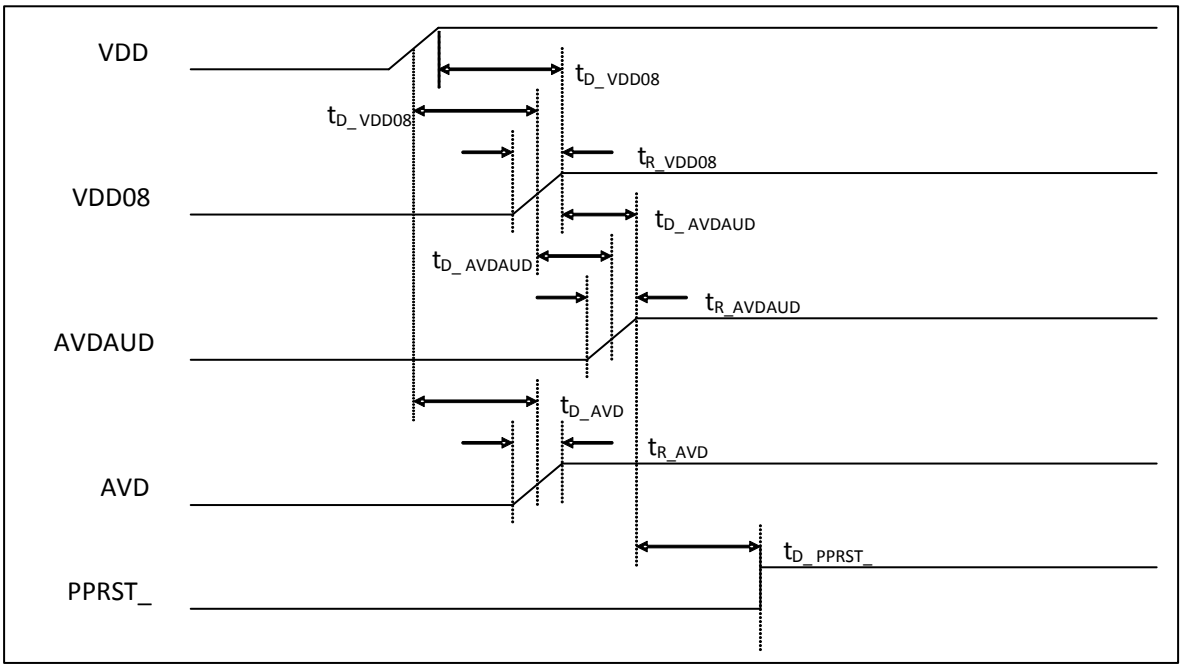


Figure 3-1 Power-On Timing Diagram

3.4.2 Reset procedure

There are 3 reset sources: 1. PPRST_ pin reset; 2. WDT timeout reset; and 3. hibernating reset when exiting hibernating mode. After reset, program start from boot.

- PPRST_ pin reset.
  This reset is trigged when PPRST_ pin is put to logic 0. It happens in power on RTC power and RESET-KEY pressed to reset the chip from unknown dead state. The reset end time is about 1M EXCLK cycles after rising edge of PPRST_.
- WDT reset.
  This reset happens in case of WDT timeout. The reset keeps for about a few RTCLK cycles.
- Hibernating reset.
  This reset happens in case of wakeup the main power from power down. The reset keeps for

about 1ms ~ 125ms programable, plus 1M EXCLK cycles, start after WKUP_ signal is recognized.

After reset, all GPIO shared pins are put to GPIO input function and most of their internal pull-up/down resistor are set to on, see “2.5Pin Description” for details. The oscillators are on. The USB 2.0 OTG PHY, the audio CODEC DAC/ADC, the SAR-ADCs is put in suspend mode.

3.4.3 BOOT

The boot sequence of the T31A is controlled by boot_sel[1:0]. The configuration is shown as follow:

Table 3-6 Boot Configuration of T31A

boot_sel[1:0]	Boot method
00	MMC/SD boot @ MSC0 (MMC/SD use GPIO Port B. MSC1 use GPIO Port C)
01	SFC boot @ CS4 (SPI boot)
10	NOR boot @ CS2 (just for FPGA testing)
11	USB boot @ USB 2.0 device, EXTCLK=24MHz

Note:

1. When SFC boot start failure, the program in bootrom will go into MSC0 boot, If it is boot from MMC/SD card at MSC0, its function pins MSC0_D0, MSC0_CLK, MSC0_CMD are initialized, the boot program loads the maximum 100KB code from MMC/SD card to cache and jump to it. Only one data bus which is MSC1_D0 is used.
2. When MSC0 boot start failure, the program in bootrom will go into MSC1 boot，If it is boot from MMC/SD card at MSC1, its function pins MSC1_D0, MSC1_CLK, MSC1_CMD are initialized, the boot program loads the maximum 100KB code from MMC/SD card to cache and jump to it. Only one data bus which is MSC1_D0 is used.If MSC1 boot start failure, jump to USB boot.

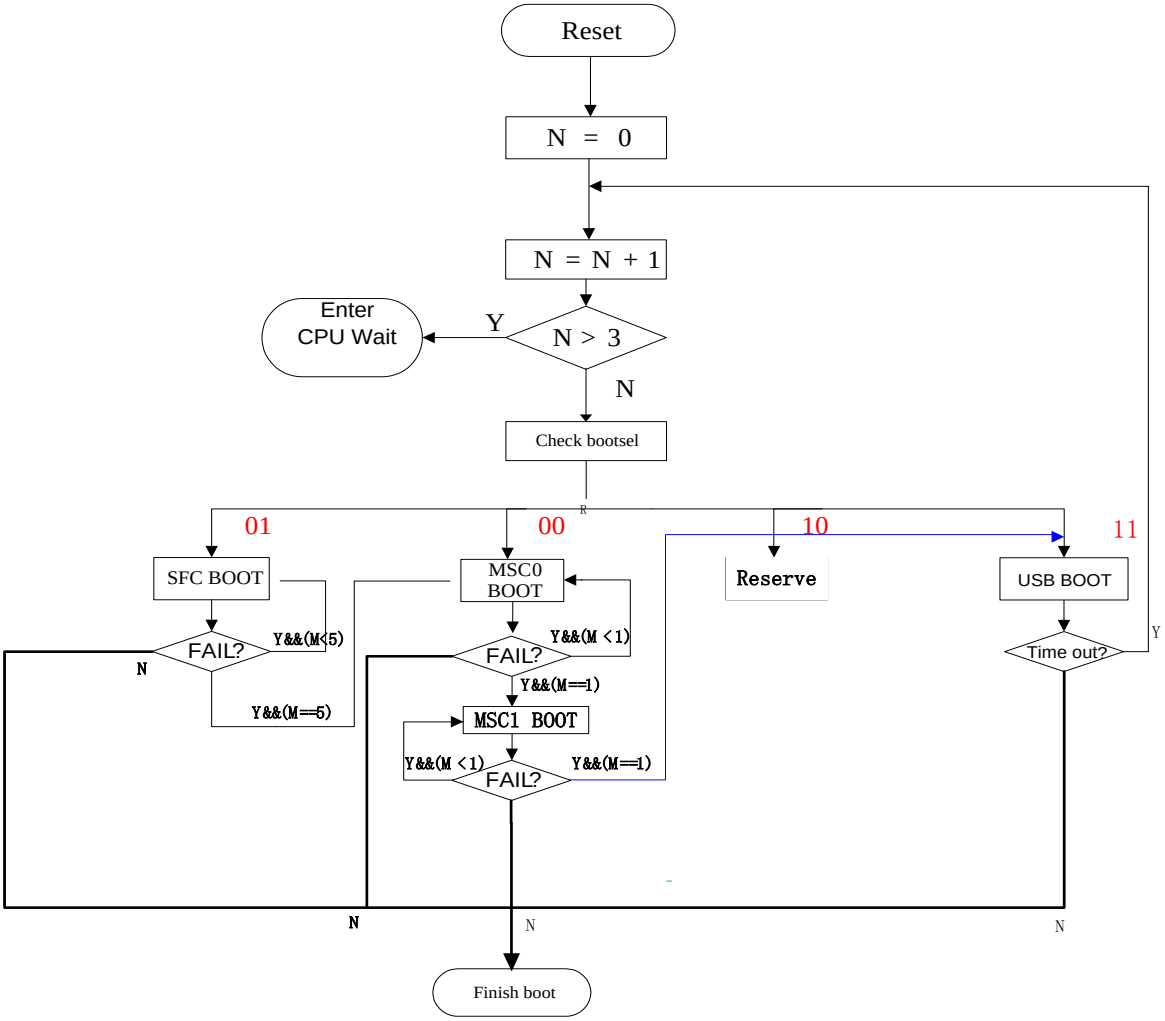


Figure 3-2 Boot sequence diagram of T31A

As shown in boot sequence Block Diagram，After reset, the boot program on the internal boot ROM executes as follows:

1 Disable all interrupts and read boot_sel[1:0] to determine the boot method.

2 There 26KB backup reading failed, the 26KB backup at 128th, 256 th , …, and finally 1024th page will be tried in consecutive order.

3 If it is boot from MMC/SD card at MSC0, its function pins MSC0_D0, MSC0_CLK, MSC0_CMD are initialized, the boot program loads the maximum 100KB code from MMC/SD card to cache and jump to it. Only one data bus which is MSC0_D0 is used.

4 If it is boot from USB, a block of code will be received through USB cable connected with host PC and be stored in cache. Then branch to this area in cache.

5 If it is boot from SPI nor/nand at SFC, its function pins SFC_CLK,SFC_CE, SFC_DR,SFC_DT, SFC_WP,SFC_HOLD are initialized,the boot program loads the maximum 100KB code from SPI NAND/NOR flash to cache and jump to it.

6 If it is boot from NOR Flash, the boot program jump to nor and run directory.