

# NB6L72

## 2.5V / 3.3V Differential 2 X 2 Crosspoint Switch with LVPECL Outputs

### Multi-Level Inputs w/ Internal Termination

#### Description

The NB6L72 is a clock or data high-bandwidth fully differential 2 x 2 Crosspoint Switch with internal source termination and LVPECL output structure, optimized for low skew and minimal jitter. The differential inputs incorporate internal 50  $\Omega$  termination resistors and will accept LVPECL, CML, LVDS, LVCMOS, or LVTTL logic levels. The SELECT inputs are single-ended and can be driven with LVCMOS/LVTTL.

The differential LVPECL outputs provide 800 mV output swings when externally terminated with a 50  $\Omega$  resistor to  $V_{CC}$  — 2.0 V.

The device is offered in a small 3 mm x 3 mm 16-pin QFN package.

The NB6L72 is a member of the ECLinPS MAX™ family of high performance clock and data management products.

#### Features

- Input Clock Frequency > 3.0GHz
- Input Data Rate > 3 Gb/s
- 425 ps Typical Propagation Delay
- 100 ps Typical Rise and Fall Times
- 0.5 ps maximum RMS Clock Jitter
- LVPECL, CML or LVDS Input Compatible
- Differential LVPECL Outputs, 800 mV Amplitude, Typical
- Operating Range:  $V_{CC}$  = 2.375 V to 3.63 V with GND = 0 V
- Internal 50  $\Omega$  Input Termination Provided
- Functionally Compatible with Existing 2.5 V/3.3 V LVEL, LVEP, EP, and SG Devices
- -40°C to +85°C Ambient Operating Temperature
- These are Pb-Free Devices



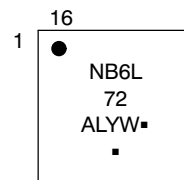
ON Semiconductor®

<http://onsemi.com>

#### MARKING DIAGRAM\*



QFN-16  
MN SUFFIX  
CASE 485G



A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
▪ = Pb-Free Package  
(Note: Microdot may be in either location)

\*For additional marking information, refer to  
Application Note AND8002/D.

#### ORDERING INFORMATION

See detailed ordering and shipping information in the package  
dimensions section on page 10 of this data sheet.

# NB6L72

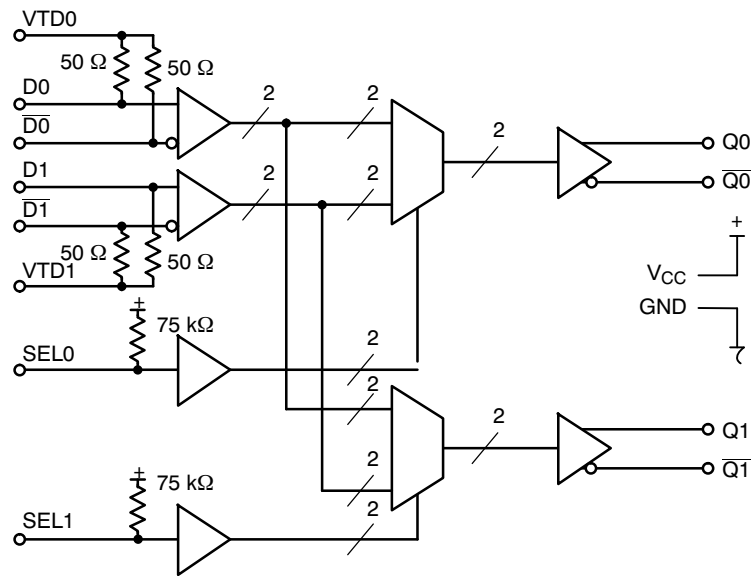
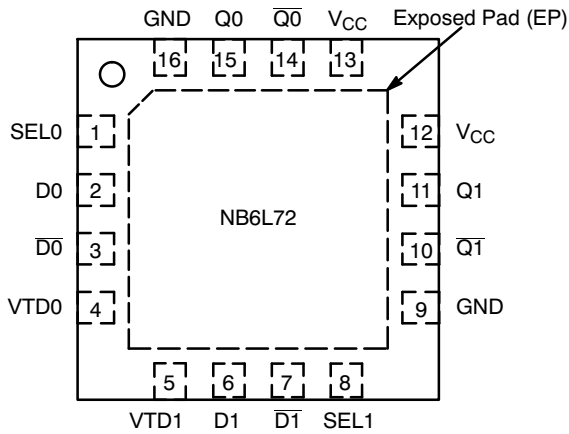


Figure 1. Logic/Block Diagram

## NB6L72



**Table 1. INPUT/OUTPUT SELECT TRUTH TABLE**

| SEL0* | SEL1* | Q0 | Q1 |
|-------|-------|----|----|
| L     | L     | D0 | D0 |
| H     | L     | D1 | D0 |
| L     | H     | D0 | D1 |
| H     | H     | D1 | D1 |

\*Defaults HIGH when left open

**Figure 2. Pin Configuration (Top View)**

**Table 2. PIN DESCRIPTION**

| Pin | Name | I/O                                      | Description                                                                                                                                                                                                                                                                                                                        |
|-----|------|------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1   | SEL0 | LVTTTL, LVCMOS Input                     | Select Logic Input control that selects D0 or D1 to output Q0. See Table 1, Select Input Function Table. Pin defaults HIGH when left open                                                                                                                                                                                          |
| 2   | D0   | LVPECL, CML, LVDS, LVTTTL, LVCMOS, Input | Noninverted Differential Input. Note 1.                                                                                                                                                                                                                                                                                            |
| 3   | D0   | LVPECL, CML, LVDS, LVTTTL, LVCMOS, Input | Inverted Differential Input. Note 1.                                                                                                                                                                                                                                                                                               |
| 4   | VTD0 | -                                        | Internal 50 $\Omega$ Termination Pin. Note 1.                                                                                                                                                                                                                                                                                      |
| 5   | VTD1 | -                                        | Internal 50 $\Omega$ termination pin. Note 1.                                                                                                                                                                                                                                                                                      |
| 6   | D1   | LVPECL, CML, LVDS, LVTTTL, LVCMOS, Input | Noninverted Differential Input. Note 1.                                                                                                                                                                                                                                                                                            |
| 7   | D1   | LVPECL, CML, LVDS, LVTTTL, LVCMOS, Input | Inverted Differential Input. Note 1.                                                                                                                                                                                                                                                                                               |
| 8   | SEL1 | LVTTTL, LVCMOS Input                     | Select Logic Input control that selects D0 or D1 to output Q1. See Table 1, Select Input Function Table. Pin defaults HIGH when left open                                                                                                                                                                                          |
| 9   | GND  | -                                        | Negative Supply Voltage                                                                                                                                                                                                                                                                                                            |
| 10  | Q1   | LVPECL Output                            | Inverted Differential Output. Typically Terminated with 50 $\Omega$ Resistor to $V_{CC} - 2.0$ V.                                                                                                                                                                                                                                  |
| 11  | Q1   | LVPECL Output                            | Noninverted Differential Output. Typically Terminated with 50 $\Omega$ Resistor to $V_{CC} - 2.0$ V.                                                                                                                                                                                                                               |
| 12  | VCC  | -                                        | Positive Supply Voltage                                                                                                                                                                                                                                                                                                            |
| 13  | VCC  | -                                        | Positive Supply Voltage                                                                                                                                                                                                                                                                                                            |
| 14  | Q0   | LVPECL Output                            | Inverted Differential Reset Input. Typically Terminated with 50 $\Omega$ Resistor to $V_{CC} - 2.0$ V.                                                                                                                                                                                                                             |
| 15  | Q0   | LVPECL Output                            | Noninverted Differential Reset Input. Typically Terminated with 50 $\Omega$ Resistor to $V_{CC} - 2.0$ V.                                                                                                                                                                                                                          |
| 16  | GND  | -                                        | Negative Supply Voltage                                                                                                                                                                                                                                                                                                            |
| -   | EP   | -                                        | The Exposed Pad (EP) on the QFN-16 package bottom is thermally connected to the die for improved heat transfer out of package. The exposed pad must be attached to a heat-sinking conduit. The pad is not electrically connected to the die, but is recommended to be electrically and thermally connected to GND on the PC board. |

1. In the differential configuration when the input termination pin ( $VTD_n$ ,  $\overline{VTD}_n$ ) are connected to a common termination voltage or left open, and if no signal is applied on  $D_n/\overline{D}_n$  input, then the device will be susceptible to self-oscillation.
2. All  $V_{CC}$  and GND pins must be externally connected to a power supply for proper operation.

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**Table 3. ATTRIBUTES**

| Characteristics                                        | Value                |
|--------------------------------------------------------|----------------------|
| ESD Protection Human Body Model<br>Machine Model       | > 2 kV<br>> 200 V    |
| Moisture Sensitivity 16-QFN                            | Level 1              |
| Flammability Rating Oxygen Index: 28 to 34             | UL 94 V-0 @ 0.125 in |
| Transistor Count                                       |                      |
| Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test |                      |

For additional information, see Application Note AND8003/D.

**Table 4. MAXIMUM RATINGS**

| Symbol            | Parameter                                                   | Condition 1         | Condition 2                          | Rating                | Unit         |
|-------------------|-------------------------------------------------------------|---------------------|--------------------------------------|-----------------------|--------------|
| V <sub>CC</sub>   | Positive Power Supply                                       | GND = 0 V           |                                      | 4.0                   | V            |
| V <sub>IO</sub>   | Positive Input/Output Voltage                               | GND = 0 V           | $-0.5 \leq V_{IO} \leq V_{CC} + 0.5$ | 4.5                   | V            |
| V <sub>INPP</sub> | Differential Input Voltage  D - $\bar{D}$                   |                     |                                      | V <sub>CC</sub> - GND | V            |
| I <sub>IN</sub>   | Input Current Through R <sub>T</sub> (50 $\Omega$ Resistor) | Static<br>Surge     |                                      | 45<br>80              | mA<br>mA     |
| I <sub>OUT</sub>  | Output Current (LVPECL Output)                              | Continuous<br>Surge |                                      | 50<br>100             | mA<br>mA     |
| T <sub>A</sub>    | Operating Temperature Range                                 | QFN-16              |                                      | -40 to +85            | °C           |
| T <sub>stg</sub>  | Storage Temperature Range                                   |                     |                                      | -65 to +150           | °C           |
| $\theta_{JA}$     | Thermal Resistance (Junction-to-Ambient) (Note 3)           | 0 lfpm<br>500 lfpm  | QFN-16<br>QFN-16                     | 42<br>35              | °C/W<br>°C/W |
| $\theta_{JC}$     | Thermal Resistance (Junction-to-Case)                       | (Note 3)            | QFN-16                               | 4                     | °C/W         |
| T <sub>sol</sub>  | Wave Solder Pb-Free                                         |                     |                                      | 265                   | °C           |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

3. JEDEC standard multilayer board - 2S2P (2 signal, 2 power) with 8 filled thermal vias under exposed pad.

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**Table 5. DC CHARACTERISTICS, Multi-Level Inputs**  $V_{CC} = 2.375 \text{ V to } 3.63 \text{ V}$ ,  $GND = 0 \text{ V}$ ,  $T_A = -40^\circ\text{C to } +85^\circ\text{C}$

| Symbol | Characteristic | Min | Typ | Max | Unit |
|--------|----------------|-----|-----|-----|------|
|--------|----------------|-----|-----|-----|------|

## POWER SUPPLY CURRENT

|          |                                                |    |    |    |    |
|----------|------------------------------------------------|----|----|----|----|
| $I_{CC}$ | Power Supply Current (Inputs and Outputs Open) | 40 | 60 | 80 | mA |
|----------|------------------------------------------------|----|----|----|----|

## LVPECL OUTPUTS (Notes 4 and 5)

|          |                                                                             |                                 |                                |                                |    |
|----------|-----------------------------------------------------------------------------|---------------------------------|--------------------------------|--------------------------------|----|
| $V_{OH}$ | Output HIGH Voltage<br>$V_{CC} = 3.3 \text{ V}$<br>$V_{CC} = 2.5 \text{ V}$ | $V_{CC} - 1075$<br>2225<br>1425 | $V_{CC} - 950$<br>2350<br>1550 | $V_{CC} - 825$<br>2475<br>1675 | mV |
| $V_{OL}$ | Output LOW Voltage<br>$V_{CC} = 3.3 \text{ V}$<br>$V_{CC} = 2.5 \text{ V}$  | $V_{CC} - 1825$<br>1475<br>675  | $V_{CC} - 1725$<br>1575<br>775 | $V_{CC} - 1625$<br>1675<br>875 | mV |

## DIFFERENTIAL INPUT DRIVEN SINGLE-ENDED (see Figures 4 and 5) (Note 6)

|           |                                                            |                |  |                |    |
|-----------|------------------------------------------------------------|----------------|--|----------------|----|
| $V_{th}$  | Input Threshold Reference Voltage Range (Note 7)           | 1125           |  | $V_{CC} - 150$ | mV |
| $V_{IH}$  | Single-ended Input HIGH Voltage                            | $V_{th} + 150$ |  | $V_{CC}$       | mV |
| $V_{IL}$  | Single-ended Input LOW Voltage                             | GND            |  | $V_{th} - 150$ | mV |
| $V_{ISE}$ | Single-ended Input Voltage Amplitude ( $V_{IH} - V_{IL}$ ) | 300            |  | $V_{CC} - GND$ | mV |

## DIFFERENTIAL INPUTS DRIVEN DIFFERENTIALLY (see Figures 7 and 9)

|           |                                                                              |      |  |                |               |
|-----------|------------------------------------------------------------------------------|------|--|----------------|---------------|
| $V_{IHD}$ | Differential Input HIGH Voltage                                              | 1050 |  | $V_{CC}$       | mV            |
| $V_{ILD}$ | Differential Input LOW Voltage                                               | GND  |  | $V_{CC} - 150$ | mV            |
| $V_{ID}$  | Differential Input Voltage ( $D_n, \overline{D_n}$ ) ( $V_{IHD} - V_{ILD}$ ) | 150  |  | $V_{CC} - GND$ | mV            |
| $V_{CMR}$ | Input Common Mode Range (Differential Configuration) (Note 9)                | 950  |  | $V_{CC} - 75$  | mV            |
| $I_{IH}$  | Input HIGH Current $D_n/\overline{D_n}$ , (VTDn/VTDn Open)                   | -150 |  | +150           | $\mu\text{A}$ |
| $I_{IL}$  | Input LOW Current $D_n/\overline{D_n}$ , (VTDn/VTDn Open)                    | -150 |  | +150           | $\mu\text{A}$ |

## SINGLE-ENDED LVCMOS/LVTTL CONTROL INPUTS

|          |                                 |      |  |          |               |
|----------|---------------------------------|------|--|----------|---------------|
| $V_{IH}$ | Single-ended Input HIGH Voltage | 2000 |  | $V_{CC}$ | mV            |
| $V_{IL}$ | Single-ended Input LOW Voltage  | GND  |  | 800      | mV            |
| $I_{IH}$ | Input HIGH Current              | -10  |  | 10       | $\mu\text{A}$ |
| $I_{IL}$ | Input LOW Current               | -150 |  | 0        | $\mu\text{A}$ |

## TERMINATION RESISTORS

|           |                                     |    |    |    |          |
|-----------|-------------------------------------|----|----|----|----------|
| $R_{TIN}$ | Internal Input Termination Resistor | 40 | 50 | 60 | $\Omega$ |
|-----------|-------------------------------------|----|----|----|----------|

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

- LVPECL outputs loaded with  $50 \Omega$  to  $V_{CC} - 2.0 \text{ V}$  for proper operation.
- Input and output parameters vary 1:1 with  $V_{CC}$ .
- $V_{th}$ ,  $V_{IH}$ ,  $V_{IL}$ , and  $V_{ISE}$  parameters must be complied with simultaneously.
- $V_{th}$  is applied to the complementary input when operating in single-ended mode.
- $V_{IHD}$ ,  $V_{ILD}$ ,  $V_{ID}$  and  $V_{CMR}$  parameters must be complied with simultaneously.
- $V_{CMR}$  minimum varies 1:1 with GND,  $V_{CMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{CMR}$  range is referenced to the most positive side of the differential input signal.

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**Table 6. AC CHARACTERISTICS**  $V_{CC} = 2.375 \text{ V}$  to  $3.63 \text{ V}$ ,  $V_{EE} = 0 \text{ V}$ , or  $V_{CC} = 0 \text{ V}$ ,  $V_{EE} = -2.375 \text{ V}$  to  $-3.63 \text{ V}$ ,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ; (Note 10)

| Symbol                   | Characteristic                                                                                                                                                                           | Min               | Typ                    | Max            | Unit |
|--------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------|------------------------|----------------|------|
| $V_{OUTPP}$              | Output Voltage Amplitude (@ $V_{INPPmin}$ )<br>(Note 14) (See Figure 16)<br>$f_{in} \leq 1.5 \text{ GHz}$<br>$f_{in} \leq 2.5 \text{ GHz}$<br>$f_{in} \leq 3.0 \text{ GHz}$              | 520<br>380<br>320 | 800<br>650<br>500      |                | mV   |
| $t_{PLH}$ ,<br>$t_{PHL}$ | Propagation Delay (@0.5GHz)<br>Dn to Qn<br>SELn to Qn                                                                                                                                    | 325               | 425                    | 525            | ps   |
| $t_{SKEW}$               | Duty Cycle Skew (Note 11)<br>Within Device Skew<br>Device to Device Skew (Note 12)                                                                                                       |                   | 5                      | 20<br>20<br>80 | ps   |
| $t_{DC}$                 | Output Clock Duty Cycle<br>(Reference Duty Cycle = 50%)<br>$f_{in} \leq 3.0 \text{ GHz}$                                                                                                 | 40                | 50                     | 60             | %    |
| $t_{JITTER}$             | RMS Random Clock Jitter (Note 13)<br>Data Dependent Jitter<br>$f_{in} = 2.5 \text{ GHz}$<br>$f_{in} = 3.0 \text{ GHz}$<br>$f_{DATA} = 2.5 \text{ Gb/s}$<br>$f_{DATA} = 3.0 \text{ Gb/s}$ |                   | 0.2<br>0.3<br>12<br>15 | 0.5<br>1       | ps   |
| $V_{INPP}$               | Input Voltage Swing/Sensitivity<br>(Differential Configuration) (Note 14)                                                                                                                | 150               |                        | $V_{CC} - GND$ | mV   |
| $t_r, t_f$               | Output Rise/Fall Times @ 0.5 GHz (20% – 80%)<br>Q, $\bar{Q}$                                                                                                                             |                   | 100                    | 160            | ps   |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

10. Measured by forcing  $V_{INPP}$  (minimum) from a 50% duty cycle clock source. All loading with an external  $R_L = 50 \Omega$  to  $V_{CC} - 2.0 \text{ V}$ . Input edge rates 40 ps (20% – 80%).

11. Duty cycle skew is measured between differential outputs using the deviations of the sum of  $T_{pw-}$  and  $T_{pw+}$  @ 0.5 GHz.

12. Device to device skew is measured between outputs under identical transition @ 0.5 GHz.

13. Additive RMS jitter with 50% duty cycle clock signal.

14. Input and output voltage swing is a single-ended measurement operating in differential mode.

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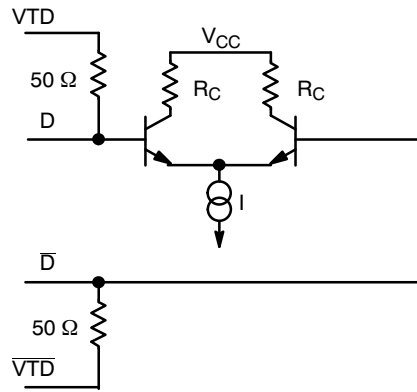


Figure 3. Input Structure

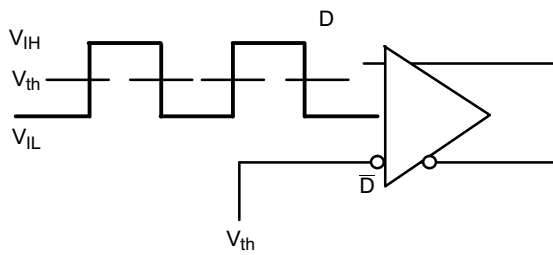


Figure 4. Differential Input Driven Single-Ended

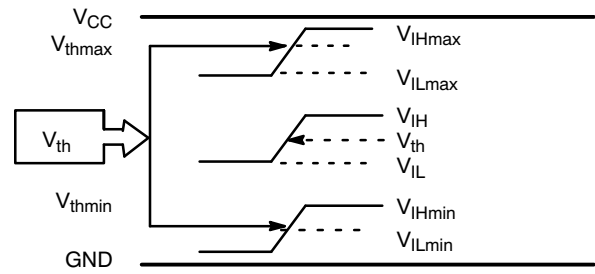


Figure 5.  $V_{th}$  Diagram

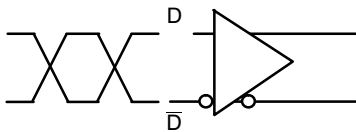


Figure 6. Differential Inputs Driven Differentially

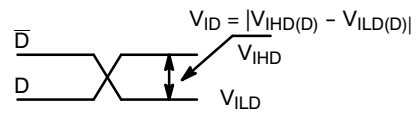


Figure 7. Differential Inputs Driven Differentially

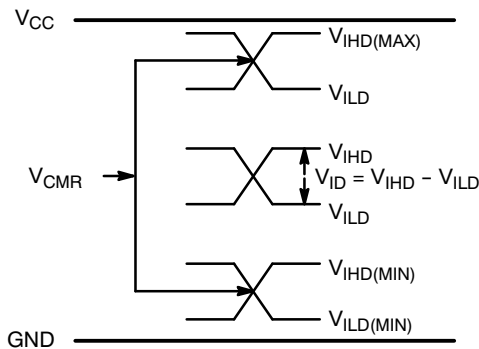


Figure 8.  $V_{CMR}$  Diagram

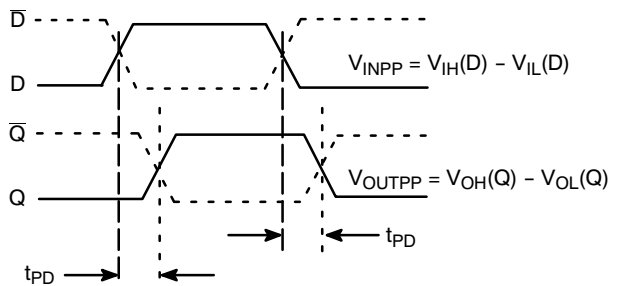


Figure 9. AC Reference Measurement

## NB6L72

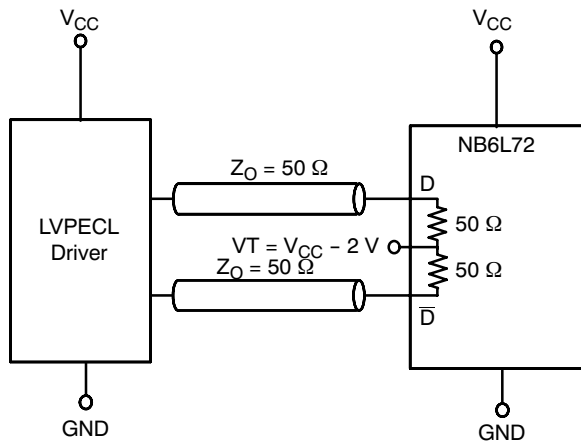


Figure 10. LVPECL Interface

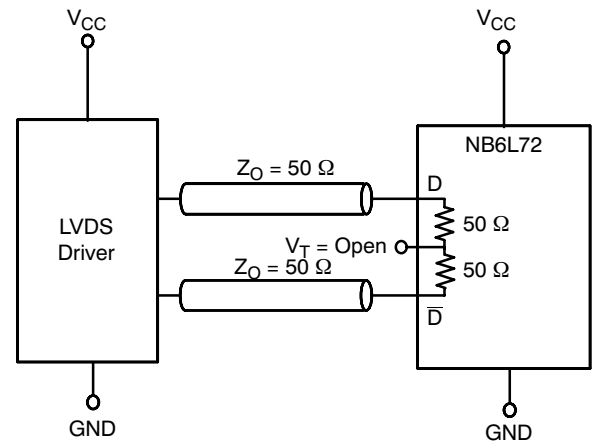


Figure 11. LVDS Interface

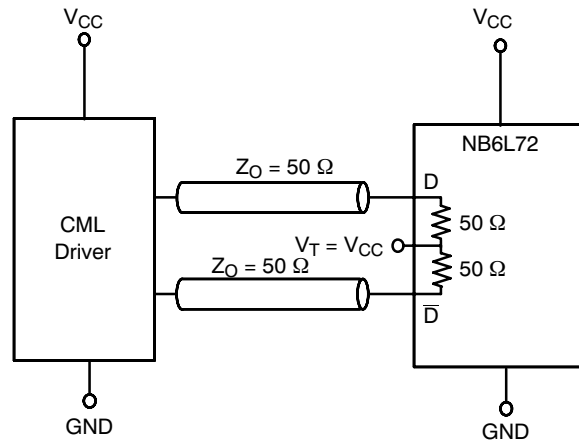


Figure 12. Standard  $50\ \Omega$  Load CML Interface

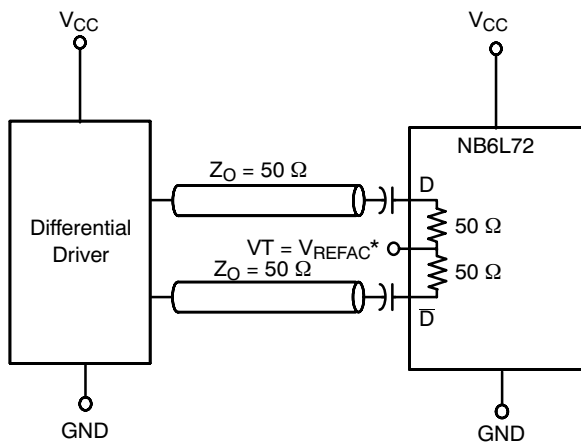


Figure 13. Capacitor-Coupled  
Differential Interface  
( $V_T$  Connected to  $V_{REFAC}$ )

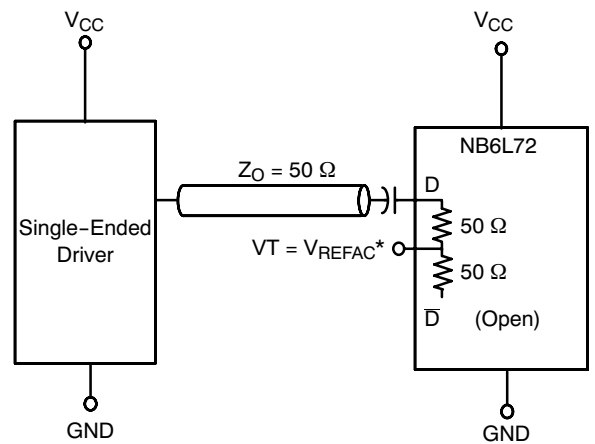
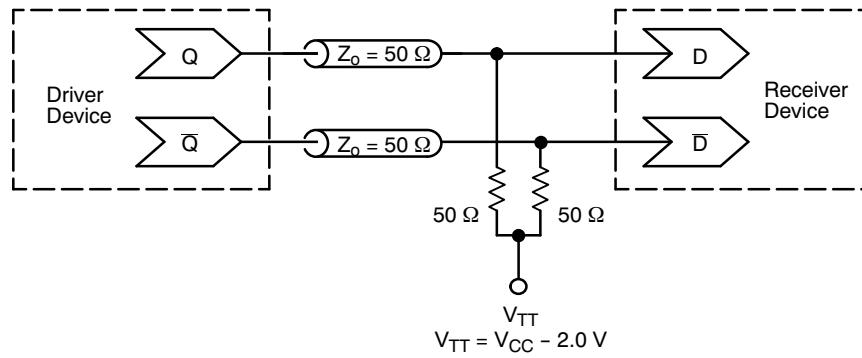


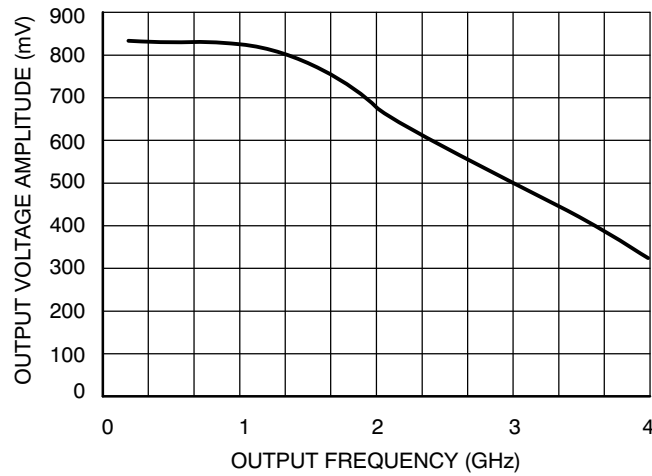
Figure 14. Capacitor-Coupled  
Single-Ended Interface  
( $V_T$  Connected to  $V_{REFAC}$ )

\* $V_{REFAC}$  bypassed to ground with a  $0.01\ \mu\text{F}$  capacitor

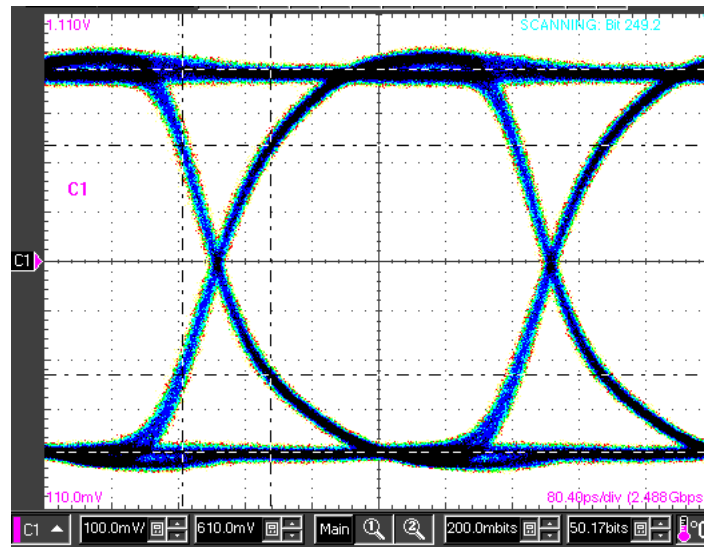
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**Figure 15. Typical Termination for Output Driver and Device Evaluation**  
(See Application Note AND8020/D – Termination of ECL Logic Devices.)

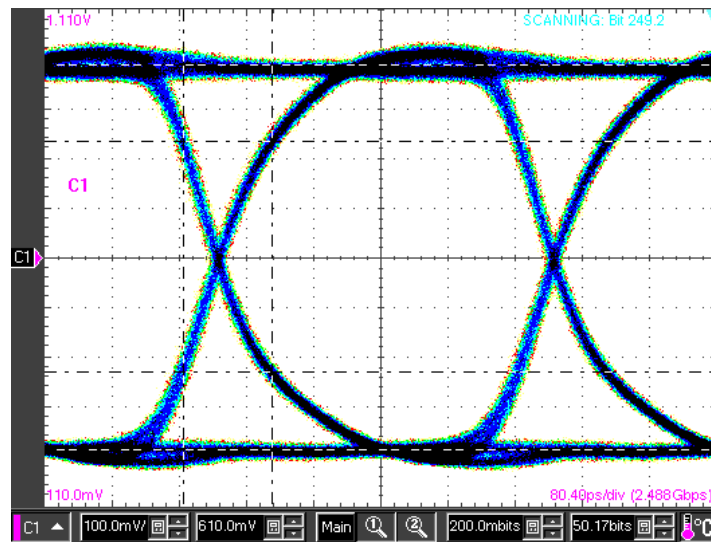


**Figure 16. Output Voltage Amplitude ( $V_{OUTPP}$ ) versus Output Frequency at Ambient Temperature (Typical)**



**Figure 17. Typical Output Wave Form – Data Signal PRBS 2<sup>23</sup>-1 Room Temperature, 400 mV Input Amplitude,  $V_{CC} = 2.5 \text{ V}$ , 2.488 Gb/s (X-scale = 80 ps/DIV; y-Scale = 100 mV/DIV)**

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Total Jitter = 28 ps  
Device Jitter = 15 ps  
Input Jitter = 13 ps

Figure 18. Typical Output Wave Form – Data Signal PRBS 2<sup>23</sup>-1 Room Temperature, 75 mV Input Amplitude, 3 Gb/s (X-scale = 80 ps/DIV; y-Scale = 100 mV/DIV)

### ORDERING INFORMATION

| Device      | Package             | Shipping <sup>†</sup> |
|-------------|---------------------|-----------------------|
| NB6L72MNG   | QFN-16<br>(Pb-free) | 123 Units / Rail      |
| NB6L72MNR2G | QFN-16<br>(Pb-free) | 3000 / Tape & Reel    |

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

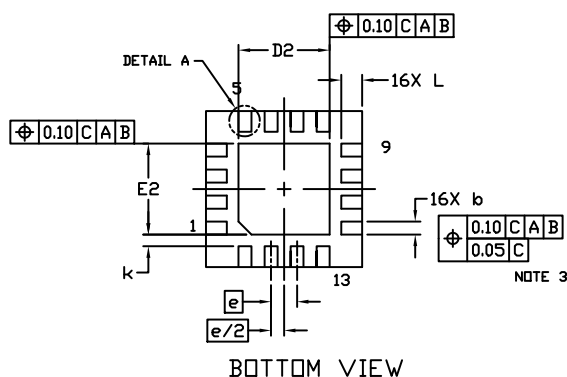
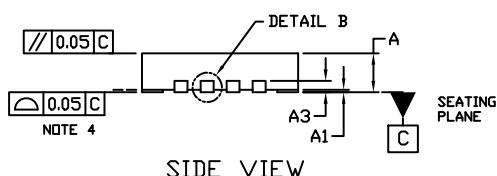
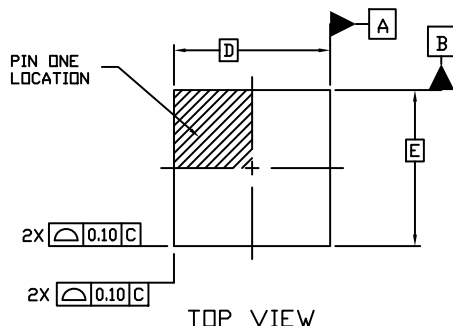
# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 2:1

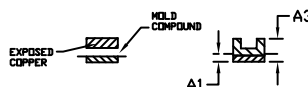
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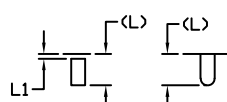


### NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.



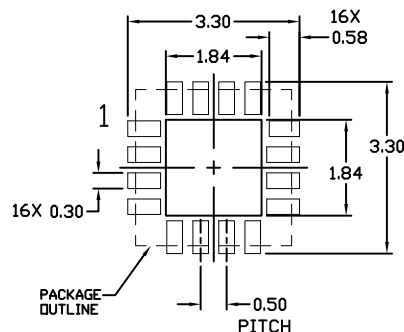
DETAIL B  
ALTERNATE  
CONSTRUCTIONS



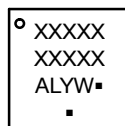
DETAIL A  
ALTERNATE TERMINAL  
CONSTRUCTIONS

| DIM | MILLIMETERS |      |      |
|-----|-------------|------|------|
|     | MIN.        | NDM. | MAX. |
| A   | 0.80        | 0.90 | 1.00 |
| A1  | 0.00        | 0.03 | 0.05 |
| A3  | 0.20 REF    |      |      |
| b   | 0.18        | 0.24 | 0.30 |
| D   | 3.00 BSC    |      |      |
| D2  | 1.65        | 1.75 | 1.85 |
| E   | 3.00 BSC    |      |      |
| E2  | 1.65        | 1.75 | 1.85 |
| e   | 0.50 BSC    |      |      |
| k   | 0.18 TYP    |      |      |
| L   | 0.30        | 0.40 | 0.50 |
| L1  | 0.00        | 0.08 | 0.15 |

### MOUNTING FOOTPRINT



### GENERIC MARKING DIAGRAM\*



XXXXX = Specific Device Code  
A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

|                  |                 |                                                                                                                                                                                     |
|------------------|-----------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
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| DESCRIPTION:     | QFN16 3X3, 0.5P | PAGE 1 OF 1                                                                                                                                                                         |

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