

# SN74AUP1G32 Low-Power Single 2-Input Positive-OR Gate

## 1 Features

- Available in the ultra-small 0.64 mm<sup>2</sup> package (DPW) with 0.5-mm pitch
- Low static-power consumption ( $I_{CC} = 0.9 \mu A$  Max)
- Low dynamic-power consumption ( $C_{pd} = 4.3 \text{ pF}$  Typ at 3.3 V)
- Low input capacitance ( $C_I = 1.5 \text{ pF}$  Typ)
- Low noise – overshoot and undershoot <10% of  $V_{CC}$
- $I_{off}$  Supports live insertion, partial-power-down mode, and back drive protection
- Input hysteresis allows slow input transition and better switching noise immunity at the input ( $V_{hys} = 250 \text{ mV}$  typ at 3.3 V)
- Wide operating  $V_{CC}$  range of 0.8 V to 3.6 V
- Optimized for 3.3-V operation
- 3.6-V I/O Tolerant to support mixed-mode signal operation
- $t_{pd} = 4.6 \text{ ns}$  Max at 3.3 V
- Suitable for point-to-point applications
- Latch-up performance exceeds 100 mA Per JESD 78, Class II
- ESD performance tested Per JESD 22
  - 2000-V Human-body model (A114-B, Class II)
  - 1000-V Charged-device model (C101)

## 2 Applications

- ATCA solutions
- Active noise cancellation (ANC)
- Barcode scanner the end of the datasheet.
- Blood pressure monitor
- CPAP machine
- Cable solutions
- DLP 3D machine vision, hyperspectral imaging, optical networking, and spectroscopy
- E-Book
- Embedded PC
- Field transmitter: temperature or pressure sensor
- Fingerprint biometrics
- HVAC: heating, ventilating, and air conditioning
- Network-attached storage (NAS)
- Server motherboard and PSU
- Software defined radio (SDR)
- TV: high-definition (HDTV), LCD, and Digital
- Video communications system
- Wireless data access card, headset, keyboard, mouse, and LAN card
- X-ray: baggage scanner, medical, and dental

## 3 Description

This single 2-input positive-OR gate performs the Boolean function  $Y = A \bullet B$  or  $Y = \overline{\overline{A} + \overline{B}}$  in positive logic.

## Device Information

PART NUMBER	PACKAGE <sup>(1)</sup>	BODY SIZE (NOM)
SN74AUP1G32	SOT (5)	1.60 mm × 1.20 mm
	USON (6)	1.45 mm × 1.00 mm
	X2SON (4)	0.80 mm × 0.80 mm
	DSBGA (6)	1.19 mm × 0.79 mm
	DSBGA (5)	1.41 mm × 0.91 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



**Simplified Schematic**



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

## Table of Contents

<b>1 Features</b> .....	<b>1</b>	<b>8 Detailed Description</b> .....	<b>11</b>
<b>2 Applications</b> .....	<b>1</b>	8.1 Overview.....	11
<b>3 Description</b> .....	<b>1</b>	8.2 Functional Block Diagram.....	11
<b>4 Revision History</b> .....	<b>2</b>	8.3 Feature Description.....	11
<b>5 Pin Configuration and Functions</b> .....	<b>3</b>	8.4 Device Functional Modes.....	11
<b>6 Specifications</b> .....	<b>4</b>	<b>9 Application and Implementation</b> .....	<b>12</b>
6.1 Absolute Maximum Ratings.....	4	9.1 Application Information.....	12
6.2 Handling Ratings.....	4	9.2 Typical Application.....	12
6.3 Recommended Operating Conditions.....	4	<b>10 Power Supply Recommendations</b> .....	<b>13</b>
6.4 Thermal Information.....	5	<b>11 Layout</b> .....	<b>13</b>
6.5 Electrical Characteristics.....	6	11.1 Layout Guidelines.....	13
6.6 Switching Characteristics, $C_L = 5 \text{ pF}$ .....	6	11.2 Layout Example.....	13
6.7 Switching Characteristics, $C_L = 10 \text{ pF}$ .....	7	<b>12 Device and Documentation Support</b> .....	<b>14</b>
6.8 Switching Characteristics, $C_L = 15 \text{ pF}$ .....	7	12.1 Receiving Notification of Documentation Updates.....	14
6.9 Switching Characteristics, $C_L = 30 \text{ pF}$ .....	7	12.2 Support Resources.....	14
6.10 Operating Characteristics.....	8	12.3 Trademarks.....	14
6.11 Typical Characteristics.....	8	12.4 Electrostatic Discharge Caution.....	14
<b>7 Parameter Measurement Information</b> .....	<b>9</b>	12.5 Glossary.....	14
7.1 Propagation Delays, Setup and Hold Times, and Pulse Width.....	9	<b>13 Mechanical, Packaging, and Orderable Information</b> .....	<b>14</b>
7.2 Enable and Disable Times.....	10		

## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Revision J (September 2019) to Revision K (May 2020)</b>	<b>Page</b>
• Corrected DPW package image description to "DPW Package X2SON 5-pins (Transparent Top View)".....	3
• Updated DPW package image.....	3
<hr/>	
<b>Changes from Revision I (June 2014) to Revision J (September 2019)</b>	<b>Page</b>
• Changed format of Pin Configuration images to allow for HTML search function .....	3
• Corrected YFP package pin descriptors in the Pin Functions table .....	3
• Added Thermal Information for the DPW package .....	5
<hr/>	
<b>Changes from Revision H (August 2012) to Revision I (June 2014)</b>	<b>Page</b>
• Updated document to new TI data sheet format.....	1
• Removed Ordering Information table.....	1
• Added Applications.....	1
• Added Handling Ratings table.....	4
• Added Thermal Information table.....	5
• Added Typical Characteristics.....	8

## 5 Pin Configuration and Functions

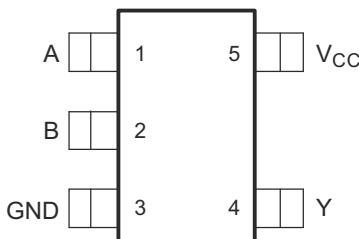


Figure 5-1. DBV Package SOT 5-pin (Top View)

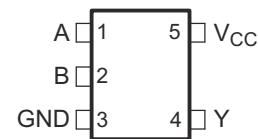


Figure 5-2. DRL Package SOT 5-pin (Top View)

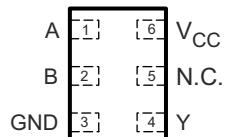


Figure 5-3. DSF Package SON 6-pin (Transparent Top View)

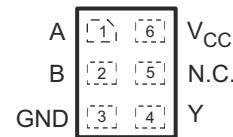


Figure 5-4. DRY Package SON 6-pin (Transparent Top View)

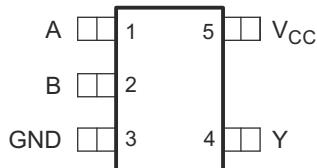


Figure 5-5. DCK Package SC70 5-pin (Top View)

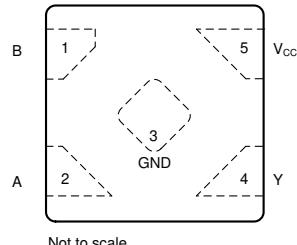
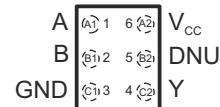


Figure 5-6. YZP Package DSBGA 5-balls (Transparent Top View)



Not to scale

See mechanical drawings at the end of the data sheet for all package dimensions

Figure 5-7. DPW Package X2SON 5-pins (Transparent Top View)

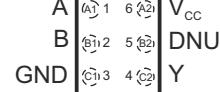


Figure 5-8. YFP Package DSBGA 6-balls (Transparent Top View)

## Pin Functions

PIN						I/O	DESCRIPTION
NAME	DRL, DCK, DBV	DPW	DRY, DSF	YZP	YFP		
A	1	2	1	A1	A1	I	Input A
B	2	1	2	B1	B1	I	Input B
GND	3	3	3	C1	C1	–	Ground
Y	4	4	4	C2	C2	O	Output Y
V <sub>CC</sub>	5	5	6	A2	A2	–	Power Pin

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage range	-0.5	4.6	V
$V_I$	Input voltage range <sup>(2)</sup>	-0.5	4.6	V
$V_O$	Voltage range applied to any output in the high-impedance or power-off state <sup>(2)</sup>	-0.5	4.6	V
$V_O$	Voltage range applied to any output in the high or low state <sup>(2)</sup>	-0.5	$V_{CC} + 0.5$	V
$I_{IK}$	Input clamp current $V_I < 0$		-50	mA
$I_{OK}$	Output clamp current $V_O < 0$		-50	mA
$I_O$	Continuous output current		$\pm 20$	mA
	Continuous current through $V_{CC}$ or GND		$\pm 50$	mA

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

### 6.2 Handling Ratings

		MIN	MAX	UNIT
$T_{stg}$	Storage temperature range	-65	125	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>	0	2000
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup>	0	1000

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

see <sup>(1)</sup>		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	0.8	3.6	V
$V_{IH}$	High-level input voltage	$V_{CC} = 0.8$ V	$V_{CC}$	V
		$V_{CC} = 1.1$ V to 1.95 V	$0.65 \times V_{CC}$	
		$V_{CC} = 2.3$ V to 2.7 V	1.6	
		$V_{CC} = 3$ V to 3.6 V	2	
$V_{IL}$	Low-level input voltage	$V_{CC} = 0.8$ V	0	V
		$V_{CC} = 1.1$ V to 1.95 V	$0.35 \times V_{CC}$	
		$V_{CC} = 2.3$ V to 2.7 V	0.7	
		$V_{CC} = 3$ V to 3.6 V	0.9	
$V_I$	Input voltage	0	3.6	V
$V_O$	Output voltage	0	$V_{CC}$	V
$I_{OH}$	High-level output current	$V_{CC} = 0.8$ V	-20	mA
		$V_{CC} = 1.1$ V	-1.1	
		$V_{CC} = 1.4$ V	-1.7	
		$V_{CC} = 1.65$ V	-1.9	
		$V_{CC} = 2.3$ V	-3.1	
		$V_{CC} = 3$ V	-4	

see <sup>(1)</sup>			MIN	MAX	UNIT
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 0.8 V		20	µA
		V <sub>CC</sub> = 1.1 V		1.1	mA
		V <sub>CC</sub> = 1.4 V		1.7	
		V <sub>CC</sub> = 1.65 V		1.9	
		V <sub>CC</sub> = 2.3 V		3.1	
		V <sub>CC</sub> = 3 V		4	
Δt/Δv	Input transition rise and fall rate	V <sub>CC</sub> = 0.8 V to 1.95 V		200	ns/V
T <sub>A</sub>	Operating free-air temperature		-40	85	°C

(1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

## 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>	DBV	DCK	DRL	DSF	DRY	DPW	UNIT	
	5 PINS	5 PINS	5 PINS	6 PINS	6 PINS	5 PINS		
R <sub>θJA</sub>	Junction-to-ambient thermal resistance (standard data sheet value)	271.4	338.4	349.7	407.1	554.9	492.1	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance (standard data sheet value)	213.5	110.6	120.5	232.0	385.4	232.6	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance (standard data sheet value)	108.2	118.8	171.4	306.9	388.2	355.4	°C/W
Ψ <sub>JT</sub>	Junction-to-top characterization parameter (standard data sheet value)	89.3	3.0	10.8	40.3	159.0	37.4	°C/W
Ψ <sub>JB</sub>	Junction-to-board characterization parameter (standard data sheet value)	107.6	117.8	169.4	306.0	384.1	353.9	°C/W
Ψ <sub>JC(bot)</sub>	Junction-to-case (bottom) thermal resistance (standard data sheet value)	–	–	–	–	–	147.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

## 6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			T <sub>A</sub> = -40°C to 85°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = -20 µA	0.8 V to 3.6 V	V <sub>CC</sub> - 0.1			V <sub>CC</sub> - 0.1		V
	I <sub>OH</sub> = -1.1 mA	1.1 V	0.75 × V <sub>CC</sub>			0.7 × V <sub>CC</sub>		
	I <sub>OH</sub> = -1.7 mA	1.4 V	1.11			1.03		
	I <sub>OH</sub> = -1.9 mA	1.65 V	1.32			1.3		
	I <sub>OH</sub> = -2.3 mA	2.3 V	2.05			1.97		
	I <sub>OH</sub> = -3.1 mA		1.9			1.85		
	I <sub>OH</sub> = -2.7 mA	3 V	2.72			2.67		
	I <sub>OH</sub> = -4 mA		2.6			2.55		
V <sub>OL</sub>	I <sub>OL</sub> = 20 µA	0.8 V to 3.6 V		0.1			0.1	V
	I <sub>OL</sub> = 1.1 mA	1.1 V		0.3 × V <sub>CC</sub>			0.3 × V <sub>CC</sub>	
	I <sub>OL</sub> = 1.7 mA	1.4 V		0.31			0.37	
	I <sub>OL</sub> = 1.9 mA	1.65 V		0.31			0.35	
	I <sub>OL</sub> = 2.3 mA	2.3 V		0.31			0.33	
	I <sub>OL</sub> = 3.1 mA			0.44			0.45	
	I <sub>OL</sub> = 2.7 mA	3 V		0.31			0.33	
	I <sub>OL</sub> = 4 mA			0.44			0.45	
I <sub>I</sub>	A or B input	V <sub>I</sub> = GND to 3.6 V	0 V to 3.6 V		0.1		0.5	µA
I <sub>off</sub>		V <sub>I</sub> or V <sub>O</sub> = 0 V to 3.6 V	0 V		0.2		0.6	µA
ΔI <sub>off</sub>		V <sub>I</sub> or V <sub>O</sub> = 0 V to 3.6 V	0 V to 0.2 V		0.2		0.6	µA
I <sub>CC</sub>		V <sub>I</sub> = GND or (V <sub>CC</sub> to 3.6 V), I <sub>O</sub> = 0	0.8 V to 3.6 V		0.5		0.9	µA
ΔI <sub>CC</sub>		V <sub>I</sub> = V <sub>CC</sub> - 0.6 V <sup>(1)</sup> , I <sub>O</sub> = 0	3.3 V		40		50	µA
C <sub>i</sub>		V <sub>I</sub> = V <sub>CC</sub> or GND	0 V		1.5			pF
			3.6 V		1.5			
C <sub>o</sub>		V <sub>O</sub> = GND	0 V		3			pF

(1) One input at V<sub>CC</sub> - 0.6 V, other input at V<sub>CC</sub> or GND.

## 6.6 Switching Characteristics, C<sub>L</sub> = 5 pF

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 7-1](#) and [Figure 7-2](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub>	T <sub>A</sub> = 25°C			T <sub>A</sub> = -40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
t <sub>pd</sub>	A or B	Y	0.8 V		18				ns
			1.2 V ± 0.1 V	2.6	7.3	13.5	2.1	16.8	
			1.5 V ± 0.1 V	1.4	5.2	9.1	0.9	11	
			1.8 V ± 0.15 V	1	4.2	7	0.5	8.8	
			2.5 V ± 0.2 V	1	3	4.7	0.5	6	
			3.3 V ± 0.3 V	1	2.4	3.7	0.5	4.6	

## 6.7 Switching Characteristics, $C_L = 10 \text{ pF}$

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 7-1](#) and [Figure 7-2](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC}$	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	
$t_{pd}$	A or B	Y	0.8 V		21				ns
			1.2 V $\pm 0.1$ V	1.5	8.5	15.4	1	18.4	
			1.5 V $\pm 0.1$ V	1	6.2	10.4	0.5	12	
			1.8 V $\pm 0.15$ V	1	5	8.1	0.5	9.6	
			2.5 V $\pm 0.2$ V	1	3.6	5.5	0.5	6.6	
			3.3 V $\pm 0.3$ V	1	2.9	4.4	0.5	5	

## 6.8 Switching Characteristics, $C_L = 15 \text{ pF}$

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 7-1](#) and [Figure 7-2](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC}$	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	
$t_{pd}$	A or B	Y	0.8 V		24				ns
			1.2 V $\pm 0.1$ V	3.6	9.9	17	3.1	21.1	
			1.5 V $\pm 0.1$ V	2.3	7.2	11.5	1.8	13.9	
			1.8 V $\pm 0.15$ V	1.6	5.8	9.1	1.1	11.2	
			2.5 V $\pm 0.2$ V	1	4.3	6.2	0.5	7.8	
			3.3 V $\pm 0.3$ V	1	3.4	5	0.5	6.2	

## 6.9 Switching Characteristics, $C_L = 30 \text{ pF}$

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 7-1](#) and [Figure 7-2](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC}$	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	
$t_{pd}$	A or B	Y	0.8 V		32.8				ns
			1.2 V $\pm 0.1$ V	4.9	13.1	21.6	4.4	26.7	
			1.5 V $\pm 0.1$ V	3.4	9.5	14.6	2.9	17.6	
			1.8 V $\pm 0.15$ V	2.5	7.7	11.4	2	14.1	
			2.5 V $\pm 0.2$ V	1.8	5.7	7.9	1.3	9.9	
			3.3 V $\pm 0.3$ V	1.5	4.7	6.4	1	7.8	

## 6.10 Operating Characteristics

$T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	$V_{CC}$	TYP	UNIT
$C_{pd}$	Power dissipation capacitance	$f = 10 \text{ MHz}$	0.8 V	4.1	pF
			$1.2 \text{ V} \pm 0.1 \text{ V}$	4.1	
			$1.5 \text{ V} \pm 0.1 \text{ V}$	4.1	
			$1.8 \text{ V} \pm 0.15 \text{ V}$	4.1	
			$2.5 \text{ V} \pm 0.2 \text{ V}$	4.2	
			$3.3 \text{ V} \pm 0.3 \text{ V}$	4.3	

## 6.11 Typical Characteristics

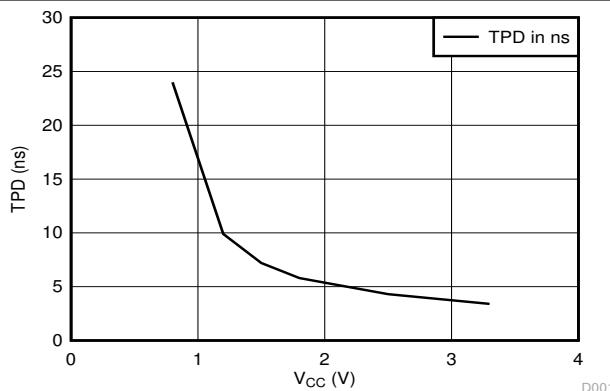


Figure 6-1. TPD vs  $V_{CC}$ , 15 pF Load

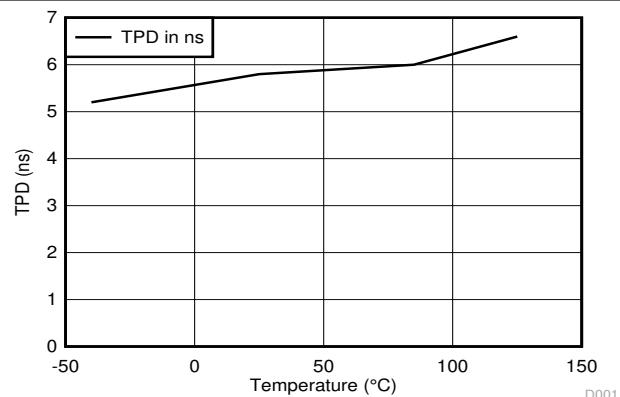
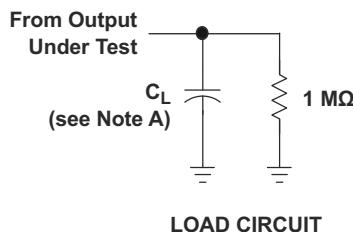


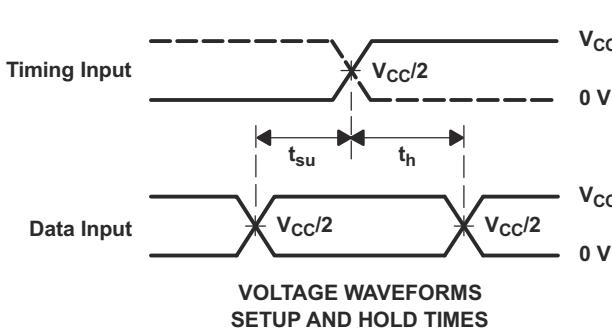
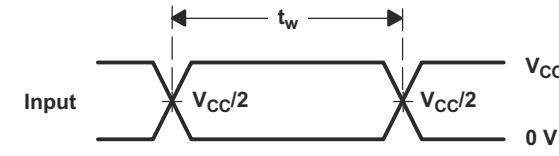
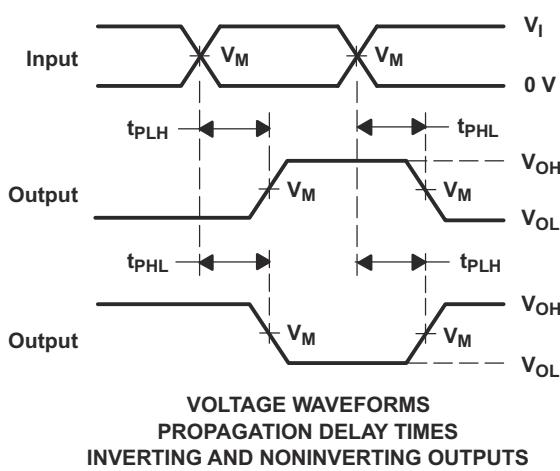
Figure 6-2. Temperature 1.8 V, 15 pF Load

## 7 Parameter Measurement Information

### 7.1 Propagation Delays, Setup and Hold Times, and Pulse Width



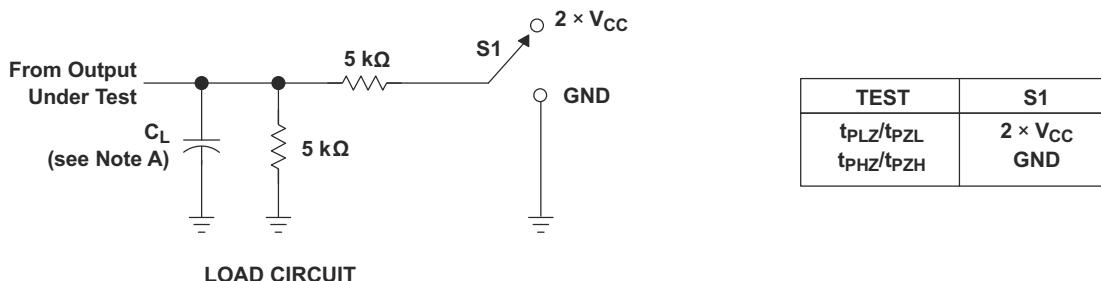
	$V_{CC} = 0.8 \text{ V}$	$V_{CC} = 1.2 \text{ V} \pm 0.1 \text{ V}$	$V_{CC} = 1.5 \text{ V} \pm 0.1 \text{ V}$	$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$	$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$
$C_L$ $V_M$ $V_I$	5, 10, 15, 30 pF $V_{CC}/2$ $V_{CC}$	5, 10, 15, 30 pF $V_{CC}/2$ $V_{CC}$	5, 10, 15, 30 pF $V_{CC}/2$ $V_{CC}$			



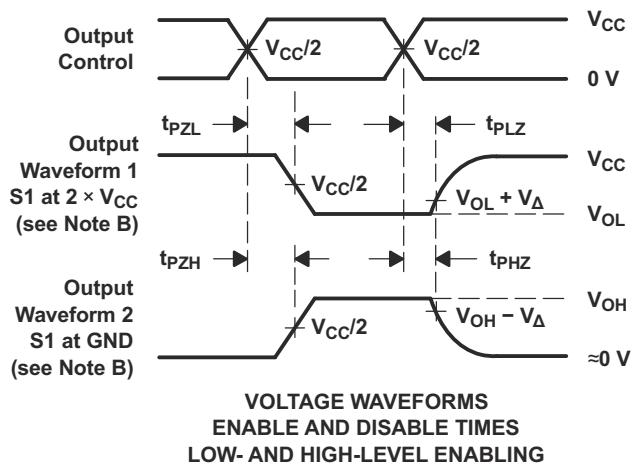
- A.  $C_L$  includes probe and jig capacitance.
- B. All input pulses are supplied by generators having the following characteristics: PRR  $\leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r$  and  $t_f = 3 \text{ ns}$ .
- C. The outputs are measured one at a time, with one transition per measurement.
- D.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
- E. All parameters and waveforms are not applicable to all devices.

**Figure 7-1. Load Circuit and Voltage Waveforms**

## 7.2 Enable and Disable Times



	$V_{CC} = 0.8 \text{ V}$	$V_{CC} = 1.2 \text{ V} \pm 0.1 \text{ V}$	$V_{CC} = 1.5 \text{ V} \pm 0.1 \text{ V}$	$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$	$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$
$C_L$	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
$V_M$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$
$V_I$	$V_{CC}$	$V_{CC}$	$V_{CC}$	$V_{CC}$	$V_{CC}$	$V_{CC}$
$V_D$	0.1 V	0.1 V	0.1 V	0.15 V	0.15 V	0.3 V



- A.  $C_L$  includes probe and jig capacitance.
- C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r$  and  $t_f = 3 \text{ ns}$ .
- D. The outputs are measured one at a time, with one transition per measurement.
- E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
- F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
- G. All parameters and waveforms are not applicable to all devices.

Figure 7-2. Load Circuit and Voltage Waveforms

## 8 Detailed Description

### 8.1 Overview

This single 2-input positive-OR gate that operates from 0.8 V to 3.6 V and performs the Boolean function  $Y = A \bullet B$  or  $Y = \overline{A} + \overline{B}$  in positive logic.

The AUP family of devices has quiescent power consumption less than 1  $\mu$ A and comes in the ultra small DPW package. The DPW package technology is a major breakthrough in IC packaging. Its tiny 0.64 mm square footprint saves significant board space over other package options while still retaining the traditional manufacturing friendly lead pitch of 0.5 mm.

### 8.2 Functional Block Diagram



### 8.3 Feature Description

- Wide operating  $V_{CC}$  range of 0.8 V to 3.6 V
- 3.6-V I/O tolerant to support down translation
- Input hysteresis allows slow input transition and better switching noise immunity at the input
- $I_{off}$  feature allows voltages on the inputs and outputs when  $V_{CC}$  is 0 V
- Low noise due to slower edge rates

### 8.4 Device Functional Modes

**Table 8-1. Function Table**

INPUTS		OUTPUT Y
A	B	
L	L	L
L	H	H
H	L	H
H	H	H

## 9 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The AUP family is TI's premier solution to the industry's low-power needs in battery-powered portable applications. This family ensures a very low static and dynamic power consumption across the entire VCC range of 0.8 V to 3.6 V, resulting in an increased battery life. This product also maintains excellent signal integrity. It has a small amount of hysteresis built in allowing for slower or noisy input signals. The lowered drive produces slower edges and prevents overshoot and undershoot on the outputs.

The AUP family of single gate logic makes excellent translators for the new lower voltage Micro- processors that typically are powered from 0.8 V to 1.2 V. They can drop the voltage of peripheral drivers and accessories that are still powered by 3.3 V to the new uC power levels.

### 9.2 Typical Application

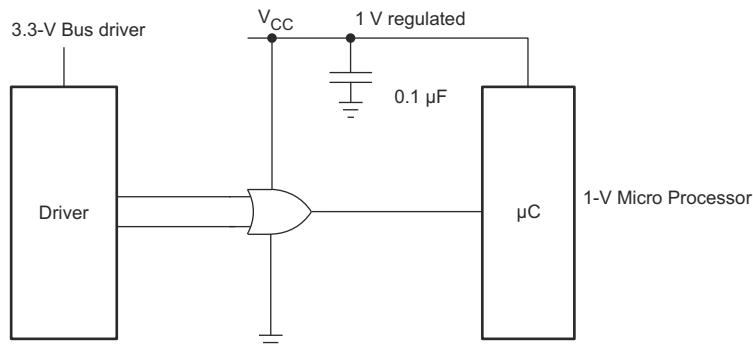


Figure 9-1. Typical Application Schematic

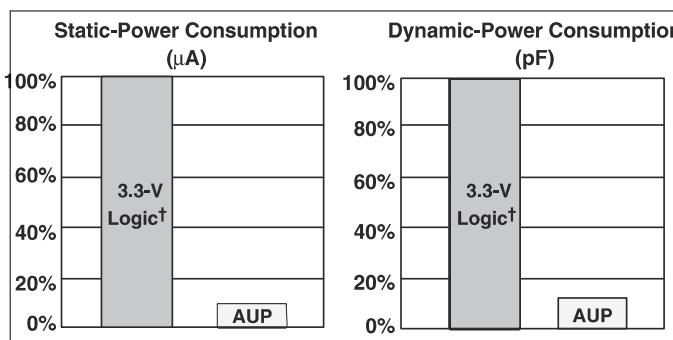
#### 9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits.

#### 9.2.2 Detailed Design Procedure

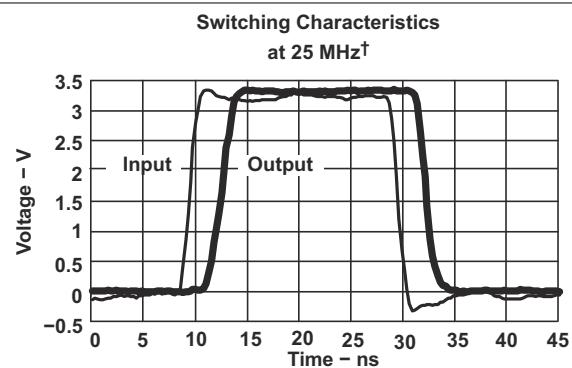
1. Recommended Input conditions
  - Rise time and fall time specifications. See  $(\Delta t/\Delta V)$  in [Recommended Operating Conditions](#) table.
  - Specified high and low levels. See  $(V_{IH}$  and  $V_{IL}$ ) in [Recommended Operating Conditions](#) table.
  - Inputs are overvoltage tolerant allowing them to go as high as 3.6 V at any valid  $V_{CC}$
2. Recommend output conditions
  - Load currents should not exceed 20 mA on the output and 50 mA total for the part
  - Outputs should not be pulled above  $V_{CC}$

### 9.2.3 Application Curves



<sup>†</sup> Single, dual, and triple gates.

**Figure 9-2. AUP – The Lowest-Power Family**



<sup>†</sup> AUP1G08 data at  $C_L = 15 \text{ pF}$

**Figure 9-3. Excellent Signal Integrity**

## 10 Power Supply Recommendations

The power supply can be any voltage between the Min and Max supply voltage rating located in the *Recommended Operating Conditions* table.

Each  $V_{CC}$  terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1  $\mu$ F is recommended and if there are multiple  $V_{CC}$  terminals then .01  $\mu$ F or .022  $\mu$ F is recommended for each power terminal. It is ok to parallel multiple bypass caps to reject different frequencies of noise. A 0.1  $\mu$ F and 1  $\mu$ F are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

## 11 Layout

### 11.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or  $V_{CC}$  whichever make more sense or is more convenient. It is generally OK to float outputs unless the part is a transceiver. If the transceiver has an output enable pin it will disable the outputs section of the part when asserted. This will not disable the input section of the I.O's so they also cannot float when disabled.

### 11.2 Layout Example



## 12 Device and Documentation Support

### 12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 12.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 12.3 Trademarks

TI E2E™ is a trademark of Texas Instruments Incorporated.

All other trademarks are the property of their respective owners.

### 12.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 12.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AUP1G32DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	H32R	Samples
SN74AUP1G32DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	H32R	Samples
SN74AUP1G32DCKR	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(HG5, HGF, HGK, HG R)	Samples
SN74AUP1G32DCKT	ACTIVE	SC70	DCK	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(HG5, HGR)	Samples
SN74AUP1G32DPWR	ACTIVE	X2SON	DPW	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	F4	Samples
SN74AUP1G32DRLR	ACTIVE	SOT-5X3	DRL	5	4000	RoHS & Green	NIPDAU   NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	(HG7, HGR)	Samples
SN74AUP1G32DRY2	ACTIVE	SON	DRY	6	5000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HG	Samples
SN74AUP1G32DRYR	ACTIVE	SON	DRY	6	5000	RoHS & Green	NIPDAU   NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	HG	Samples
SN74AUP1G32DSF2	ACTIVE	SON	DSF	6	5000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HG	Samples
SN74AUP1G32DSFR	ACTIVE	SON	DSF	6	5000	RoHS & Green	NIPDAU   NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	HG	Samples
SN74AUP1G32YFPR	ACTIVE	DSBGA	YFP	6	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM		HGN	Samples
SN74AUP1G32YZPR	ACTIVE	DSBGA	YZP	5	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	HGN	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

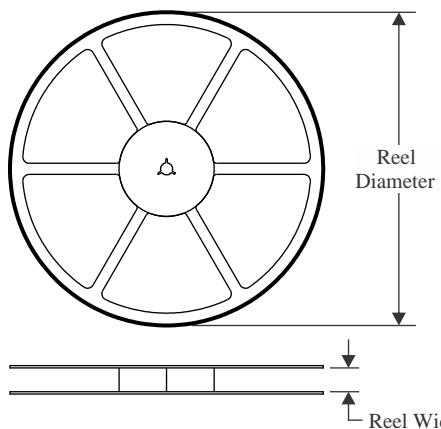
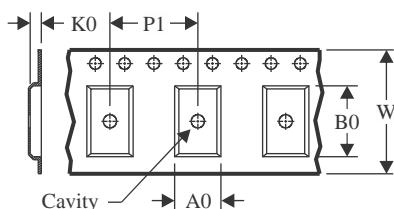
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

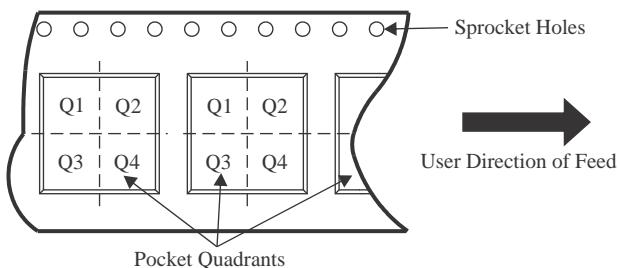
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

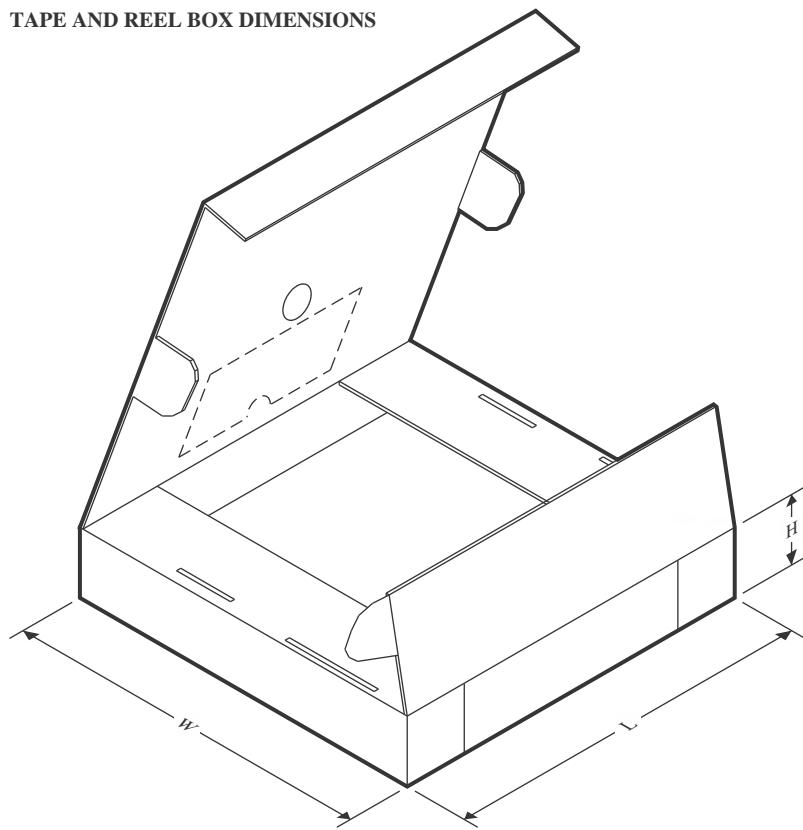
**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUP1G32DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74AUP1G32DBVT	SOT-23	DBV	5	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74AUP1G32DCKR	SC70	DCK	5	3000	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74AUP1G32DCKR	SC70	DCK	5	3000	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3
SN74AUP1G32DCKT	SC70	DCK	5	250	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3
SN74AUP1G32DCKT	SC70	DCK	5	250	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74AUP1G32DPWR	X2SON	DPW	5	3000	178.0	8.4	0.91	0.91	0.5	2.0	8.0	Q3
SN74AUP1G32DRLR	SOT-5X3	DRL	5	4000	180.0	9.5	1.78	1.78	0.69	4.0	8.0	Q3
SN74AUP1G32DRLR	SOT-5X3	DRL	5	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
SN74AUP1G32DRY2	SON	DRY	6	5000	180.0	9.5	1.6	1.15	0.75	4.0	8.0	Q3
SN74AUP1G32DRYR	SON	DRY	6	5000	180.0	9.5	1.15	1.6	0.75	4.0	8.0	Q1
SN74AUP1G32DSF2	SON	DSF	6	5000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q3
SN74AUP1G32DSFR	SON	DSF	6	5000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
SN74AUP1G32YFPR	DSBGA	YFP	6	3000	178.0	9.2	0.89	1.29	0.62	4.0	8.0	Q1
SN74AUP1G32YZPR	DSBGA	YZP	5	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AUP1G32DBVR	SOT-23	DBV	5	3000	202.0	201.0	28.0
SN74AUP1G32DBVT	SOT-23	DBV	5	250	202.0	201.0	28.0
SN74AUP1G32DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
SN74AUP1G32DCKR	SC70	DCK	5	3000	202.0	201.0	28.0
SN74AUP1G32DCKT	SC70	DCK	5	250	202.0	201.0	28.0
SN74AUP1G32DCKT	SC70	DCK	5	250	180.0	180.0	18.0
SN74AUP1G32DPWR	X2SON	DPW	5	3000	205.0	200.0	33.0
SN74AUP1G32DRLR	SOT-5X3	DRL	5	4000	184.0	184.0	19.0
SN74AUP1G32DRLR	SOT-5X3	DRL	5	4000	202.0	201.0	28.0
SN74AUP1G32DRY2	SON	DRY	6	5000	184.0	184.0	19.0
SN74AUP1G32DRYR	SON	DRY	6	5000	184.0	184.0	19.0
SN74AUP1G32DSF2	SON	DSF	6	5000	184.0	184.0	19.0
SN74AUP1G32DSFR	SON	DSF	6	5000	210.0	185.0	35.0
SN74AUP1G32YFPR	DSBGA	YFP	6	3000	220.0	220.0	35.0
SN74AUP1G32YZPR	DSBGA	YZP	5	3000	220.0	220.0	35.0

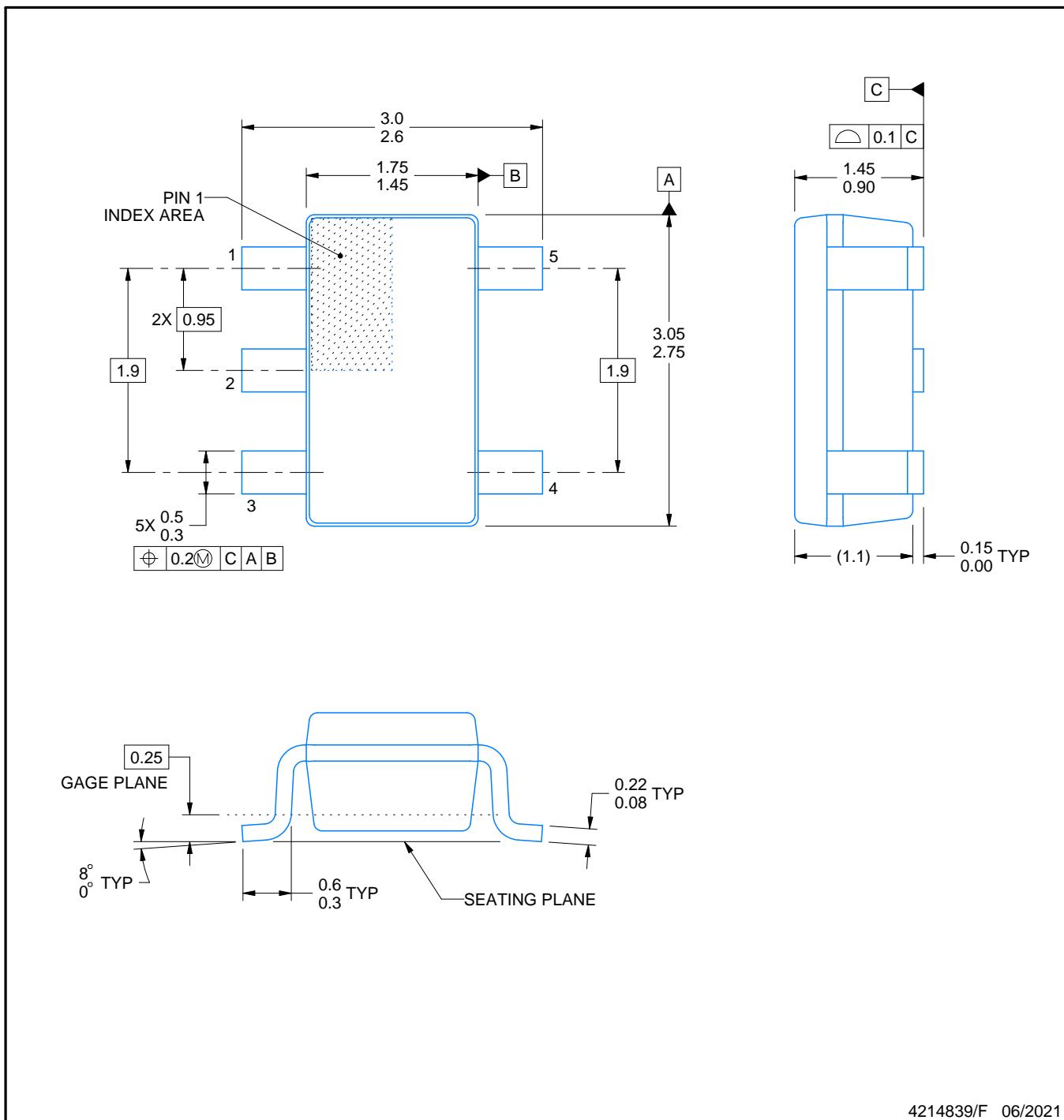
# PACKAGE OUTLINE

DBV0005A



SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



## NOTES:

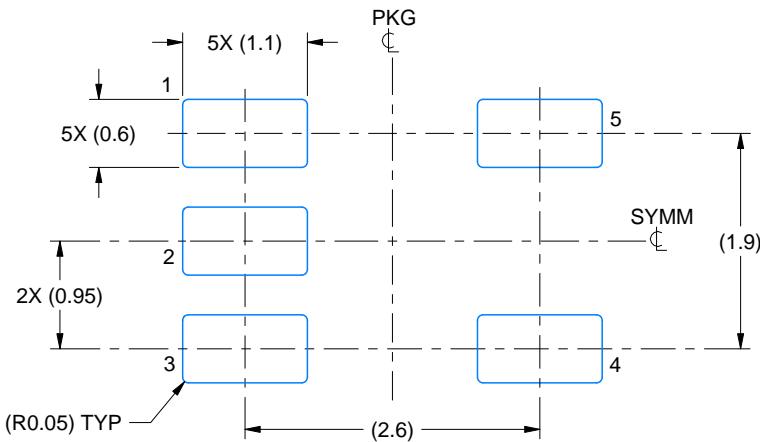
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.

# EXAMPLE BOARD LAYOUT

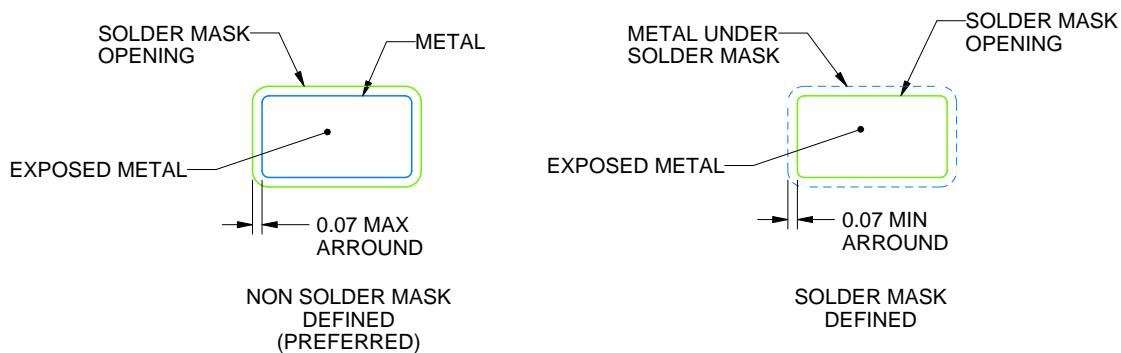
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

4214839/F 06/2021

NOTES: (continued)

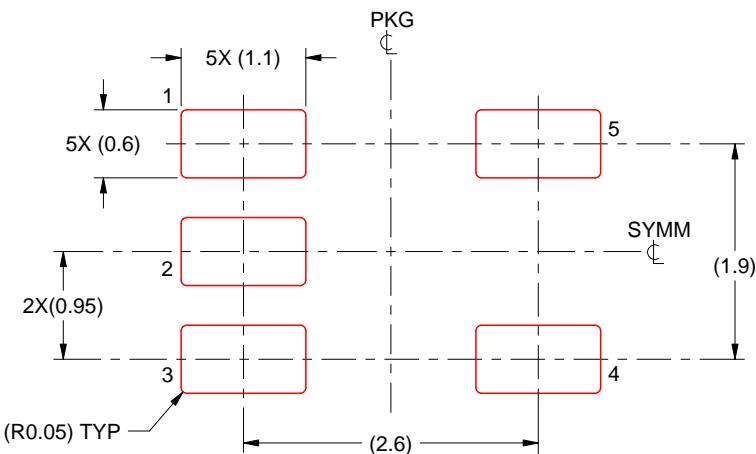
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

4214839/F 06/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

## GENERIC PACKAGE VIEW

DPW 5

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4211218-3/D

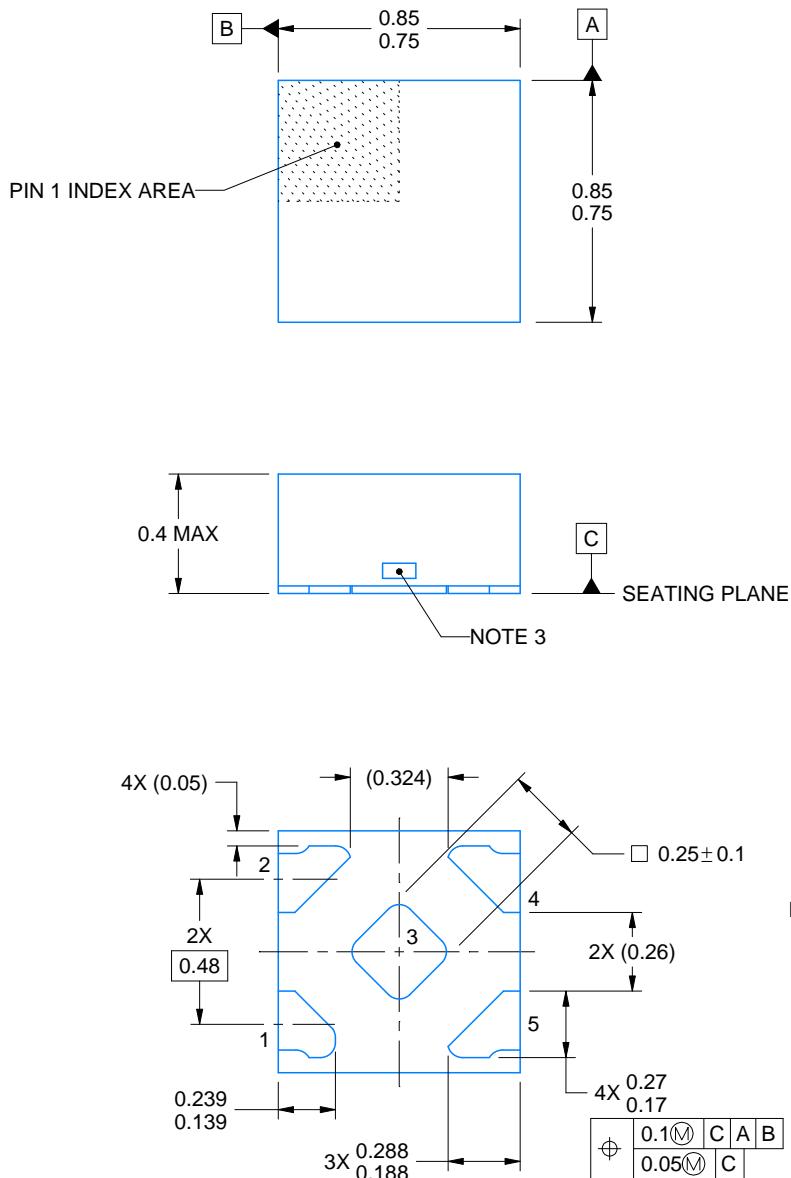
## PACKAGE OUTLINE

**DPW0005A**



## X2SON - 0.4 mm max height

## PLASTIC SMALL OUTLINE - NO LEAD



4223102/D 03/2022

## NOTES:

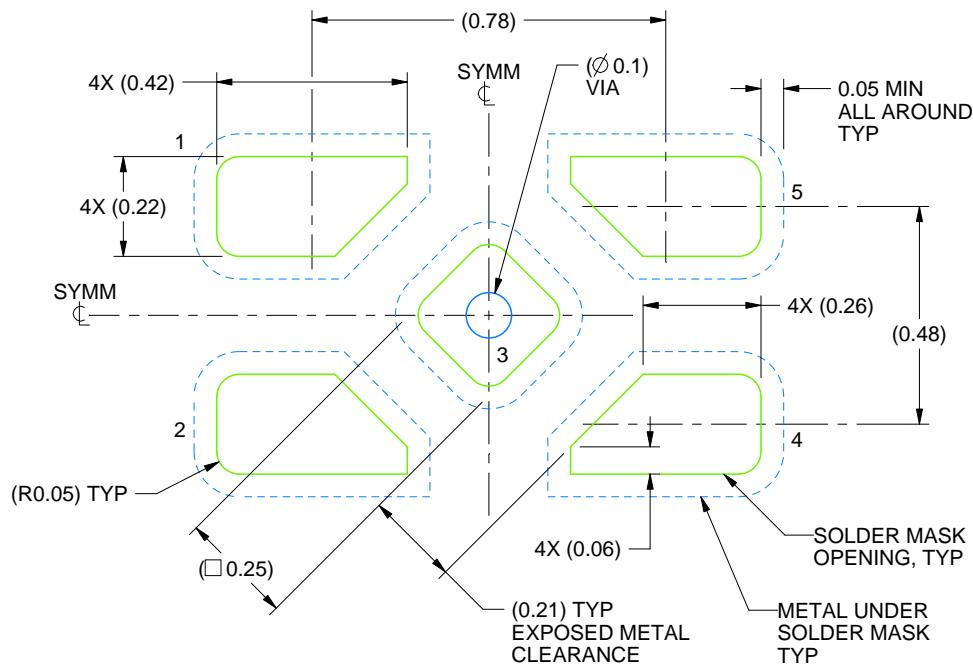
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The size and shape of this feature may vary.

# EXAMPLE BOARD LAYOUT

DPW0005A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE  
SOLDER MASK DEFINED  
SCALE:60X

4223102/D 03/2022

NOTES: (continued)

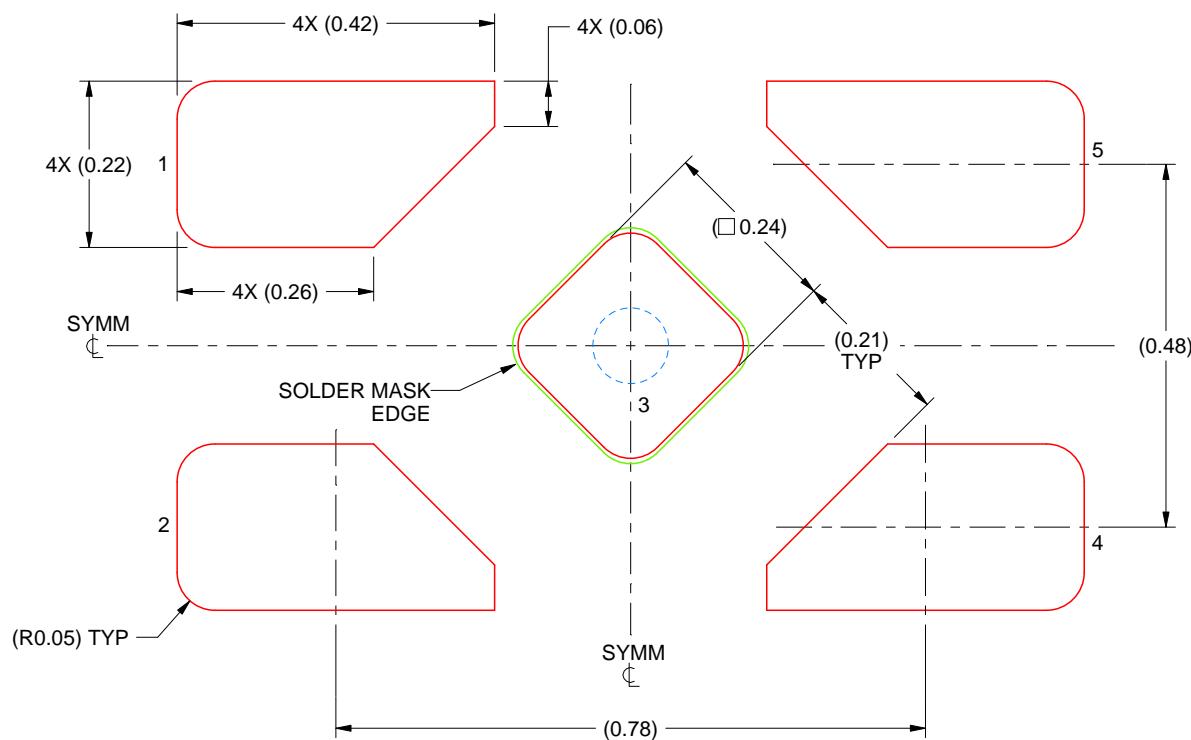
4. This package is designed to be soldered to a thermal pad on the board. For more information, refer to QFN/SON PCB application note in literature No. SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).

## EXAMPLE STENCIL DESIGN

**DPW0005A**

## **X2SON - 0.4 mm max height**

## PLASTIC SMALL OUTLINE - NO LEAD



## SOLDER PASTE EXAMPLE BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 3  
92% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:100X

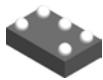
4223102/D 03/2022

#### NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

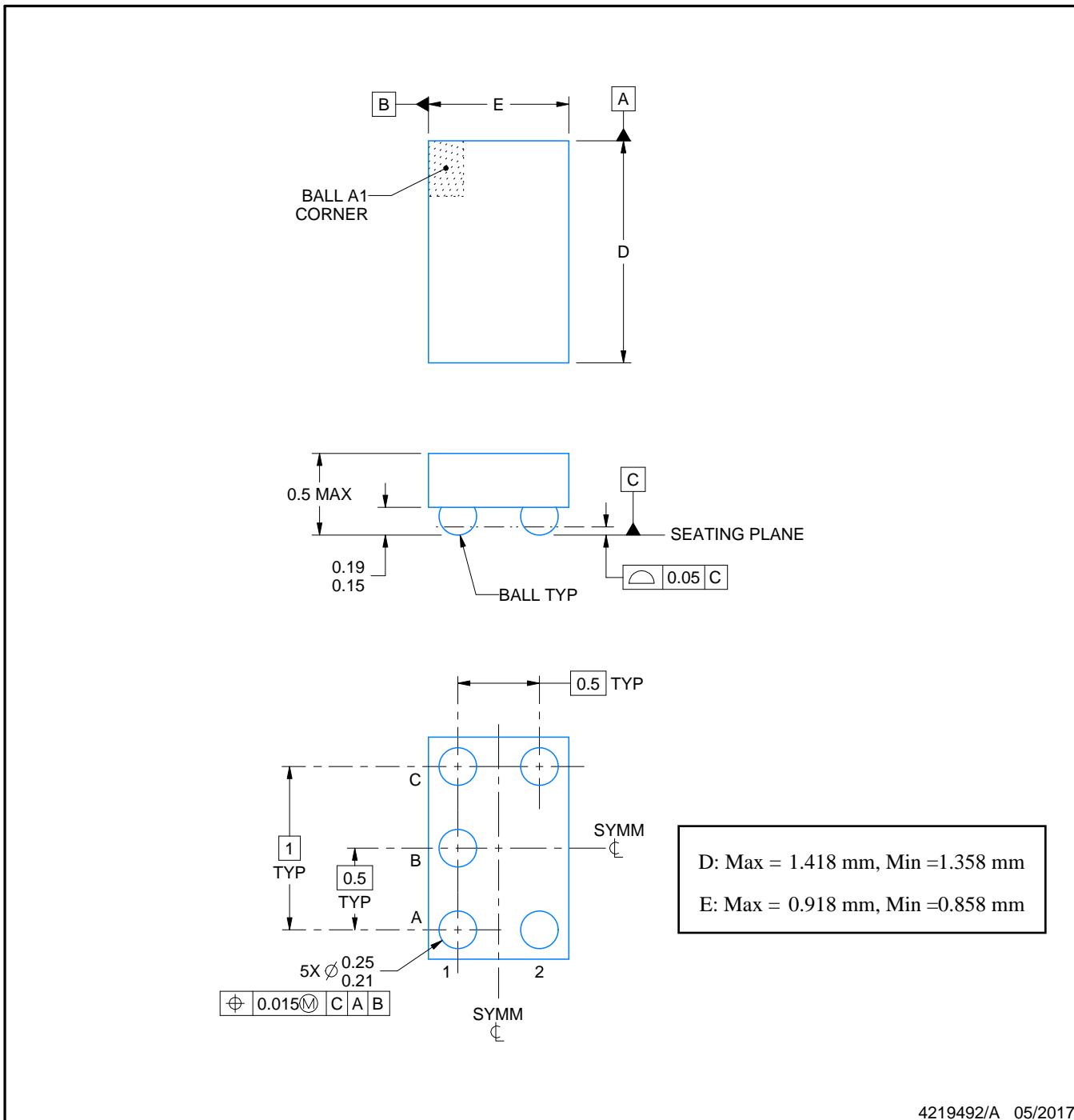
# PACKAGE OUTLINE

YZP0005



DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



4219492/A 05/2017

## NOTES:

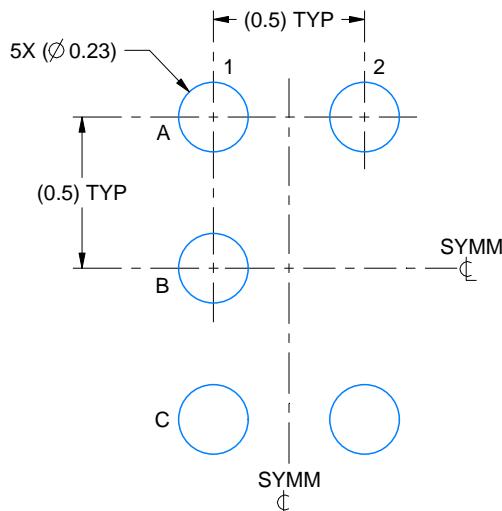
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

# EXAMPLE BOARD LAYOUT

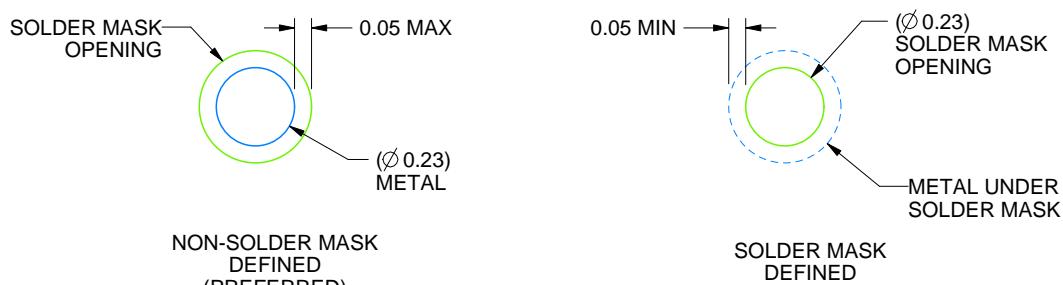
YZP0005

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE  
SCALE:40X



SOLDER MASK DETAILS  
NOT TO SCALE

4219492/A 05/2017

NOTES: (continued)

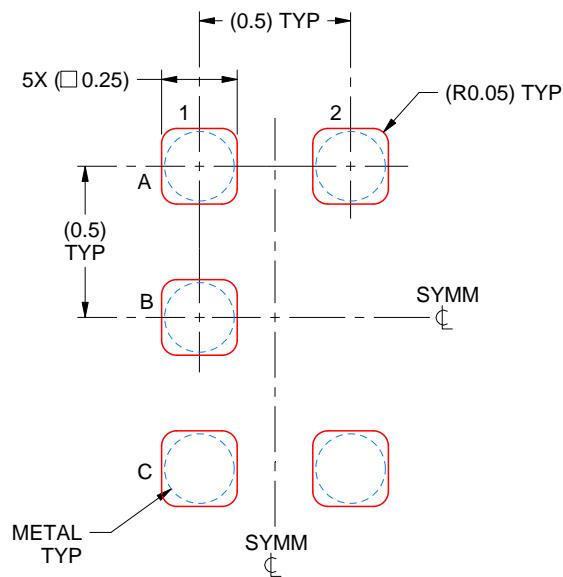
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 ([www.ti.com/lit/snva009](http://www.ti.com/lit/snva009)).

# EXAMPLE STENCIL DESIGN

YZP0005

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE  
BASED ON 0.1 mm THICK STENCIL  
SCALE:40X

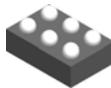
4219492/A 05/2017

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

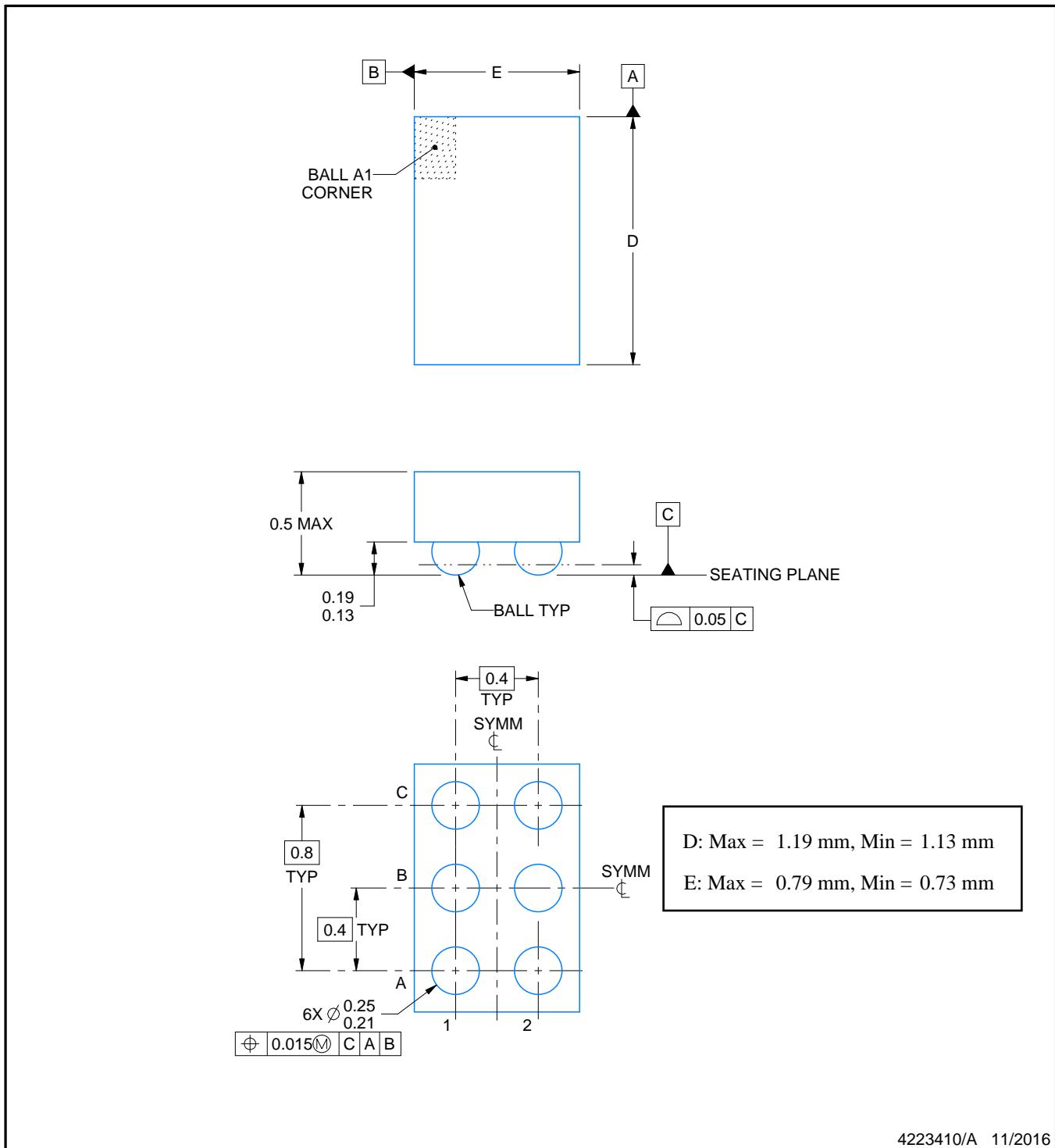
# PACKAGE OUTLINE

**YFP0006**



**DSBGA - 0.5 mm max height**

DIE SIZE BALL GRID ARRAY



4223410/A 11/2016

**NOTES:**

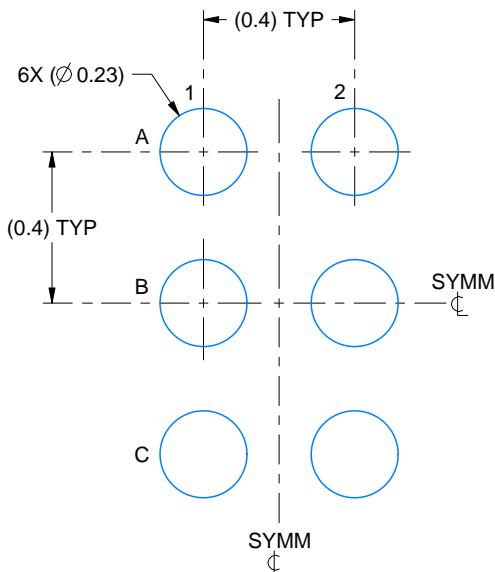
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

# EXAMPLE BOARD LAYOUT

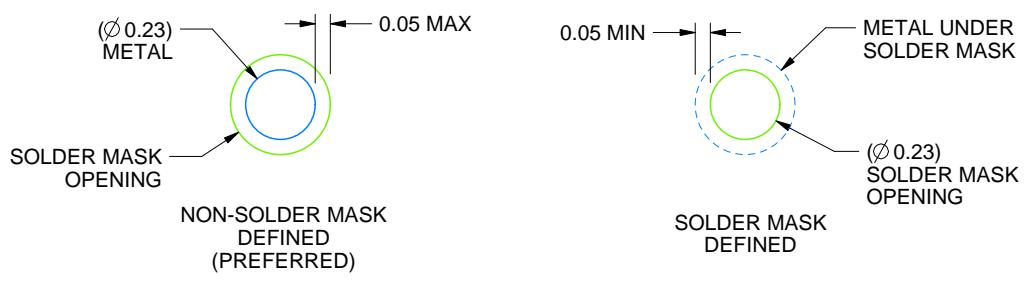
YFP0006

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE  
SCALE:50X



SOLDER MASK DETAILS  
NOT TO SCALE

4223410/A 11/2016

NOTES: (continued)

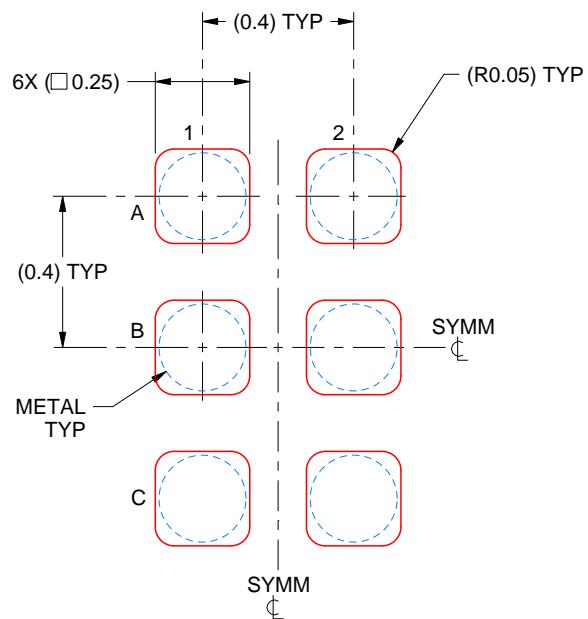
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.  
For more information, see Texas Instruments literature number SNVA009 ([www.ti.com/lit/snva009](http://www.ti.com/lit/snva009)).

# EXAMPLE STENCIL DESIGN

YFP0006

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE  
BASED ON 0.1 mm THICK STENCIL  
SCALE:50X

4223410/A 11/2016

NOTES: (continued)

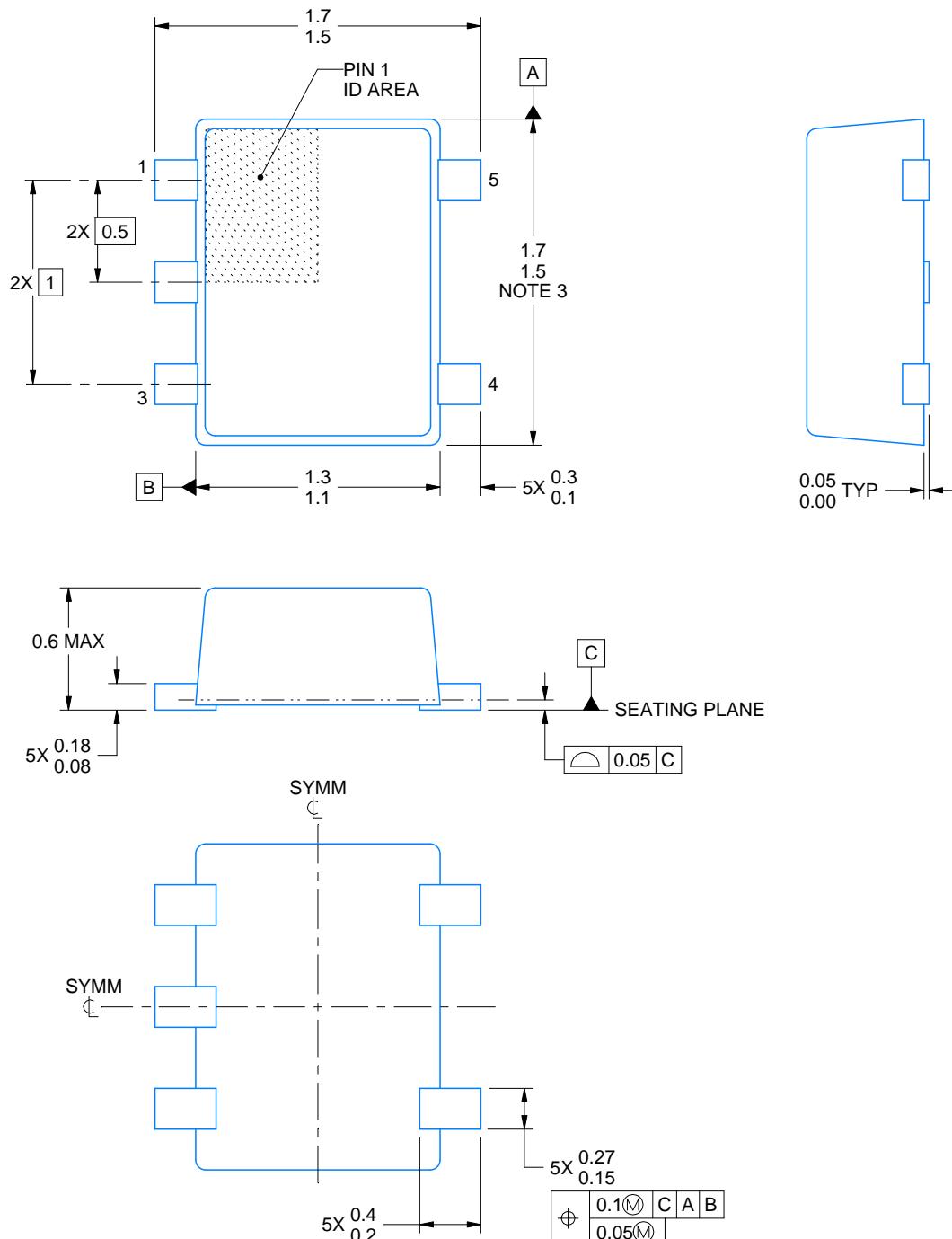
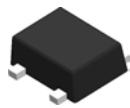
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

# PACKAGE OUTLINE

## SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE

DRL0005A



4220753/B 12/2020

### NOTES:

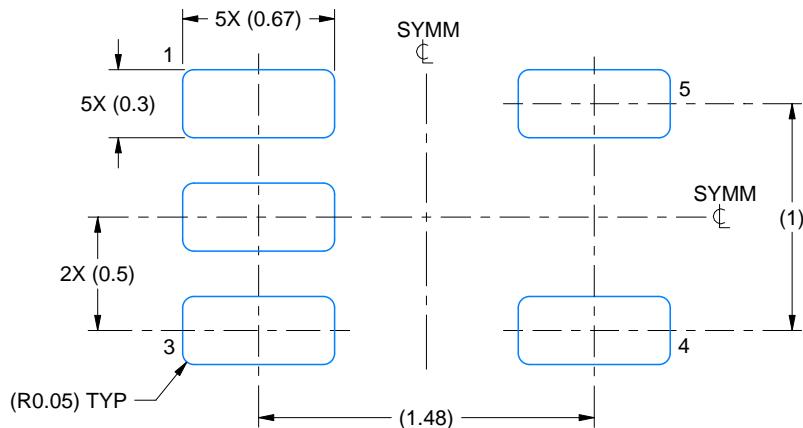
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD-1

# EXAMPLE BOARD LAYOUT

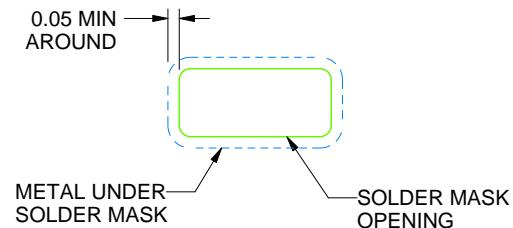
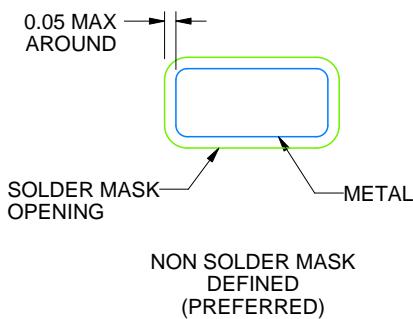
DRL0005A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE  
SCALE:30X



SOLDERMASK DETAILS

4220753/B 12/2020

NOTES: (continued)

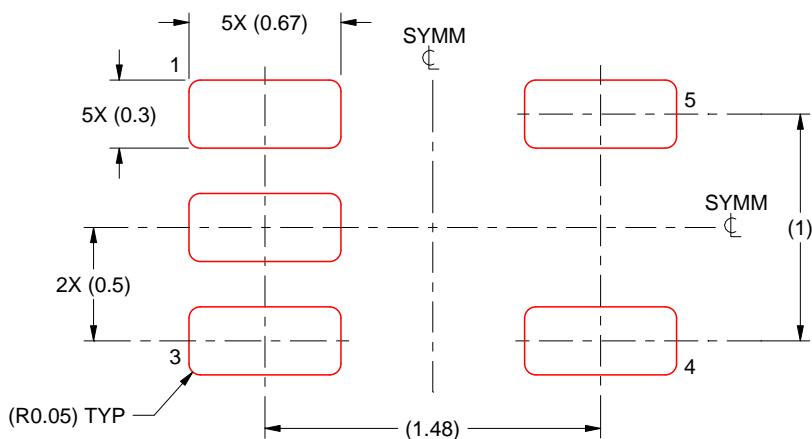
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DRL0005A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE  
BASED ON 0.1 mm THICK STENCIL  
SCALE:30X

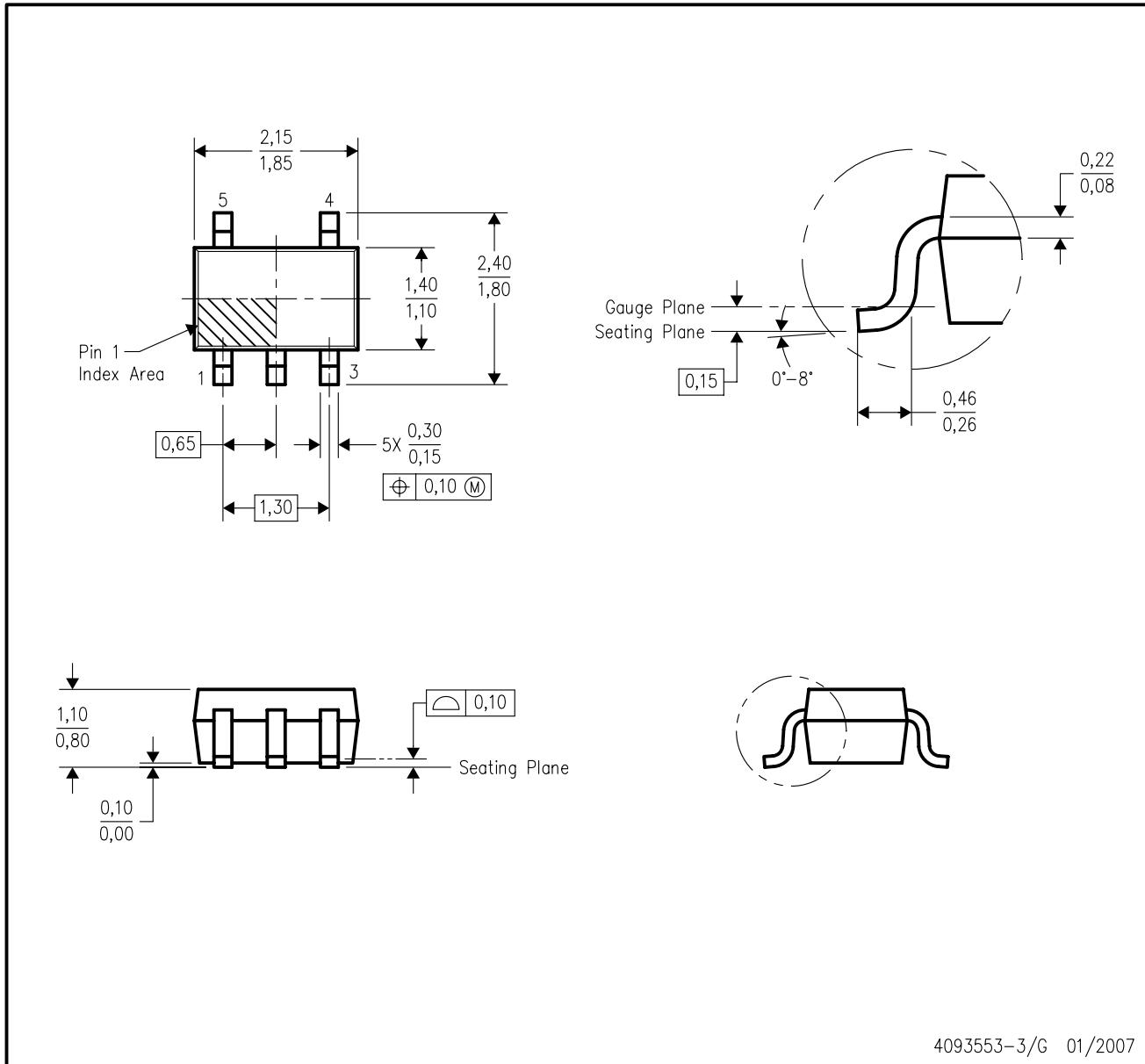
4220753/B 12/2020

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

## DCK (R-PDSO-G5)

## PLASTIC SMALL-OUTLINE PACKAGE



4093553-3/G 01/2007

NOTES:

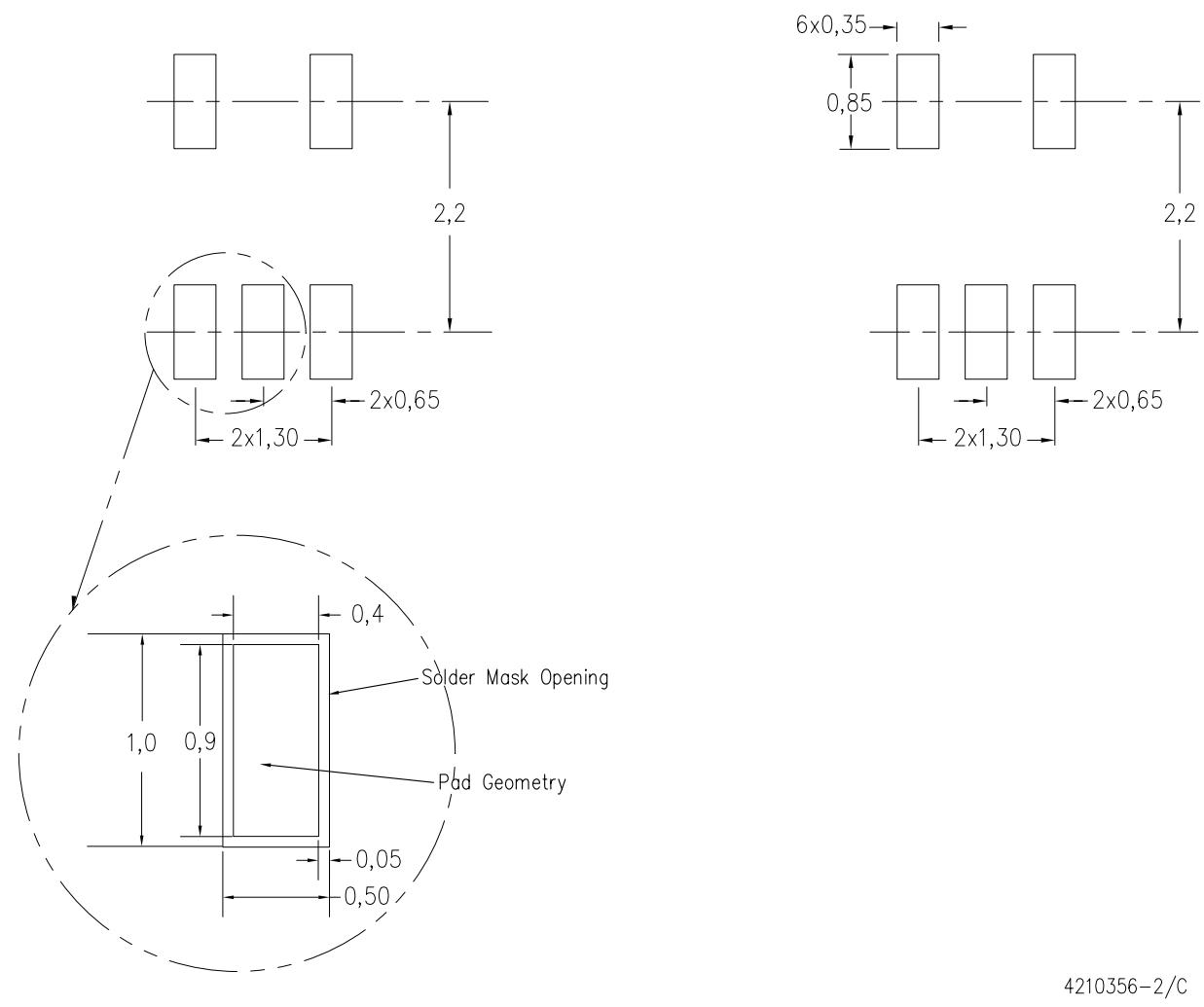
- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- Falls within JEDEC MO-203 variation AA.

DCK (R-PDSO-G5)

PLASTIC SMALL OUTLINE

Example Board Layout

Stencil Openings  
Based on a stencil thickness  
of .127mm (.005inch).



NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- Publication IPC-7351 is recommended for alternate designs.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

DRY 6

## GENERIC PACKAGE VIEW

### USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4207181/G

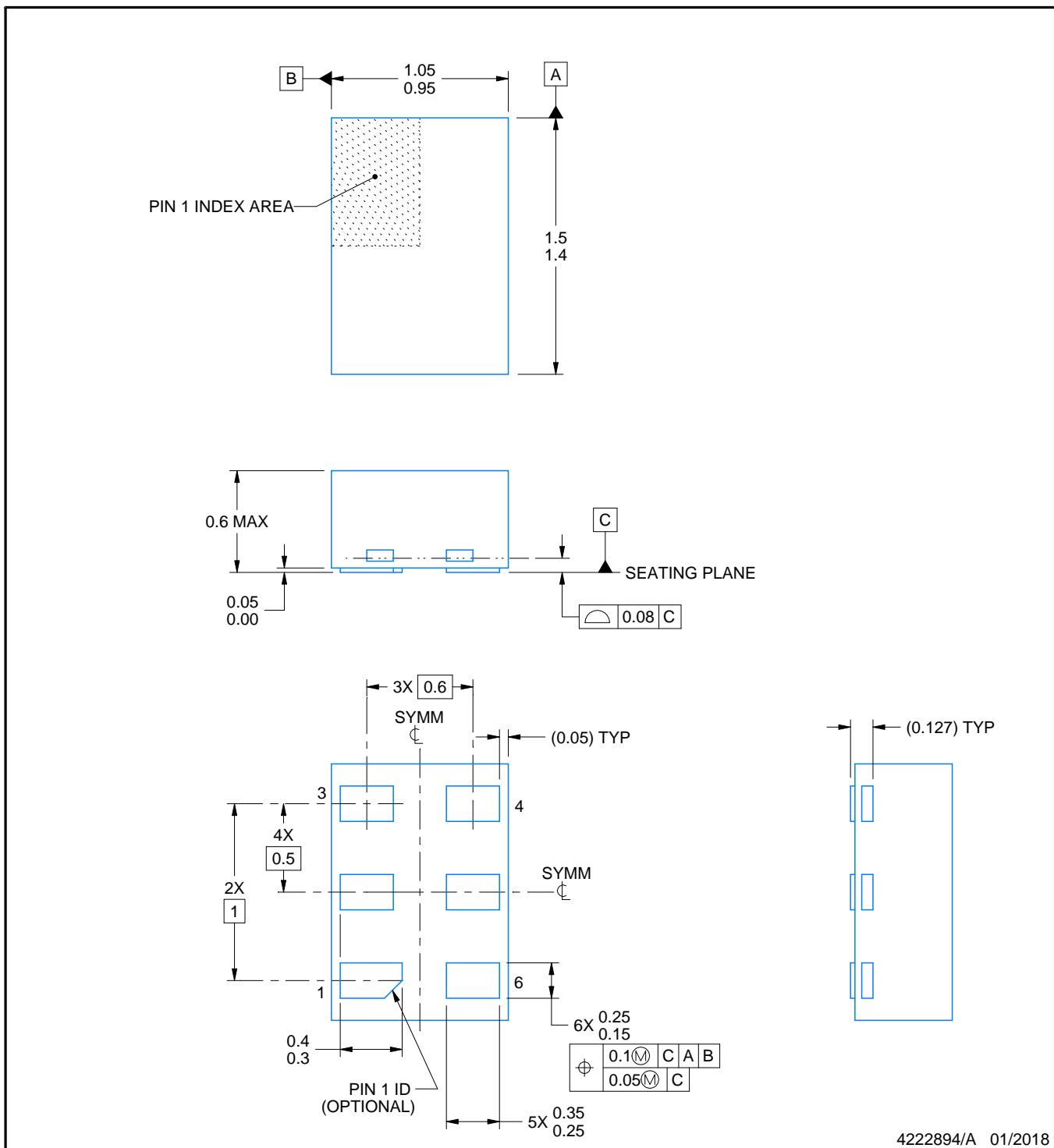
# PACKAGE OUTLINE

DRY0006A



USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



## NOTES:

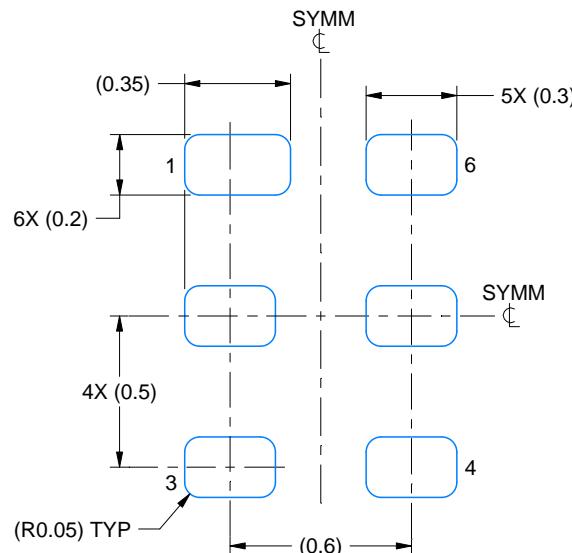
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

# EXAMPLE BOARD LAYOUT

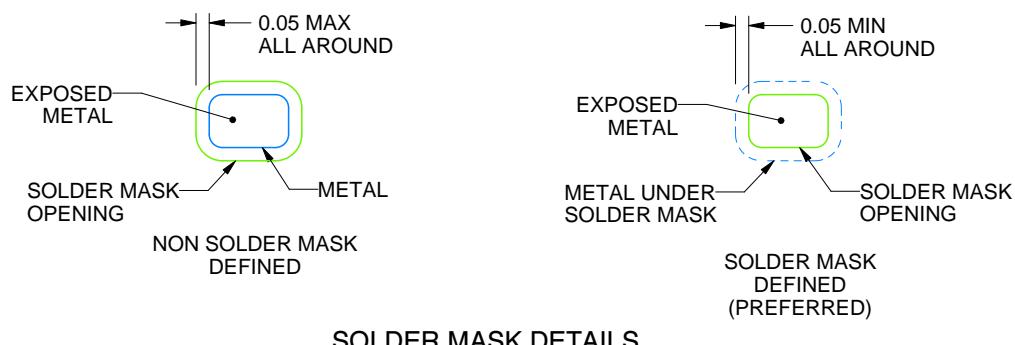
DRY0006A

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE  
1:1 RATIO WITH PKG SOLDER PADS  
EXPOSED METAL SHOWN  
SCALE:40X



SOLDER MASK DETAILS

4222894/A 01/2018

NOTES: (continued)

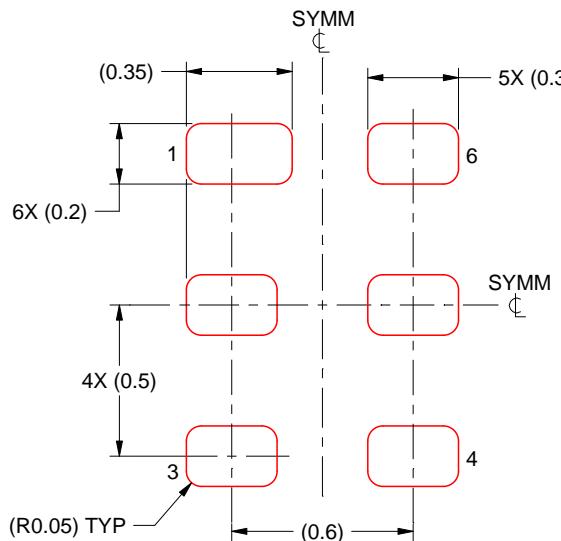
3. For more information, see QFN/SON PCB application report in literature No. SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).

# EXAMPLE STENCIL DESIGN

DRY0006A

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.075 - 0.1 mm THICK STENCIL  
SCALE:40X

4222894/A 01/2018

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

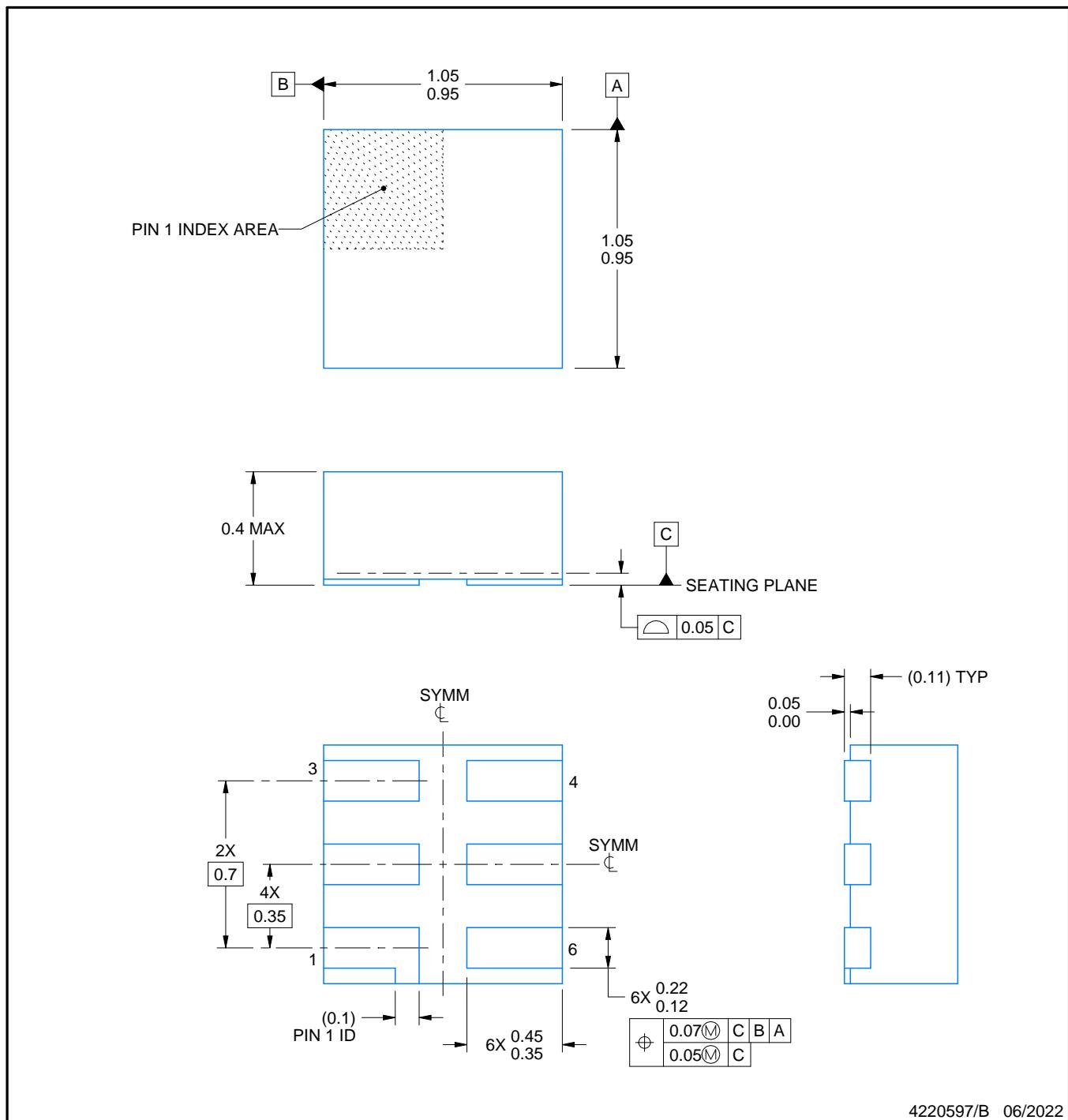


## PACKAGE OUTLINE

**DSF0006A**

## X2SON - 0.4 mm max height

## PLASTIC SMALL OUTLINE - NO LEAD



4220597/B 06/2022

## NOTES:

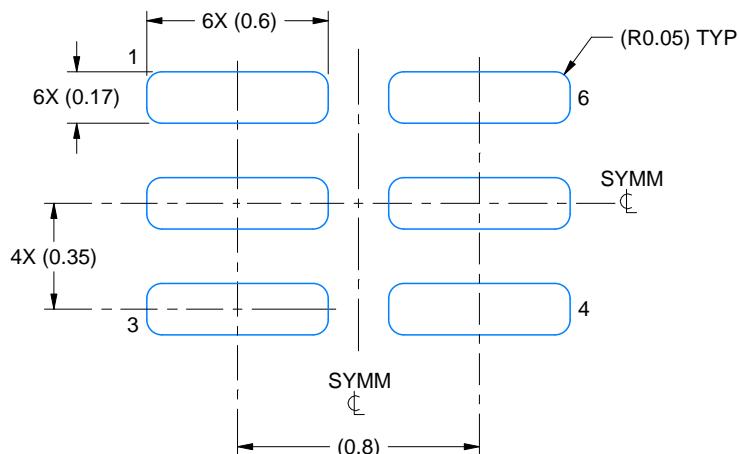
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MO-287, variation X2AAF.

# EXAMPLE BOARD LAYOUT

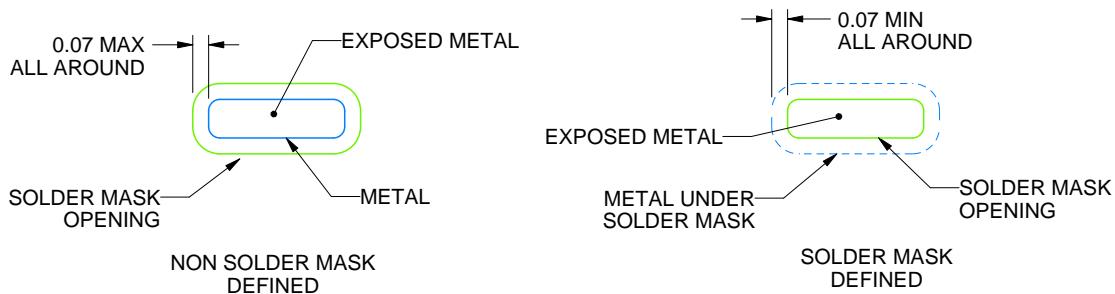
DSF0006A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:40X



SOLDER MASK DETAILS

4220597/B 06/2022

NOTES: (continued)

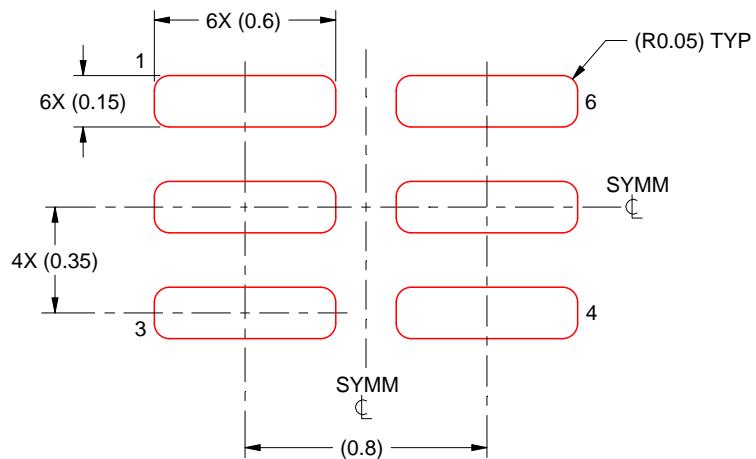
4. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).

# EXAMPLE STENCIL DESIGN

DSF0006A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.09 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:40X

4220597/B 06/2022

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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