

NCP456R

2 A Single Load Switch for Low Voltage Rail

The NCP456R is a power load switch with very low Ron NMOSFET controlled by external logic pin, allowing optimization of battery life, and portable device autonomy.

Indeed, thanks to a best in class current consumption optimization with NMOS structure, leakage currents are drastically decreased. Offering optimized leakages isolation on the ICs connected on the battery.

Reverse voltage protection, from OUT to IN is offered in the NCP456R.

Proposed in wide input voltage range from 0.75 V to 5.5 V, and a very small CSP6 0.85 x 1.25 mm².

Features

- 0.75 V – 5.5 V Operating Range
- 24 mΩ N MOSFET
- Vbias Rail Input
- DC Current up to 2 A
- Reverse Blocking Option
- Active High EN Pin
- CSP6, 0.85 x 1.25 mm², Pitch 0.4 mm
- These Devices are Pb-Free and are RoHS Compliant

Typical Applications

- Notebooks
- Tablets
- Wireless
- Mobile Phones
- Digital Cameras



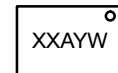
ON Semiconductor®

<http://onsemi.com>



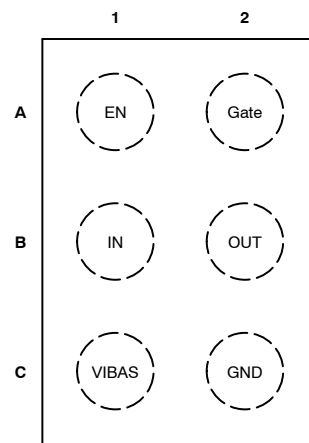
**WLCSP6, 1.25x0.85
CASE 567GZ**

**MARKING
DIAGRAM**



A = Assembly Location
Y = Year
W = Work Week

PIN CONNECTIONS



Top View

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 11 of this data sheet.

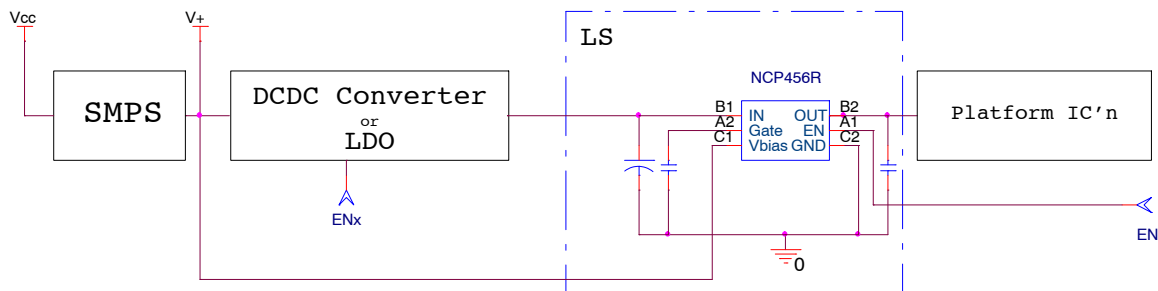


Figure 1. Typical Application Schematic

NCP456R

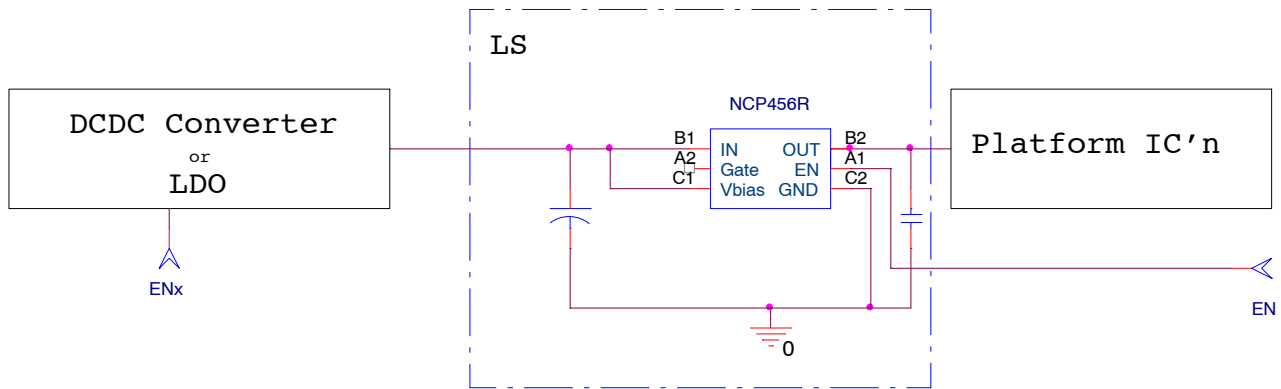


Figure 2. Application Schematic with Vbias Connected to IN and No Gate Delay

PIN FUNCTION DESCRIPTION

| Pin Name | Pin Number | Type | Description |
|----------|------------|-------|--|
| EN | A1 | INPUT | Enable input, logic high turns on power switch . |
| IN | B1 | POWER | Load-switch input pin. |
| VBIAS | C1 | POWER | External supply voltage input. |
| GATE | A2 | INPUT | OUT pin slew rate control (t_{rise}). |
| OUT | B2 | POWER | Load-switch output pin. |
| GND | C2 | POWER | Ground connection. |

NCP456R

BLOCK DIAGRAM

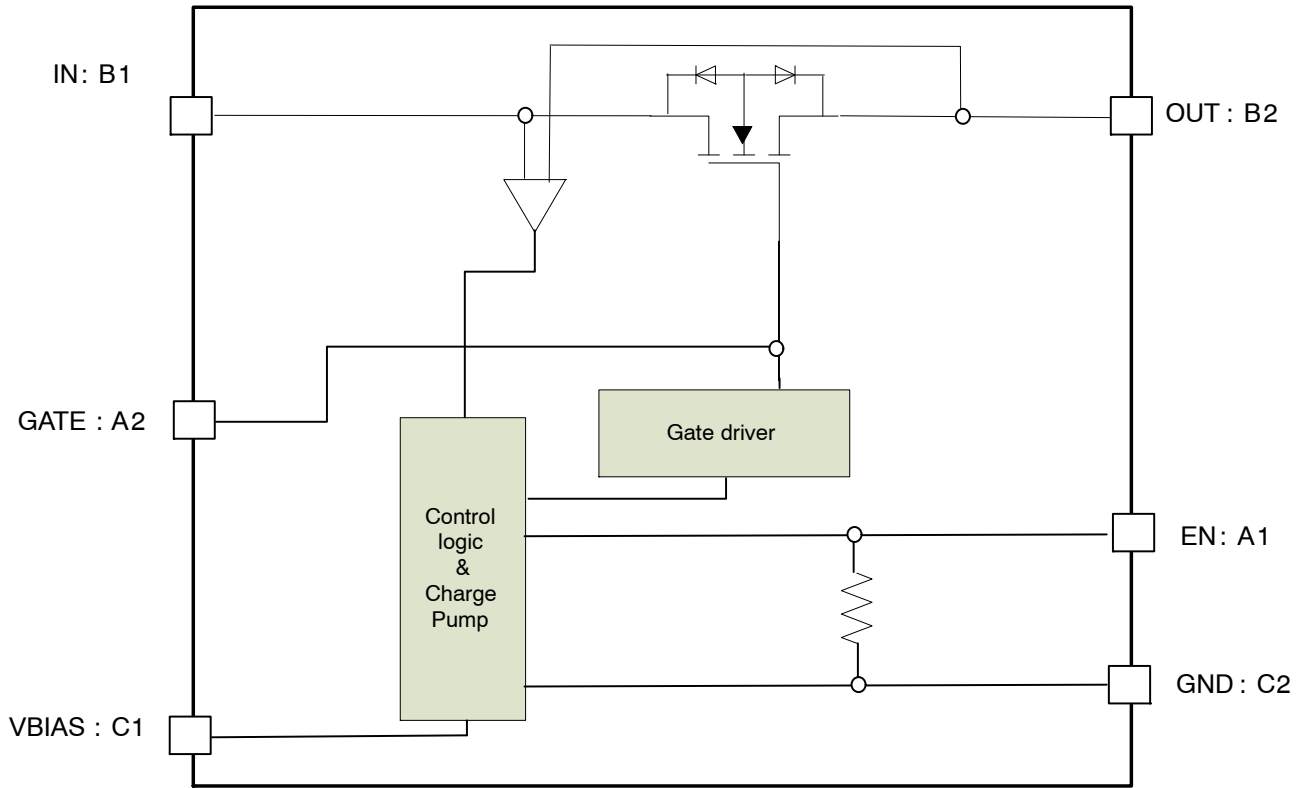


Figure 3. Block Diagram

NCP456R

MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|--|---|---------------|------|
| IN, OUT, EN, VBIAS, GATE Pins: (Note 1) | $V_{EN}, V_{IN}, V_{OUT}, V_{BIAS}, V_{GATE}$ | -0.3 to + 6.5 | V |
| From IN to OUT Pins: Input/Output (Note 1) | V_{IN}, V_{OUT} | ±6.5 | V |
| Human Body Model (HBM) ESD Rating are (Note 2) | ESD HBM | 2000 | V |
| Machine Model (MM) ESD Rating are (Note 2) | ESD MM | 200 | V |
| Latch-up Protection (Note 3) Pins IN, OUT, EN, VBIAS and GATE | LU | 100 | mA |
| Maximum Junction Temperature | T_J | -40 to + 125 | °C |
| Storage Temperature Range | T_{STG} | -40 to + 150 | °C |
| Moisture Sensitivity (Note 4) | MSL | Level 1 | |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- According to JEDEC standard JESD22-A108.
- This device series contains ESD protection and passes the following tests:
Human Body Model (HBM) ±2.0 kV per JEDEC standard: JESD22-A114 for all pins.
Machine Model (MM) ±250 V per JEDEC standard: JESD22-A115 for all pins.
- Latch up Current Maximum Rating: ±100 mA per JEDEC standard: JESD78 class II.
- Moisture Sensitivity Level (MSL): 1 per IPC/JEDEC standard: J-STD-020.

OPERATING CONDITIONS

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------------|--|---------------|------|-----|-----|------|
| V_{IN} | Operational Power Supply | | 0.75 | | 5.5 | V |
| V_{EN} | Enable Voltage | | 0 | | 5.5 | V |
| V_{BIAS} | Bias voltage ($V_{BIAS} \geq \text{best of } V_{IN}, V_{out}$) | | 1.2 | | 5.5 | V |
| T_A | Ambient Temperature Range | | -40 | 25 | +85 | °C |
| C_{IN} | Decoupling input capacitor | | 100 | | | nF |
| C_{OUT} | Decoupling output capacitor | | 100 | | | nF |
| $R_{\theta JA}$ | Thermal Resistance Junction to Air | CSP6 (Note 5) | | 100 | | °C/W |
| I_{OUT} | Maximum DC current | | | | 2 | A |
| P_D | Power Dissipation Rating | (Note 6) | | 0.2 | | W |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

- The $R_{\theta JA}$ is dependent of the PCB heat dissipation and thermal via.
- The maximum power dissipation (P_D) is given by the following formula:

$$P_D = \frac{T_{JMAX} - T_A}{R_{\theta JA}}$$

NCP456R

ELECTRICAL CHARACTERISTICS Min & Max Limits apply for T_A between -40°C to $+85^{\circ}\text{C}$ for V_{IN} and V_{BIAS} between 0.75 V to 5.5 V (Unless otherwise noted). Typical values are referenced to $T_A = +25^{\circ}\text{C}$, $V_{IN} = 3.3\text{ V}$ and $V_{BIAS} = 5\text{ V}$ (Unless otherwise noted).

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit | |
|---------------------|---|--|-----------------------------|-----|-----|------|------------------|
| POWER SWITCH | | | | | | | |
| $R_{DS(on)}$ | Static drain-source on-state resistance for each rail | $V_{IN} = V_{BIAS} = 5.5\text{ V}$ | $T_A = 25^{\circ}\text{C}$ | | 24 | 33 | $\text{m}\Omega$ |
| | | | $T_J = 125^{\circ}\text{C}$ | | | 39 | |
| | | $V_{IN} = V_{BIAS} = 3.3\text{ V}$ | $T_A = 25^{\circ}\text{C}$ | | 24 | 33 | |
| | | | $T_J = 125^{\circ}\text{C}$ | | | 39 | |
| | | $V_{IN} = V_{BIAS} = 1.8\text{ V}$ | $T_A = 25^{\circ}\text{C}$ | | 25 | 34 | |
| | | | $T_J = 125^{\circ}\text{C}$ | | | 40 | |
| | | $V_{IN} = V_{BIAS} = 1.5\text{ V}$ | $T_A = 25^{\circ}\text{C}$ | | 26 | 35 | |
| | | | $T_J = 125^{\circ}\text{C}$ | | | 41 | |
| | | $V_{IN} = V_{BIAS} = 1.2\text{ V}$ | $T_A = 25^{\circ}\text{C}$ | | 28 | 40 | |
| | | | $T_J = 125^{\circ}\text{C}$ | | | 42 | |
| | | $V_{IN} = 1.0\text{ V}$, $V_{BIAS} = 1.2\text{ V}$ | $T_A = 25^{\circ}\text{C}$ | | 30 | 40 | |
| | | | $T_J = 125^{\circ}\text{C}$ | | | 42 | |
| | | $V_{IN} = 0.8\text{ V}$, $V_{BIAS} = 1.2\text{ V}$ | $T_A = 25^{\circ}\text{C}$ | | 35 | 45 | |
| | | | $T_J = 125^{\circ}\text{C}$ | | | 50 | |

TIMINGS

| | | | | | | | | |
|----------|------------------|-----------------------|--|--|------|-----|---------------|---------------|
| T_R | Output rise time | $V_{IN} = 5\text{ V}$ | No cap on GATE pin | | 0.11 | | ms | |
| | | | Gate capacitor = 1 nF | | 1.4 | | | |
| | | | Gate capacitor = 10 nF | | 15.7 | | | |
| T_F | Output fall time | | $C_{LOAD} = 1\ \mu\text{F}$, $R_{LOAD} = 25\ \Omega$ (Note 8) | | 50 | | μs | |
| T_{en} | Enable time | | From EN low to high to $V_{out} = 10\%$ of fully on- NCP456R. 10 nF gate capacitor | | 3 | | ms | |
| | | | From EN low to high to $V_{out} = 10\%$ of fully on- NCP456R. 1 nF gate capacitor | | 300 | | μs | |
| | | | From EN low to high to $V_{out} = 10\%$ of fully on- NCP456R. Without gate capacitor | | 51 | | μs | |
| T_R | Output rise time | | $V_{IN} = 3.3\text{ V}$ | No cap on GATE pin | | 0.1 | 0.3 | ms |
| | | | | Gate capacitor = 1 nF | | 1 | | |
| | | | | Gate capacitor = 10 nF | | 11 | | |
| T_F | Output fall time | | | $C_{LOAD} = 1\ \mu\text{F}$, $R_{LOAD} = 25\ \Omega$ (Note 8) | | 60 | 120 | μs |
| T_{en} | Enable time | | | From EN low to high to $V_{out} = 10\%$ of fully on- NCP456R. 10 nF Gate capacitor. | | 2.4 | | ms |
| | | | | From EN low to high to $V_{out} = 10\%$ of fully on- NCP456R. 1 nF Gate capacitor. | | 230 | | μs |
| | | | | From EN low to high to $V_{out} = 10\%$ of fully on- NCP456R. Without gate capacitor | | 50 | 120 | μs |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

7. Parameters are guaranteed for C_{LOAD} and R_{LOAD} connected to the OUT pin with respect to the ground

8. Guaranteed by design and characterization, not production tested.

NCP456R

ELECTRICAL CHARACTERISTICS Min & Max Limits apply for T_A between -40°C to $+85^{\circ}\text{C}$ for V_{IN} and V_{BIAS} between 0.75 V to 5.5 V (Unless otherwise noted). Typical values are referenced to $T_A = +25^{\circ}\text{C}$, $V_{IN} = 3.3\text{ V}$ and $V_{BIAS} = 5\text{ V}$ (Unless otherwise noted).

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------|-----------|------------|-----|-----|-----|------|
|--------|-----------|------------|-----|-----|-----|------|

TIMINGS

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------|------------------|--|-----|------|-----|---------------|
| T_R | Output rise time | No cap on GATE pin | | 0.06 | | ms |
| | | Gate capacitor = 1 nF | | 0.6 | | |
| | | Gate capacitor = 10 nF | | 6 | | |
| T_F | Output fall time | $C_{LOAD} = 1\ \mu\text{F}$, $R_{LOAD} = 25\ \Omega$ (Note 8) | | 35 | | μs |
| T_{en} | Enable time | $V_{IN} = 1.8\text{ V}$ From EN low to high to $V_{out} = 10\%$ of fully on- 10 nF Gate capacitor | | 1.8 | | ms |
| | | From EN low to high to $V_{out} = 10\%$ of fully on- 1 nF Gate capacitor | | 180 | | μs |
| | | From EN low to high to $V_{out} = 10\%$ of fully on- NCP456R. Without gate capacitor | | 42 | | μs |
| T_R | Output rise time | No cap on GATE pin | | 0.04 | | ms |
| | | Gate capacitor = 1 nF | | 0.35 | | |
| | | Gate capacitor = 10 nF | | 3.5 | | |
| T_F | Output fall time | $C_{LOAD} = 1\ \mu\text{F}$, $R_{LOAD} = 25\ \Omega$ (Note 8) | | 20 | | μs |
| T_{en} | Enable time | $V_{IN} = 1\text{ V}$ From EN low to high to $V_{out} = 10\%$ of fully on- 1 nF gate capacitor | | 140 | | μs |
| | | From EN low to high to $V_{out} = 10\%$ of fully on- NCP456R. Without gate capacitor | | 40 | | μs |

LOGIC

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------|--------------------------|------------|-----|-----|-----|------------------|
| V_{IH} | High-level input voltage | | 0.9 | | | V |
| V_{IL} | Low-level input voltage | | | | 0.4 | V |
| R_{EN} | Pull down resistor | | 3 | | 7 | $\text{M}\Omega$ |

REVERSE CURRENT BLOCKING

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------------|----------------------------------|-----------------------------------|-----|-----|-----|---------------|
| V_{rev_thr} | Reverse threshold | $V_{out} - V_{in}$ | | 32 | | mV |
| V_{rev_hyst} | Reverse threshold hysteresis | | | 50 | | mV |
| T_{rev} | Reverse comparator response time | $V_{out} - V_{in} > V_{rev_thr}$ | | 2.5 | | μs |

QUIESCENT CURRENT

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-------------|------------------------------|---|-----|------|-----|---------------|
| I_{VBIAS} | Bias current for charge pump | $V_{BIAS} = 3.3\text{ V}$, EN = high | | 1.5 | 6 | μA |
| I_{IN} | IN Current consumption | EN = high | | 0.01 | 0.3 | μA |
| I_{STB} | Standby current IN | EN = low, IN standby current, $V_{IN} = 3.3\text{ V}$ | | 0.01 | 0.3 | μA |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

7. Parameters are guaranteed for C_{LOAD} and R_{LOAD} connected to the OUT pin with respect to the ground

8. Guaranteed by design and characterization, not production tested.

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ELECTRICAL CHARACTERISTICS Min & Max Limits apply for T_A between -40°C to $+85^{\circ}\text{C}$ for V_{IN} and V_{BIAS} between 0.75 V to 5.5 V (Unless otherwise noted). Typical values are referenced to $T_A = +25^{\circ}\text{C}$, $V_{IN} = 3.3\text{ V}$ and $V_{BIAS} = 5\text{ V}$ (Unless otherwise noted).

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------------------|----------------------------|---|-----|------|-----|---------------|
| QUIESCENT CURRENT | | | | | | |
| $I_{STDV_{bias}}$ | Standby current V_{BIAS} | $V_{BIAS} = 3.3\text{ V}$ EN = low | | 0.4 | 2 | μA |
| I_{out_leak} | Output leakage current | IN connected to GND, $V_{OUT} = 5\text{ V}$ | | 0.01 | 0.5 | μA |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

7. Parameters are guaranteed for C_{LOAD} and R_{LOAD} connected to the OUT pin with respect to the ground
8. Guaranteed by design and characterization, not production tested.

TIMINGS

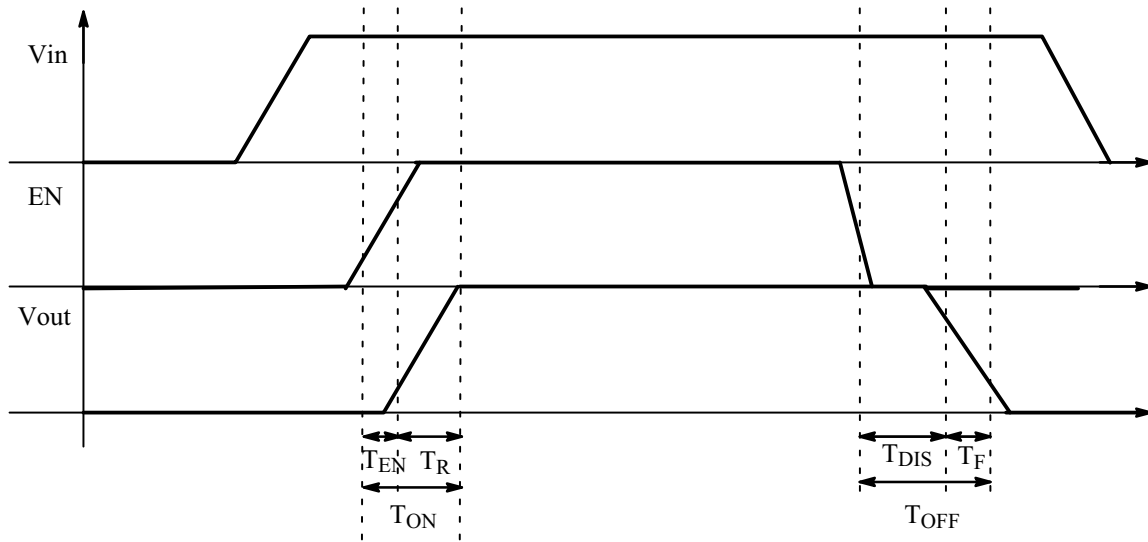


Figure 4. Enable, Rise and Fall Time

NCP456R

TYPICAL CHARACTERISTICS

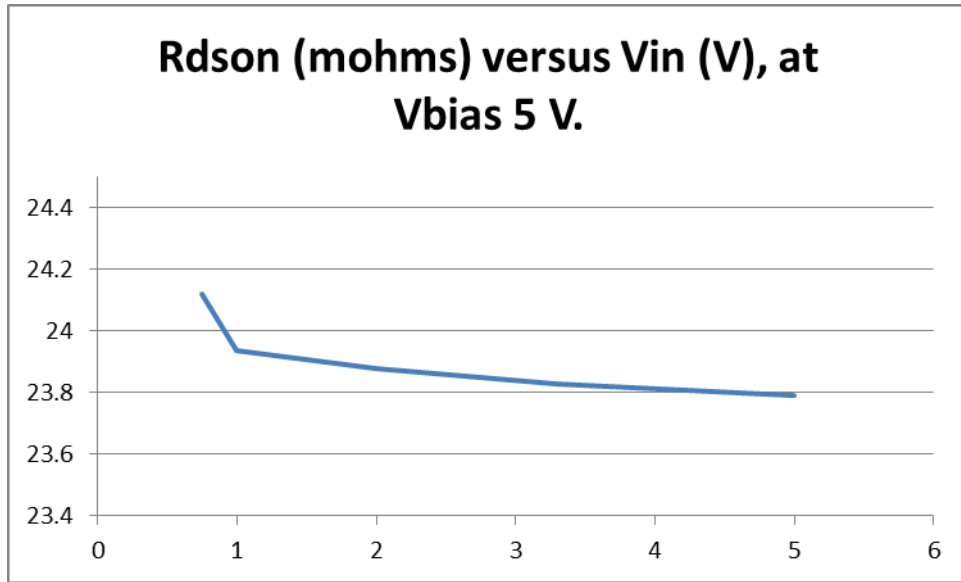


Figure 5. $R_{DS(on)}$ versus V_{in} , Room Temperature, Vbias 5 V

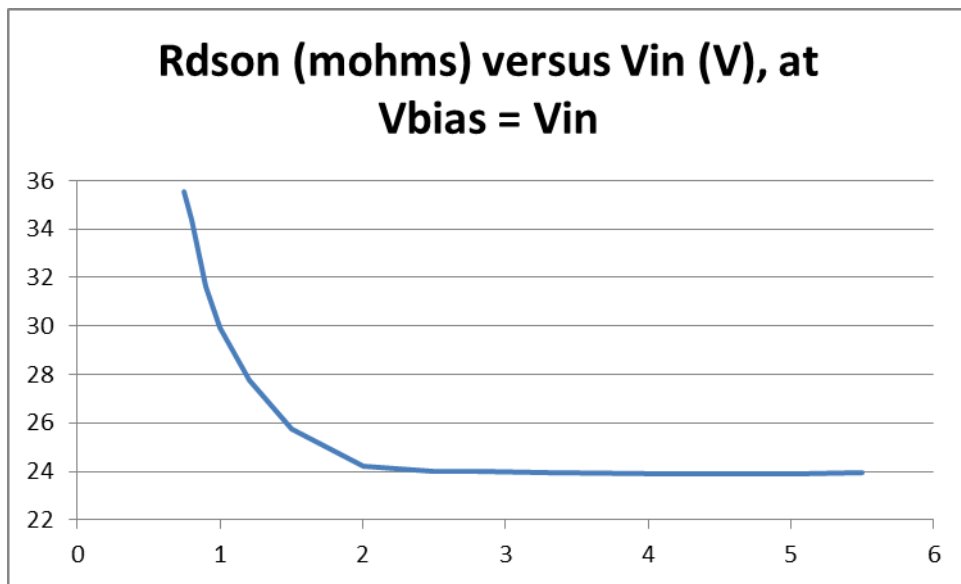


Figure 6. $R_{DS(on)}$ versus V_{in} , Room Temperature, Vbias Connected to V_{in}

FUNCTIONAL DESCRIPTION

Overview

The NCP456R is a high side N Channel MOSFET power distribution switch designed to isolate ICs connected on the battery or DCDC supplies in order to save energy. The part can be used with a wide range of supply from 0.75 V to 5.5 V.

Enable input

Enable pin is an active high. The path is opened when EN pin is tied low (disable), forcing NMOS switch off.

The IN/OUT path is activated with a minimum of $V_{BIAS} \geq \max(V_{IN}, V_{OUT}) = 0.75\text{ V}$ and EN forced to high level.

V_{BIAS} Rail

The core of the IC is supplied due to V_{BIAS} supply rail (common +5 V, 3.3 V, 1.8 V, 1.2 V ...etc). Indeed, no current consumption is used on IN pin, allowing to improve power saving of the rail that must be isolated by the power switch.

If Vbias rail is not available or used, Vbias pin and Vin pin can be connected together as close as possible the DUT.

Output Rise Time – Gate Control

The NMOS is control with internal charge pump and driver. A minimum gate slew rate is internally set to avoid

huge inrush current when EN is set from low to high. The default gate slew rate depends on Vin level. The higher Vin level, the longer rise time.

In addition, an external capacitor can be connected between Gate pin and GND in order to slow down the gate rising. See electrical table for more details.

Cin and Cout Capacitors

100 nF external capacitors must be connected as close as possible the DUT for noise immunity and better stability. In case of input hot plug (input voltage connected with fast slew rate – few μs – it's strongly recommended to avoid big capacitor connected on the input. That allows to avoid input over voltage transients.

Reverse Blocking Control

A reverse blocking control circuitry is embedded to eliminate leakages from OUT to IN in case of $V_{out} > V_{in}$.

A comparator measures the dropout voltage on the switch between OUT and IN and turn off the NMOS if this voltage exceeds specified reverse voltage. This comparator is available whatever the EN pin level.

APPLICATION INFORMATION

Power Dissipation

Main contributor in term of junction temperature is the power dissipation of the power MOSFET. Assuming this, the power dissipation and the junction temperature in normal mode can be calculated with the following equations:

$$P_D = R_{DS(on)} \times (I_{out})^2 \quad (\text{eq. 1})$$

P_D = Power dissipation (W)
 $R_{DS(on)}$ = Power MOSFET on resistance (Ω)
 I_{out} = Output current (A)

$$T_J = R_D \times R_{\theta JA} + T_A \quad (\text{eq. 2})$$

T_J = Junction temperature ($^{\circ}\text{C}$)
 $R_{\theta JA}$ = Package thermal resistance ($^{\circ}\text{C}/\text{W}$)
 T_A = Ambient temperature ($^{\circ}\text{C}$)

Demoboard

The NCP456R integrates a 2 A rated NMOS FET, and the PCB rules must be respected to properly evacuate the heat out of the silicon.

The package is a CSP and due to the low thermal resistance of the silicon, all the balls can be used to improved power dissipation. Indeed, even if the power crosses the IN / OUT pins only, all the balls around this power area should be connected to the larger PCB area.

In the below PCB example (application demonstration board), all the PCB areas connected to 6 balls are enlarged. In addition vias are connected to bottom side with exactly same form factor of the other PCB side.

Additional improvements can be done also by using more copper thickness and the thinner epoxy as possible.

NCP456R

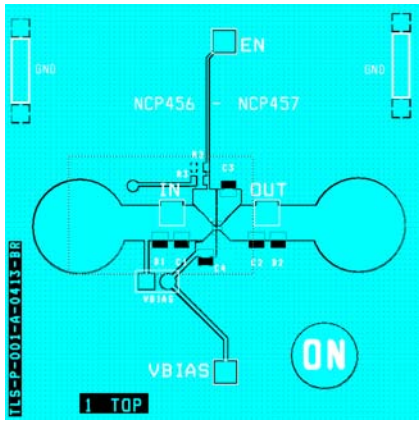


Figure 7. PCB Top View

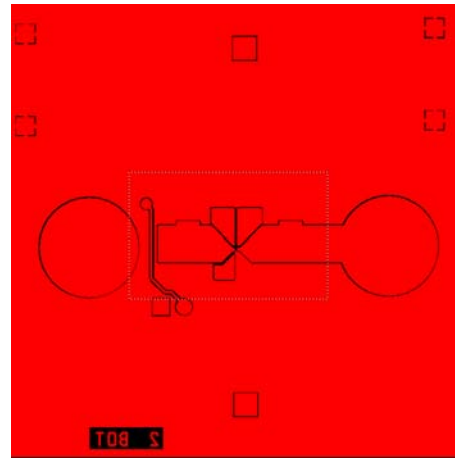


Figure 8. PCB Bottom View

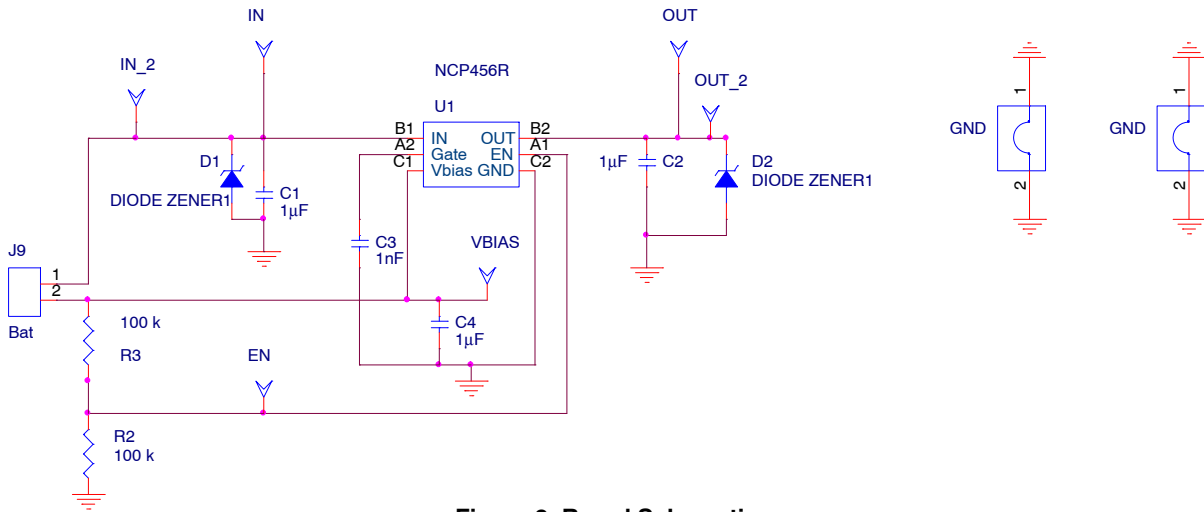


Figure 9. Board Schematic

NCP456R

BILL OF MATERIAL

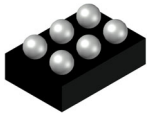
| Quantity | Reference schem | Part description | Part number | Manufacturer |
|----------|------------------------|-------------------------|-------------------------|------------------|
| 2 | IN, OUT | Socket, 4mm, metal, PK5 | B010 | HIRSCHMANN |
| 4 | IN_2, OUT_2, VBIAS, EN | HEADER200 | 2.54 mm, 77313-101-06LF | FC |
| 1 | J9 (Bat) | HEADER200-2 | 2.54 mm, 77313-101-06LF | FC |
| 3 | C1, C2, C4 | 1uF | GRM155R70J105KA12# | Murata |
| 1 | C3 | 1nF, Not mounted | GRM188R60J102ME47# | Murata |
| 1 | D1, D2 | TVS | ESD9x | ON semiconductor |
| 2 | GND2,GND | GND JUMPER | D3082F05 | Harvin |
| 2 | R2, R3 | Resistor 100k 0603 | MC 0.063 0603 1% 100K | MULTICOMP |
| 1 | U1 | Load switch | NCP456 - 457 | ON semiconductor |

ORDERING INFORMATION

| Device | Options | Marking | Package | Shipping |
|---------------|----------------------------|---------|--------------------------------|------------------|
| NCP456RFCCT2G | Reverse Voltage Protection | 56dYW | WLCSP 1.25 x 0.85 mm (Pb-Free) | 3000 Tape / Reel |

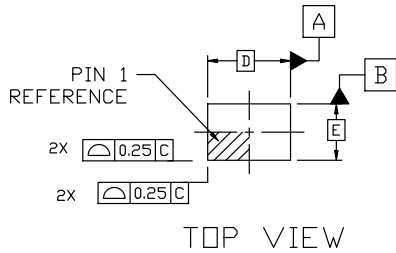
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

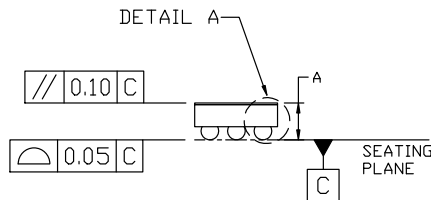


WLCSP6 1.25x0.85x0.559
CASE 567GZ
ISSUE C

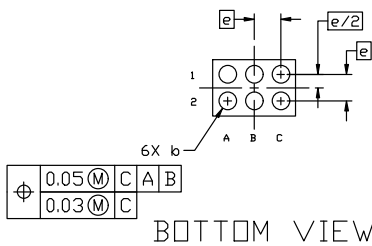
DATE 16 JUN 2022



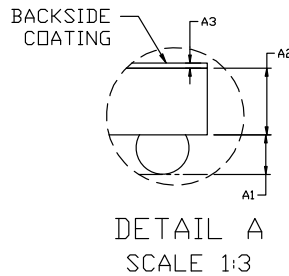
TOP VIEW



SIDE VIEW



BOTTOM VIEW

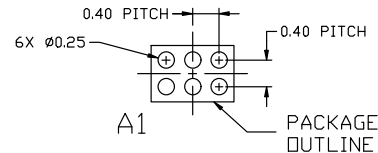


DETAIL A
SCALE 1:3

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION *b* IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER PARALLEL TO DATUM C.
4. COPLANARITY APPLIES TO THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. DATUM C, THE SEATING PLANE, IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

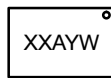
| DIM | MILLIMETERS | | |
|----------|-------------|-------|-------|
| | MIN. | NOM. | MAX. |
| A | 0.509 | 0.559 | 0.609 |
| A1 | 0.174 | 0.199 | 0.224 |
| A2 | 0.310 | 0.335 | 0.360 |
| A3 | 0.025 BSC | | |
| <i>b</i> | 0.240 | 0.265 | 0.290 |
| D | 1.25 BSC | | |
| E | 0.85 BSC | | |
| <i>e</i> | 0.40 BSC | | |



RECOMMENDED
MOUNTING FOOTPRINT*

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC
MARKING DIAGRAM*



A = Assembly Location
Y = Year
W = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

| | | |
|-------------------------|-------------------------------|--|
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| DESCRIPTION: | WLCSP6 1.25x0.85x0.559 | PAGE 1 OF 1 |

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