

# NID9N05ACL, NID9N05BCL

## Power MOSFET

### 9.0 A, 52 V, N-Channel, Logic Level, Clamped MOSFET w/ESD Protection in a DPAK Package



ON Semiconductor®

[www.onsemi.com](http://www.onsemi.com)

#### Benefits

- High Energy Capability for Inductive Loads
- Low Switching Noise Generation

#### Features

- Diode Clamp Between Gate and Source
- ESD Protection – HBM 5000 V
- Active Over-Voltage Gate to Drain Clamp
- Scalable to Lower or Higher  $R_{DS(on)}$
- Internal Series Gate Resistance
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

#### Applications

- Automotive and Industrial Markets:  
Solenoid Drivers, Lamp Drivers, Small Motor Drivers

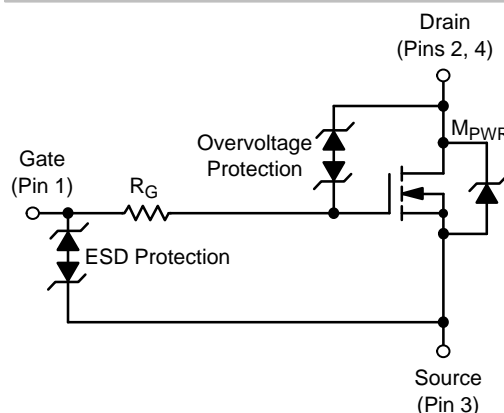
#### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage Internally Clamped	$V_{DSS}$	52–59	V
Gate-to-Source Voltage – Continuous	$V_{GS}$	$\pm 15$	V
Drain Current – Continuous @ $T_A = 25^\circ\text{C}$ – Single Pulse ( $t_p = 10 \mu\text{s}$ )	$I_D$ $I_{DM}$	9.0 35	A
Total Power Dissipation @ $T_A = 25^\circ\text{C}$	$P_D$	1.74	W
Operating and Storage Temperature Range	$T_J, T_{stg}$	–55 to 175	$^\circ\text{C}$
Single Pulse Drain-to-Source Avalanche Energy – Starting $T_J = 125^\circ\text{C}$ ( $V_{DD} = 50 \text{ V}$ , $I_{D(pk)} = 1.5 \text{ A}$ , $V_{GS} = 10 \text{ V}$ , $R_G = 25 \Omega$ )	$E_{AS}$	160	mJ
Thermal Resistance, Junction-to-Case Junction-to-Ambient (Note 1) Junction-to-Ambient (Note 2)	$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	5.2 72 100	$^\circ\text{C/W}$
Maximum Lead Temperature for Soldering Purposes, 1/8" from Case for 10 seconds	$T_L$	260	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. When surface mounted to a FR4 board using 1" pad size, (Cu area 1.127 in<sup>2</sup>).
2. When surface mounted to a FR4 board using minimum recommended pad size, (Cu area 0.412 in<sup>2</sup>).

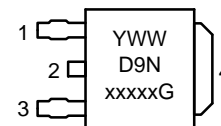
$V_{DSS}$ (Clamped)	$R_{DS(on)}$ TYP	$I_D$ MAX (Limited)
52 V	90 m $\Omega$	9.0 A



#### MARKING DIAGRAM



DPAK  
CASE 369C  
STYLE 2



Y	= Year	1	= Gate
WW	= Work Week	2	= Drain
xxxxx	= 05ACL or 05BCL	3	= Source
G	= Pb-Free Package	4	= Drain

#### ORDERING INFORMATION

Device	Package	Shipping†
NID9N05ACL4G	DPAK (Pb-Free)	2500/Tape & Reel
NID9N05BCL4G	DPAK (Pb-Free)	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

# NID9N05ACL, NID9N05BCL

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage (Note 3) (V <sub>GS</sub> = 0 V, I <sub>D</sub> = 1.0 mA, T <sub>J</sub> = 25°C) (V <sub>GS</sub> = 0 V, I <sub>D</sub> = 1.0 mA, T <sub>J</sub> = -40°C to 125°C) Temperature Coefficient (Negative)	V <sub>(BR)DSS</sub>	52 50.8 -	55 54 -10	59 59.5 -	V V mV/°C
Zero Gate Voltage Drain Current (V <sub>DS</sub> = 40 V, V <sub>GS</sub> = 0 V) (V <sub>DS</sub> = 40 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125°C)	I <sub>DSS</sub>	- -	- -	10 25	μA
Gate-Body Leakage Current (V <sub>GS</sub> = ±8 V, V <sub>DS</sub> = 0 V) (V <sub>GS</sub> = ±14 V, V <sub>DS</sub> = 0 V)	I <sub>GSS</sub>	- -	- ±22	±10 -	μA

### ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage (Note 3) (V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 100 μA) Threshold Temperature Coefficient (Negative)	V <sub>GS(th)</sub>	1.3 -	1.75 -4.5	2.5 -	V mV/°C
Static Drain-to-Source On-Resistance (Note 3) (V <sub>GS</sub> = 4.0 V, I <sub>D</sub> = 1.5 A) (V <sub>GS</sub> = 3.5 V, I <sub>D</sub> = 0.6 A) (V <sub>GS</sub> = 3.0 V, I <sub>D</sub> = 0.2 A) (V <sub>GS</sub> = 12 V, I <sub>D</sub> = 9.0 A) (V <sub>GS</sub> = 12 V, I <sub>D</sub> = 12 A)	R <sub>DS(on)</sub>	- - - 70 67	153 175 - 90 95	181 364 1210 - -	mΩ
Forward Transconductance (Note 3) (V <sub>DS</sub> = 15 V, I <sub>D</sub> = 9.0 A)	g <sub>FS</sub>	-	24	-	Mhos

### DYNAMIC CHARACTERISTICS

Input Capacitance	(V <sub>DS</sub> = 40 V, V <sub>GS</sub> = 0 V, f = 10 kHz)	C <sub>iss</sub>	-	155	250	pF
Output Capacitance		C <sub>oss</sub>	-	60	100	
Transfer Capacitance		C <sub>rss</sub>	-	25	40	
Input Capacitance	(V <sub>DS</sub> = 25 V, V <sub>GS</sub> = 0 V, f = 10 kHz)	C <sub>iss</sub>	-	175	-	pF
Output Capacitance		C <sub>oss</sub>	-	70	-	
Transfer Capacitance		C <sub>rss</sub>	-	30	-	

### SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	(V <sub>GS</sub> = 10 V, V <sub>DD</sub> = 40 V, I <sub>D</sub> = 9.0 A, R <sub>G</sub> = 9.0 Ω)	t <sub>d(on)</sub>	-	130	200	ns
Rise Time		t <sub>r</sub>	-	500	750	
Turn-Off Delay Time		t <sub>d(off)</sub>	-	1300	2000	
Fall Time		t <sub>f</sub>	-	1150	1850	
Turn-On Delay Time	(V <sub>GS</sub> = 10 V, V <sub>DD</sub> = 15 V, I <sub>D</sub> = 1.5 A, R <sub>G</sub> = 2 kΩ)	t <sub>d(on)</sub>	-	200	-	ns
Rise Time		t <sub>r</sub>	-	500	-	
Turn-Off Delay Time		t <sub>d(off)</sub>	-	2500	-	
Fall Time		t <sub>f</sub>	-	1800	-	
Turn-On Delay Time	(V <sub>GS</sub> = 10 V, V <sub>DD</sub> = 15 V, I <sub>D</sub> = 1.5 A, R <sub>G</sub> = 50 Ω)	t <sub>d(on)</sub>	-	120	-	ns
Rise Time		t <sub>r</sub>	-	275	-	
Turn-Off Delay Time		t <sub>d(off)</sub>	-	1600	-	
Fall Time		t <sub>f</sub>	-	1100	-	
Gate Charge	(V <sub>GS</sub> = 4.5 V, V <sub>DS</sub> = 40 V, I <sub>D</sub> = 9.0 A) (Note 3)	Q <sub>T</sub>	-	4.5	7.0	nC
		Q <sub>1</sub>	-	1.2	-	
		Q <sub>2</sub>	-	2.7	-	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

4. Switching characteristics are independent of operating junction temperatures.

# NID9N05ACL, NID9N05BCL

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

### SWITCHING CHARACTERISTICS (Note 4)

Gate Charge	(V <sub>GS</sub> = 4.5 V, V <sub>DS</sub> = 15 V, I <sub>D</sub> = 1.5 A) (Note 3)	Q <sub>T</sub>	–	3.6	–	nC
		Q <sub>1</sub>	–	1.0	–	
		Q <sub>2</sub>	–	2.0	–	

### SOURCE–DRAIN DIODE CHARACTERISTICS

Forward On–Voltage	(I <sub>S</sub> = 4.5 A, V <sub>GS</sub> = 0 V) (Note 3) (I <sub>S</sub> = 4.0 A, V <sub>GS</sub> = 0 V) (I <sub>S</sub> = 4.5 A, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125°C)	V <sub>SD</sub>	–	0.86	1.2	V
			–	0.845	–	
			–	0.725	–	
Reverse Recovery Time	(I <sub>S</sub> = 4.5 A, V <sub>GS</sub> = 0 V, di <sub>S</sub> /dt = 100 A/μs) (Note 3)	t <sub>rr</sub>	–	700	–	ns
		t <sub>a</sub>	–	200	–	
		t <sub>b</sub>	–	500	–	
Reverse Recovery Stored Charge		Q <sub>RR</sub>	–	6.5	–	μC

### ESD CHARACTERISTICS

Electro–Static Discharge Capability	Human Body Model (HBM)	ESD	5000	–	–	V
	Machine Model (MM)		500	–	–	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
4. Switching characteristics are independent of operating junction temperatures.

# NID9N05ACL, NID9N05BCL

## TYPICAL PERFORMANCE CURVES

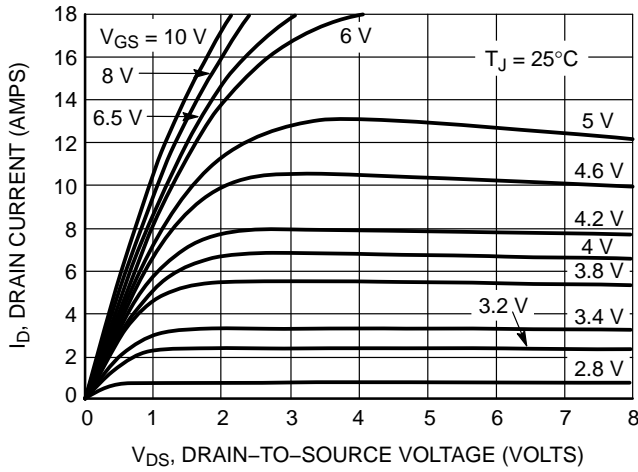


Figure 1. On-Region Characteristics

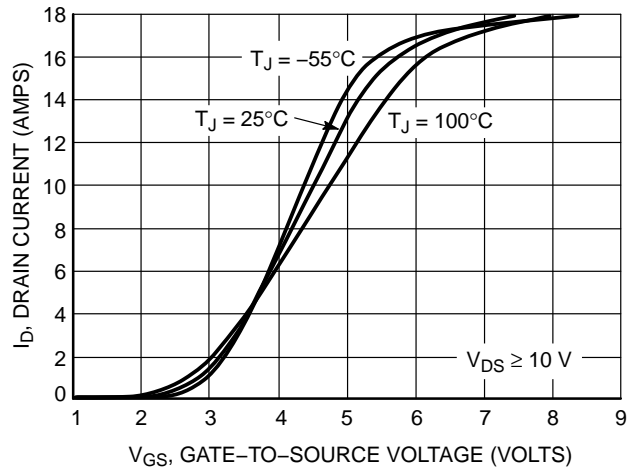


Figure 2. Transfer Characteristics

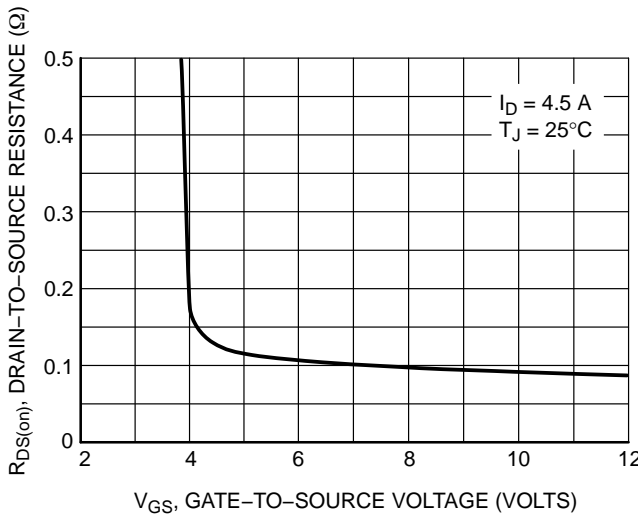


Figure 3. On-Resistance versus Gate-to-Source Voltage

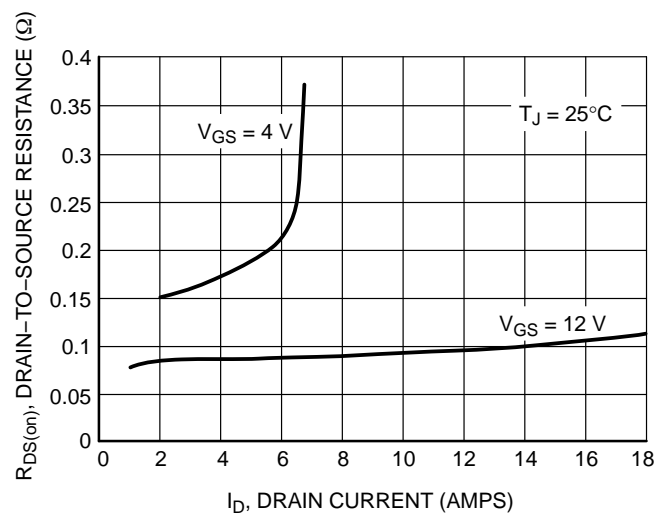


Figure 4. On-Resistance versus Drain Current and Gate Voltage

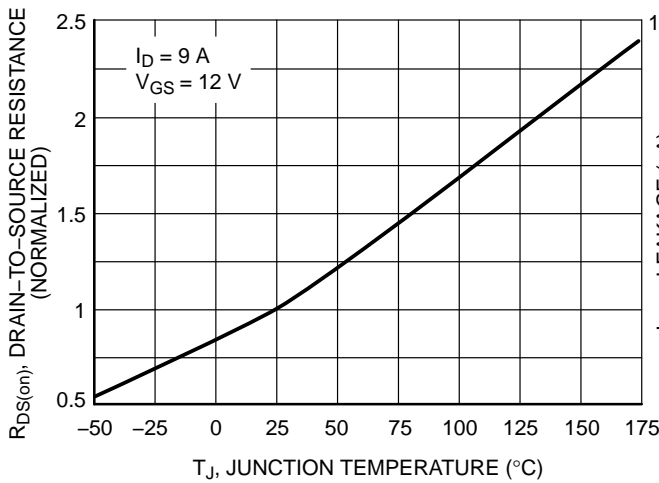


Figure 5. On-Resistance Variation with Temperature

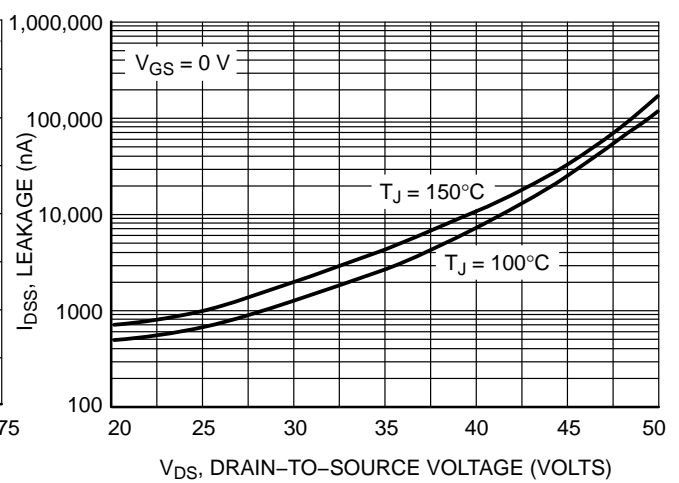


Figure 6. Drain-to-Source Leakage Current versus Voltage

# NID9N05ACL, NID9N05BCL

## TYPICAL PERFORMANCE CURVES

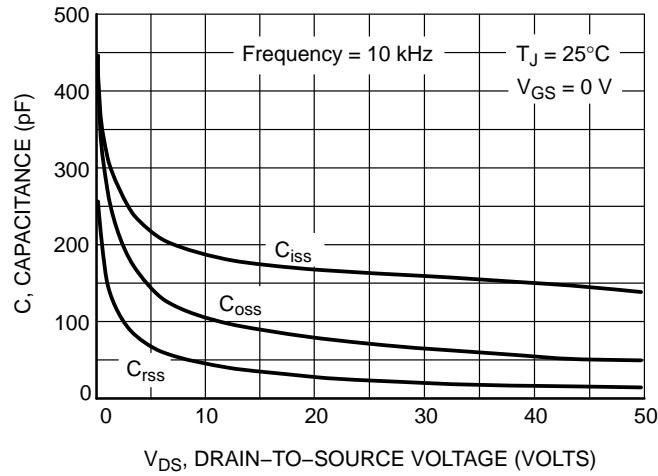


Figure 7. Capacitance Variation

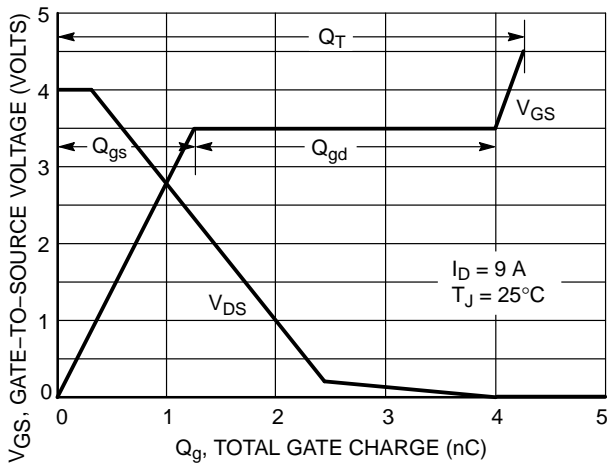


Figure 8. Gate-To-Source and Drain-To-Source Voltage versus Total Charge

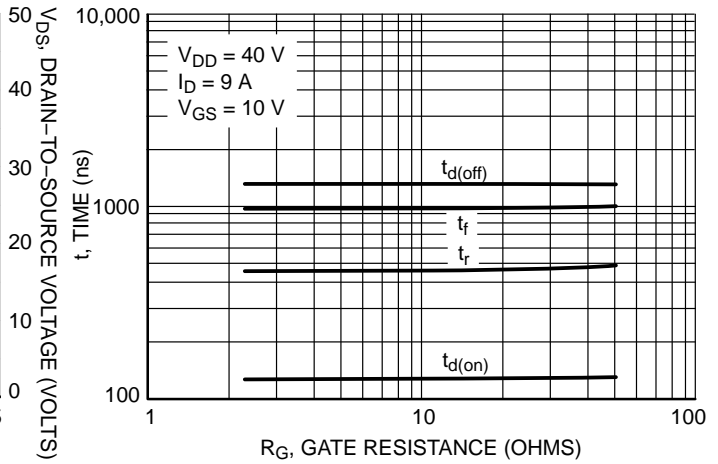


Figure 9. Resistive Switching Time Variation versus Gate Resistance

## DRAIN-TO-SOURCE DIODE CHARACTERISTICS

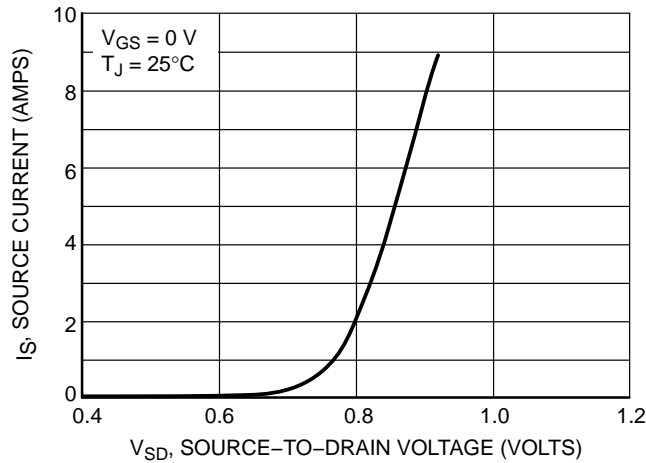


Figure 10. Diode Forward Voltage versus Current

# NID9N05ACL, NID9N05BCL

## SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain-to-source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ( $T_C$ ) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, "Transient Thermal Resistance – General Data and Its Use."

Switching between the off-state and the on-state may traverse any load line provided neither rated peak current ( $I_{DM}$ ) nor rated voltage ( $V_{DSS}$ ) is exceeded and the transition time ( $t_r, t_f$ ) do not exceed 10  $\mu$ s. In addition the total power averaged over a complete switching cycle must not exceed  $(T_{J(MAX)} - T_C)/(R_{\theta JC})$ .

A Power MOSFET designated E-FET can be safely used in switching circuits with unclamped inductive loads. For

reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non-linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E-FETs can withstand the stress of drain-to-source avalanche at currents up to rated pulsed current ( $I_{DM}$ ), the energy rating is specified at rated continuous current ( $I_D$ ), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous  $I_D$  can safely be assumed to equal the values indicated.

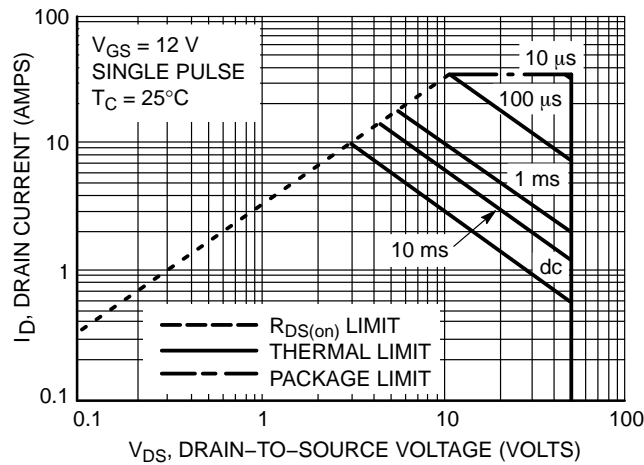


Figure 11. Maximum Rated Forward Biased Safe Operating Area

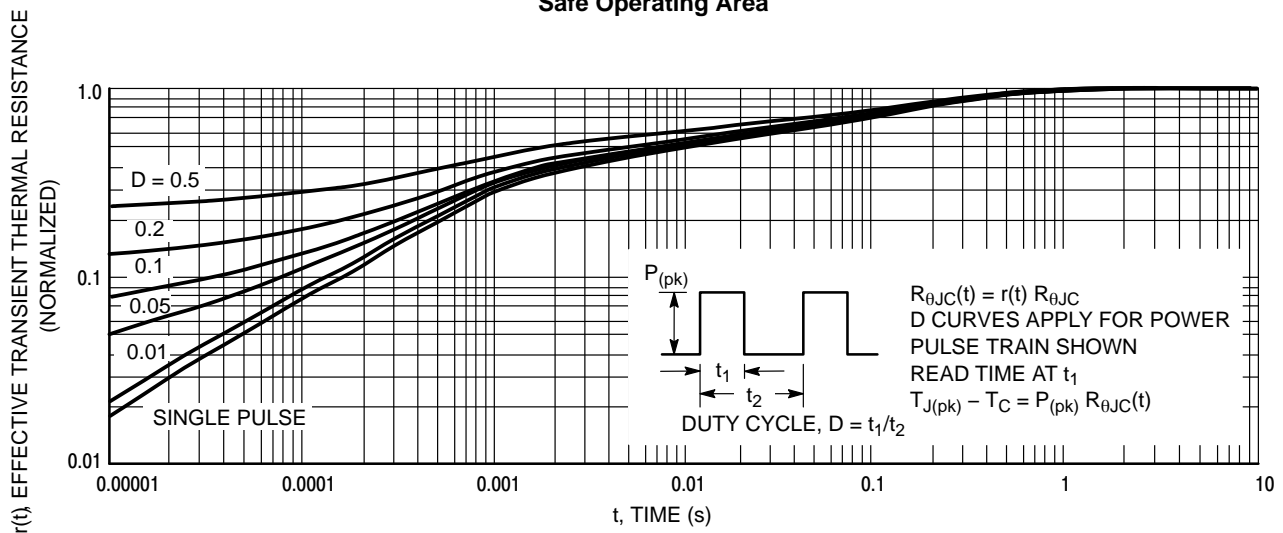


Figure 12. Thermal Response

# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



## DPAK (SINGLE GAUGE) CASE 369C ISSUE F

DATE 21 JUL 2015

SCALE 1:1



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.028	0.045	0.72	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090	BSC	2.29	BSC
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.114	REF	2.90	REF
L2	0.020	BSC	0.51	BSC
L3	0.035	0.050	0.89	1.27
L4	---	0.040	---	1.01
Z	0.155	---	3.93	---

### GENERIC MARKING DIAGRAM\*

- |  |  |   |   |  |
|--|--|---|---|--|
| <p>STYLE 1:<br/>PIN 1. BASE<br/>2. COLLECTOR<br/>3. EMITTER<br/>4. COLLECTOR</p> | <p>STYLE 2:<br/>PIN 1. GATE<br/>2. DRAIN<br/>3. SOURCE<br/>4. DRAIN</p>          | <p>STYLE 3:<br/>PIN 1. ANODE<br/>2. CATHODE<br/>3. ANODE<br/>4. CATHODE</p> | <p>STYLE 4:<br/>PIN 1. CATHODE<br/>2. ANODE<br/>3. GATE<br/>4. ANODE</p>              | <p>STYLE 5:<br/>PIN 1. GATE<br/>2. ANODE<br/>3. CATHODE<br/>4. ANODE</p>     |
| <p>STYLE 6:<br/>PIN 1. MT1<br/>2. MT2<br/>3. GATE<br/>4. MT2</p>                 | <p>STYLE 7:<br/>PIN 1. GATE<br/>2. COLLECTOR<br/>3. EMITTER<br/>4. COLLECTOR</p> | <p>STYLE 8:<br/>PIN 1. N/C<br/>2. CATHODE<br/>3. ANODE<br/>4. CATHODE</p>   | <p>STYLE 9:<br/>PIN 1. ANODE<br/>2. CATHODE<br/>3. RESISTOR ADJUST<br/>4. CATHODE</p> | <p>STYLE 10:<br/>PIN 1. CATHODE<br/>2. ANODE<br/>3. CATHODE<br/>4. ANODE</p> |



- XXXXXX = Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

### SOLDERING FOOTPRINT\*



SCALE 3:1 (mm/inches)

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DOCUMENT NUMBER:	98AON10527D	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	DPAK (SINGLE GAUGE)	PAGE 1 OF 1

onsemi and ONSEMI are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

**onsemi**, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## PUBLICATION ORDERING INFORMATION

### LITERATURE FULFILLMENT:

Email Requests to: [orderlit@onsemi.com](mailto:orderlit@onsemi.com)

**onsemi Website:** [www.onsemi.com](http://www.onsemi.com)

### TECHNICAL SUPPORT

**North American Technical Support:**  
Voice Mail: 1 800-282-9855 Toll Free USA/Canada  
Phone: 011 421 33 790 2910

**Europe, Middle East and Africa Technical Support:**

Phone: 00421 33 790 2910

For additional information, please contact your local Sales Representative