

# NID5004N

## Self-Protected FET with Temperature and Current Limit

40 V, 6.5 A, Single N-Channel, DPAK

Self-protected FETs are a series of power MOSFETs which utilize ON Semiconductor HDPlus™ technology. The self-protected MOSFET incorporates protection features such as integrated thermal and current limits. The self-protected MOSFETs include an integrated Drain-to-Gate Clamp that provides overvoltage protection from transients and avalanche. The device is protected from Electrostatic Discharge (ESD) by utilizing an integrated Gate-to-Source Clamp.

### Features

- Short Circuit Protection
- In Rush Current Limit
- Thermal Shutdown with Automatic Restart
- Avalanche Rated
- Overvoltage Protection
- ESD Protection (4 kV HBM)
- Controlled Slew Rate for Low Noise Switching
- AEC Q101 Qualified
- This is a Pb-Free Device

### Applications

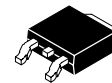
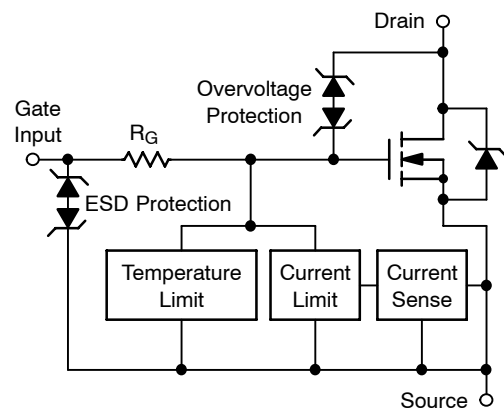
- Solenoid Driver
- Relay Driver
- Small Motors
- Lighting
- Relay Replacement
- Load Switching



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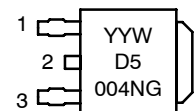
<http://onsemi.com>

V <sub>DSS</sub> (Clamped)	R <sub>DS(on)</sub> Typ	I <sub>D</sub> Typ (Limited)
40 V	110 mΩ @ 10 V	6.5 A



DPAK  
CASE 369C  
STYLE 2

### MARKING DIAGRAM



D5004N = Device Code  
Y = Year  
WW = Work Week  
G = Pb-Free Device

1 = Gate  
2 = Drain  
3 = Source

### ORDERING INFORMATION

Device	Package	Shipping†
NID5004NT4G	DPAK (Pb-Free)	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

## NID5004N

### MOSFET MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage Internally Clamped	$V_{DSS}$	44	Vdc
Gate-to-Source Voltage	$V_{GS}$	$\pm 14$	Vdc
Drain Current Continuous	$I_D$	Internally Limited	
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ (Note 1) @ $T_A = 25^\circ\text{C}$ (Note 2)	$P_D$	1.3 2.5	W
Thermal Resistance Junction-to-Case Junction-to-Ambient (Note 1) Junction-to-Ambient (Note 2)	$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	3.0 95 50	$^\circ\text{C/W}$
Single Pulse Drain-to-Source Avalanche Energy ( $V_{DD} = 30\text{ Vdc}$ , $V_{GS} = 5.0\text{ Vdc}$ , $I_L = 1.8\text{ Apk}$ , $L = 160\text{ mH}$ , $R_G = 25\ \Omega$ ) (Note 3)	$E_{AS}$	273	mJ
Operating and Storage Temperature Range (Note 4)	$T_J, T_{stg}$	-55 to 150	$^\circ\text{C}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Surface mounted onto minimum pad size (100 sq/mm) FR4 PCB, 1 oz cu.
2. Mounted onto 1" square pad size (700 sq/mm) FR4 PCB, 1 oz cu.
3. Not subject to Production Test
4. Normal pre-fault operating range. See thermal limit range conditions.

# NID5004N

## MOSFET ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>					
Drain-to-Source Clamped Breakdown Voltage ( $V_{GS} = 0\text{ V}$ , $I_D = 2\text{ mA}$ )	$V_{(BR)DSS}$	36	40	44	V
Zero Gate Voltage Drain Current ( $V_{DS} = 32\text{ V}$ , $V_{GS} = 0\text{ V}$ )	$I_{DSS}$	-	27	100	$\mu\text{A}$
Gate Input Current ( $V_{GS} = 5.0\text{ V}$ , $V_{DS} = 0\text{ V}$ )	$I_{GSS}$	-	45	200	$\mu\text{A}$

## ON CHARACTERISTICS

Gate Threshold Voltage ( $V_{DS} = V_{GS}$ , $I_D = 150\ \mu\text{A}$ ) Threshold Temperature Coefficient	$V_{GS(th)}$	1.0 -	1.85 5.0	2.2 -	V -mV/ $^\circ\text{C}$
Static Drain-to-Source On-Resistance (Note 5) ( $V_{GS} = 10\text{ V}$ , $I_D = 2.0\text{ A}$ , $T_J @ 25^\circ\text{C}$ )	$R_{DS(on)}$	-	110	130	m $\Omega$
Static Drain-to-Source On-Resistance (Note 5) ( $V_{GS} = 5.0\text{ V}$ , $I_D = 2.0\text{ A}$ , $T_J @ 25^\circ\text{C}$ ) ( $V_{GS} = 5.0\text{ V}$ , $I_D = 2.0\text{ A}$ , $T_J @ 150^\circ\text{C}$ )	$R_{DS(on)}$	- -	130 240	150 270	m $\Omega$
Source-Drain Forward On Voltage ( $I_S = 7.0\text{ A}$ , $V_{GS} = 0\text{ V}$ )	$V_{SD}$	-	0.9	1.1	V

## SWITCHING CHARACTERISTICS (Note 6)

Turn-on Delay Time	$R_L = 6.6\ \Omega$ , $V_{in} = 0\text{ to }10\text{ V}$ , $V_{DD} = 13.8\text{ V}$ , $I_D = 2.0\text{ A}$ , 10% $V_{in}$ to 10% $I_D$	$t_{d(on)}$	-	97	115	ns
Turn-on Rise Time	$R_L = 6.6\ \Omega$ , $V_{in} = 0\text{ to }10\text{ V}$ , $V_{DD} = 13.8\text{ V}$ , $I_D = 2.0\text{ A}$ , 10% $I_D$ to 90% $I_D$	$t_{rise}$	-	282	300	ns
Turn-off Delay Time	$R_L = 6.6\ \Omega$ , $V_{in} = 0\text{ to }10\text{ V}$ , $V_{DD} = 13.8\text{ V}$ , $I_D = 2.0\text{ A}$ , 90% $V_{in}$ to 90% $I_D$	$t_{d(off)}$	-	930	1020	ns
Turn-off Fall Time	$R_L = 6.6\ \Omega$ , $V_{in} = 0\text{ to }10\text{ V}$ , $V_{DD} = 13.8\text{ V}$ , $I_D = 2.0\text{ A}$ , 90% $I_D$ to 10% $I_D$	$t_{fall}$	-	690	750	ns
Slew Rate ON	$R_L = 6.6\ \Omega$ , $V_{in} = 0\text{ to }10\text{ V}$ , $V_{DD} = 13.8\text{ V}$ , $I_D = 2.0\text{ A}$ , 70% to 50% $V_{DD}$	$dV_{DS}/dT_{on}$	-	64	-	V/ $\mu\text{s}$
Slew Rate OFF	$R_L = 6.6\ \Omega$ , $V_{in} = 0\text{ to }10\text{ V}$ , $V_{DD} = 13.8\text{ V}$ , $I_D = 2.0\text{ A}$ , 50% to 70% $V_{DD}$	$dV_{DS}/dT_{off}$	-	28	-	V/ $\mu\text{s}$

## SELF PROTECTION CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise noted) (Note 7)

Current Limit	$V_{DS} = 10\text{ V}$ , $V_{GS} = 5.0\text{ V}$ , $T_J = 25^\circ\text{C}$ (Note 8) $V_{DS} = 10\text{ V}$ , $V_{GS} = 5.0\text{ V}$ , $T_J = 100^\circ\text{C}$ (Note 6, 8) $V_{DS} = 10\text{ V}$ , $V_{GS} = 10\text{ V}$ , $T_J = 25^\circ\text{C}$ (Note 6, 8)	$I_{LIM}$	4.0 4.0 -	6.5 5.5 7.9	11 11 -	A
Temperature Limit (Turn-off)	$V_{GS} = 5.0\text{ V}$ (Note 6)	$T_{LIM(off)}$	150	180	200	$^\circ\text{C}$
Thermal Hysteresis	$V_{GS} = 5.0\text{ V}$	$\Delta T_{LIM(on)}$	-	10	-	$^\circ\text{C}$
Temperature Limit (Turn-off)	$V_{GS} = 10\text{ V}$ (Note 6)	$T_{LIM(off)}$	150	180	200	$^\circ\text{C}$
Thermal Hysteresis	$V_{GS} = 10\text{ V}$	$\Delta T_{LIM(on)}$	-	20	-	$^\circ\text{C}$
Input Current during Thermal Fault	$V_{DS} = 0\text{ V}$ , $V_{GS} = 5.0\text{ V}$ , $T_J = T_J > T_{(fault)}$ (Note 6) $V_{DS} = 0\text{ V}$ , $V_{GS} = 10\text{ V}$ , $T_J = T_J > T_{(fault)}$ (Note 6)	$I_{g(fault)}$	5.5 12	5.2 11	-	mA

## ESD ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Electrostatic Discharge Capability Human Body Model (HBM) Machine Model (MM) (Note 6)	ESD	4000 400	- -	- -	V
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5. Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\leq 2\%$ .
6. Not subject to Production Test
7. Fault conditions are viewed as beyond the normal operating range of the part.
8. Current limit measured at  $380\ \mu\text{s}$  after gate pulse.

TYPICAL PERFORMANCE CURVES

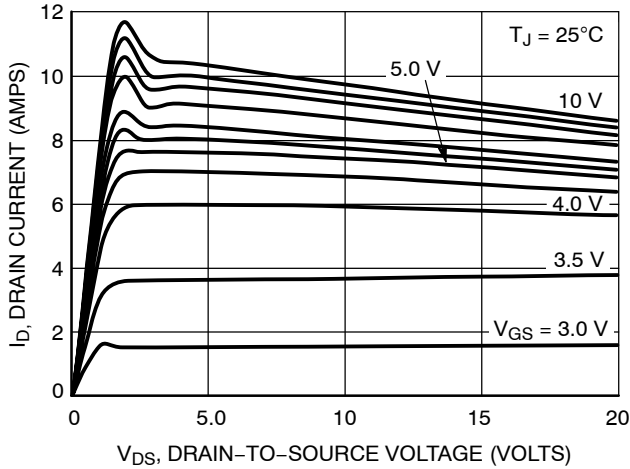


Figure 1. On-Region Characteristics

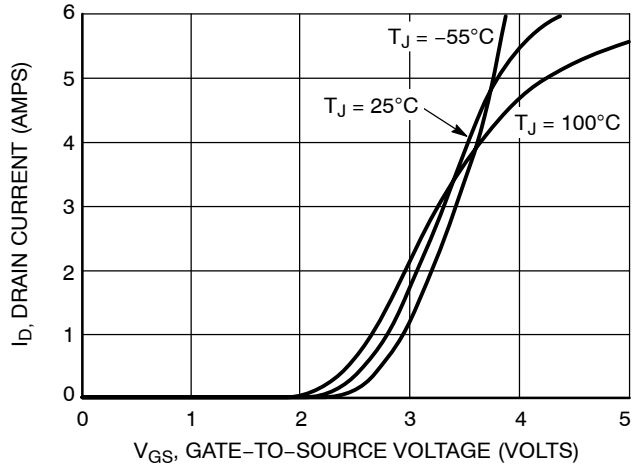


Figure 2. Transfer Characteristics

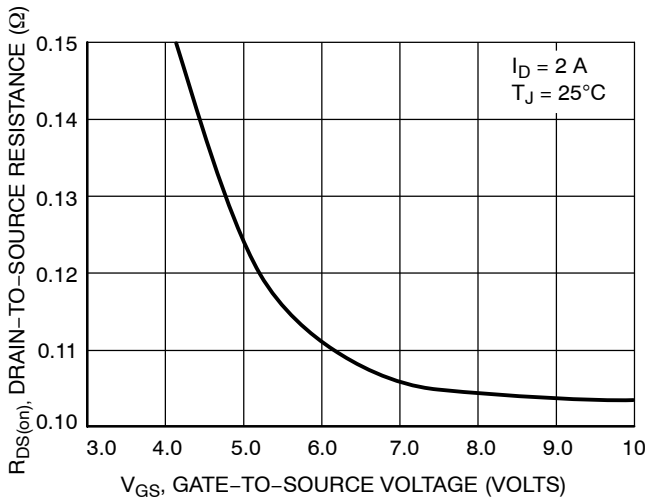


Figure 3. On-Resistance vs. Gate-to-Source Voltage

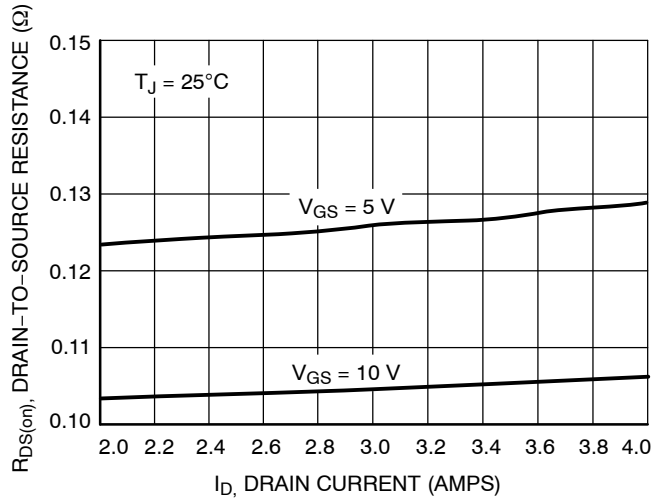


Figure 4. On-Resistance vs. Drain Current

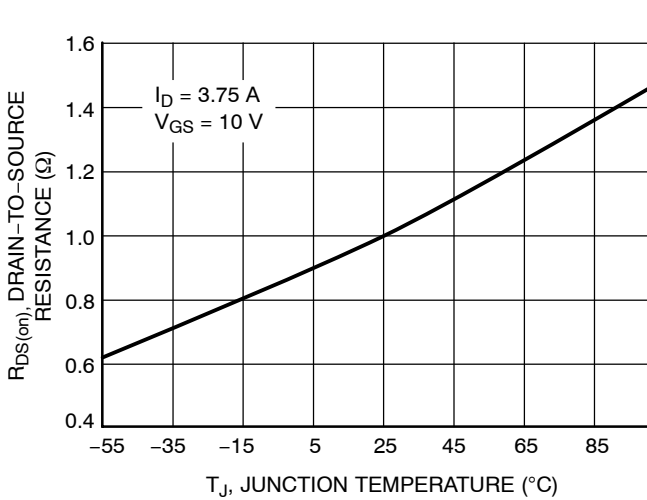


Figure 5. On-Resistance Variation with Temperature

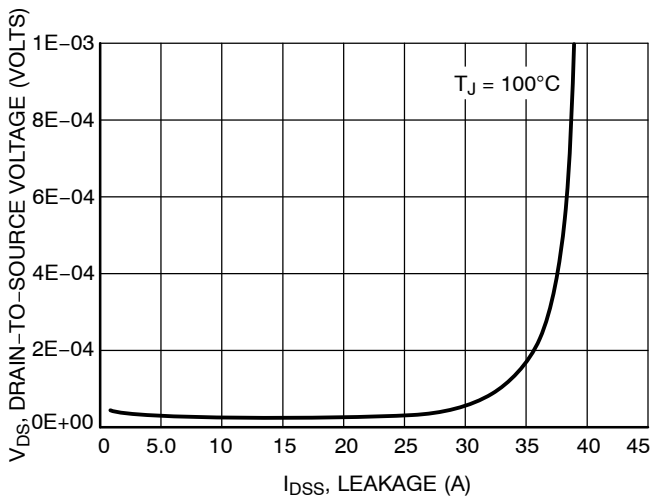


Figure 6. Drain-to-Source Leakage Current vs. Voltage

# NID5004N

## z TYPICAL PERFORMANCE CURVES

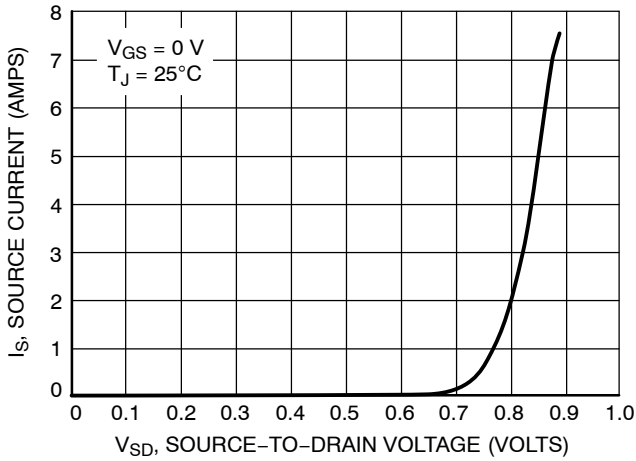


Figure 7. Diode Forward Voltage vs. Current

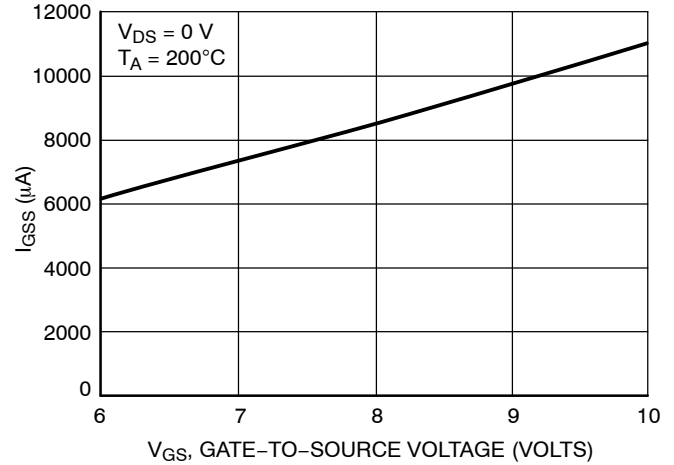


Figure 8. Input Current vs. Gate Voltage

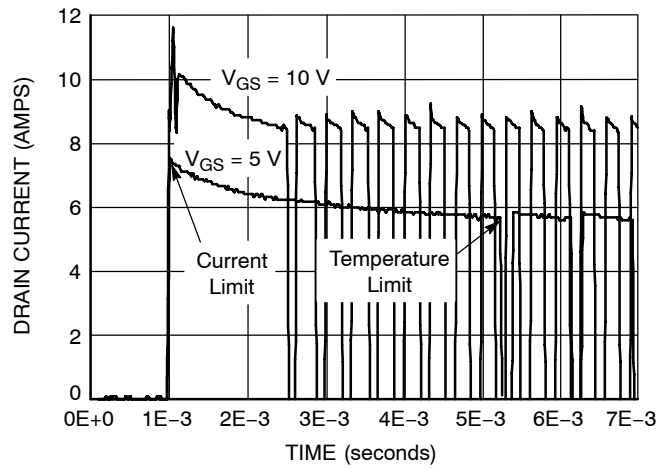


Figure 9. Short Circuit Response\*

\*(Actual thermal cycling response in short circuit dependent on device power level, thermal mounting, and ambient temperature conditions)

# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



## DPAK (SINGLE GAUGE) CASE 369C ISSUE F

DATE 21 JUL 2015

SCALE 1:1



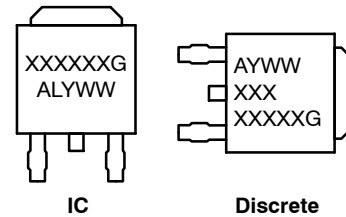
**NOTES:**

- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
- CONTROLLING DIMENSION: INCHES.
- THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
- DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
- DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
- DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
- OPTIONAL MOLD FEATURE.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.028	0.045	0.72	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090	BSC	2.29	BSC
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.114	REF	2.90	REF
L2	0.020	BSC	0.51	BSC
L3	0.035	0.050	0.89	1.27
L4	---	0.040	---	1.01
Z	0.155	---	3.93	---

### GENERIC MARKING DIAGRAM\*

- |   |   |  |  |   |
|---|---|--|--|---|
| <p><b>STYLE 1:</b><br/>PIN 1. BASE<br/>2. COLLECTOR<br/>3. EMITTER<br/>4. COLLECTOR</p> | <p><b>STYLE 2:</b><br/>PIN 1. GATE<br/>2. DRAIN<br/>3. SOURCE<br/>4. DRAIN</p>          | <p><b>STYLE 3:</b><br/>PIN 1. ANODE<br/>2. CATHODE<br/>3. ANODE<br/>4. CATHODE</p> | <p><b>STYLE 4:</b><br/>PIN 1. CATHODE<br/>2. ANODE<br/>3. GATE<br/>4. ANODE</p>              | <p><b>STYLE 5:</b><br/>PIN 1. GATE<br/>2. ANODE<br/>3. CATHODE<br/>4. ANODE</p>     |
| <p><b>STYLE 6:</b><br/>PIN 1. MT1<br/>2. MT2<br/>3. GATE<br/>4. MT2</p>                 | <p><b>STYLE 7:</b><br/>PIN 1. GATE<br/>2. COLLECTOR<br/>3. EMITTER<br/>4. COLLECTOR</p> | <p><b>STYLE 8:</b><br/>PIN 1. N/C<br/>2. CATHODE<br/>3. ANODE<br/>4. CATHODE</p>   | <p><b>STYLE 9:</b><br/>PIN 1. ANODE<br/>2. CATHODE<br/>3. RESISTOR ADJUST<br/>4. CATHODE</p> | <p><b>STYLE 10:</b><br/>PIN 1. CATHODE<br/>2. ANODE<br/>3. CATHODE<br/>4. ANODE</p> |



- XXXXXX = Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

### SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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