

# MC14099B

## 8-Bit Addressable Latches

The MC14099B is an 8-bit addressable latch. Data is entered in serial form when the appropriate latch is addressed (via address pins A0, A1, A2) and write disable is in the low state. For the MC14099B the input is a unidirectional write only port.

The data is presented in parallel at the output of the eight latches independently of the state of Write Disable, Write/Read or Chip Enable.

A Master Reset capability is available on both parts.

### Features

- Serial Data Input
- Parallel Output
- Master Reset
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-Power Schottky TTL Load over the Rated Temperature Range
- MC14099B pin for pin compatible with CD4099B
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- This Device is Pb-Free and is RoHS Compliant

### MAXIMUM RATINGS (Voltages Referenced to $V_{SS}$ )

| Symbol            | Parameter                                         | Value                  | Unit |
|-------------------|---------------------------------------------------|------------------------|------|
| $V_{DD}$          | DC Supply Voltage Range                           | -0.5 to +18.0          | V    |
| $V_{in}, V_{out}$ | Input or Output Voltage Range (DC or Transient)   | -0.5 to $V_{DD} + 0.5$ | V    |
| $I_{in}, I_{out}$ | Input or Output Current (DC or Transient) per Pin | $\pm 10$               | mA   |
| $P_D$             | Power Dissipation, per Package (Note 1)           | 500                    | mW   |
| $T_A$             | Ambient Temperature Range                         | -55 to +125            | °C   |
| $T_{stg}$         | Storage Temperature Range                         | -65 to +150            | °C   |
| $T_L$             | Lead Temperature (8-Second Soldering)             | 260                    | °C   |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Temperature Derating: "D/DW" Packages: -7.0 mW/°C From 65°C To 125°C

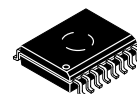
This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either  $V_{SS}$  or  $V_{DD}$ ). Unused outputs must be left open.



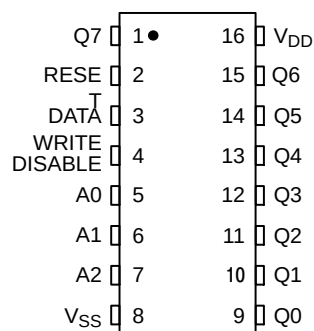
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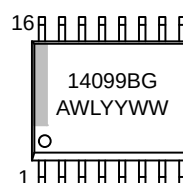


SOIC-16 WD  
DW SUFFIX  
CASE 751G

### PIN ASSIGNMENT



### MARKING DIAGRAM

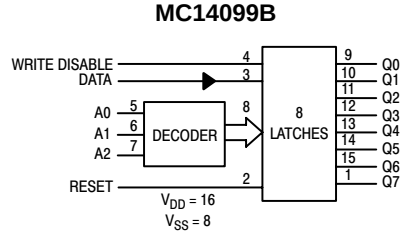


A = Assembly Location  
WL = Wafer Lot  
YY = Year  
WW = Work Week  
G = Pb-Free Indicator

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

# MC14099B



## ELECTRICAL CHARACTERISTICS (Voltages Referenced to $V_{SS}$ )

| Characteristic                                                                                                                                                                                           | Symbol                | $V_{DD}$<br>Vdc | -55°C                                                                                                          |           | 25°C  |                 |           | 125°C |           | Unit      |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------|-----------------|----------------------------------------------------------------------------------------------------------------|-----------|-------|-----------------|-----------|-------|-----------|-----------|
|                                                                                                                                                                                                          |                       |                 | Min                                                                                                            | Max       | Min   | Typ<br>(Note 2) | Max       | Min   | Max       |           |
| Output Voltage<br>$V_{in} = V_{DD}$ or 0                                                                                                                                                                 | “0” Level<br>$V_{OL}$ | 5.0             | –                                                                                                              | 0.05      | –     | 0               | 0.05      | –     | 0.05      | Vdc       |
|                                                                                                                                                                                                          |                       | 10              | –                                                                                                              | 0.05      | –     | 0               | 0.05      | –     | 0.05      |           |
|                                                                                                                                                                                                          |                       | 15              | –                                                                                                              | 0.05      | –     | 0               | 0.05      | –     | 0.05      |           |
|                                                                                                                                                                                                          | “1” Level<br>$V_{OH}$ | 5.0             | 4.95                                                                                                           | –         | 4.95  | 5.0             | –         | 4.95  | –         | Vdc       |
|                                                                                                                                                                                                          |                       | 10              | 9.95                                                                                                           | –         | 9.95  | 10              | –         | 9.95  | –         |           |
|                                                                                                                                                                                                          |                       | 15              | 14.95                                                                                                          | –         | 14.95 | 15              | –         | 14.95 | –         |           |
| Input Voltage<br>( $V_O = 4.5$ or $0.5$ Vdc)<br>( $V_O = 9.0$ or $1.0$ Vdc)<br>( $V_O = 13.5$ or $1.5$ Vdc)                                                                                              | “0” Level<br>$V_{IL}$ | 5.0             | –                                                                                                              | 1.5       | –     | 2.25            | 1.5       | –     | 1.5       | Vdc       |
|                                                                                                                                                                                                          |                       | 10              | –                                                                                                              | 3.0       | –     | 4.50            | 3.0       | –     | 3.0       |           |
|                                                                                                                                                                                                          |                       | 15              | –                                                                                                              | 4.0       | –     | 6.75            | 4.0       | –     | 4.0       |           |
|                                                                                                                                                                                                          | “1” Level<br>$V_{IH}$ | 5.0             | 3.5                                                                                                            | –         | 3.5   | 2.75            | –         | 3.5   | –         | Vdc       |
|                                                                                                                                                                                                          |                       | 10              | 7.0                                                                                                            | –         | 7.0   | 5.50            | –         | 7.0   | –         |           |
|                                                                                                                                                                                                          |                       | 15              | 11                                                                                                             | –         | 11    | 8.25            | –         | 11    | –         |           |
| Output Drive Current<br>( $V_{OH} = 2.5$ Vdc)<br>( $V_{OH} = 4.6$ Vdc)<br>( $V_{OH} = 9.5$ Vdc)<br>( $V_{OH} = 13.5$ Vdc)<br><br>( $V_{OL} = 0.4$ Vdc)<br>( $V_{OL} = 0.5$ Vdc)<br>( $V_{OL} = 1.5$ Vdc) | Source<br>$I_{OH}$    | 5.0             | –3.0                                                                                                           | –         | –2.4  | –4.2            | –         | –1.7  | –         | mAdc      |
|                                                                                                                                                                                                          |                       | 5.0             | –0.64                                                                                                          | –         | –0.51 | –0.88           | –         | –0.36 | –         |           |
|                                                                                                                                                                                                          |                       | 10              | –1.6                                                                                                           | –         | –1.3  | –2.25           | –         | –0.9  | –         |           |
|                                                                                                                                                                                                          |                       | 15              | –4.2                                                                                                           | –         | –3.4  | –8.8            | –         | –2.4  | –         |           |
|                                                                                                                                                                                                          | Sink<br>$I_{OL}$      | 5.0             | 0.64                                                                                                           | –         | 0.51  | 0.88            | –         | 0.36  | –         | mAdc      |
|                                                                                                                                                                                                          |                       | 10              | 1.6                                                                                                            | –         | 1.3   | 2.25            | –         | 0.9   | –         |           |
|                                                                                                                                                                                                          |                       | 15              | 4.2                                                                                                            | –         | 3.4   | 8.8             | –         | 2.4   | –         |           |
| Input Current                                                                                                                                                                                            | $I_{in}$              | 15              | –                                                                                                              | $\pm 0.1$ | –     | $\pm 0.00001$   | $\pm 0.1$ | –     | $\pm 1.0$ | $\mu$ Adc |
| Input Capacitance ( $V_{in} = 0$ )                                                                                                                                                                       | $C_{in}$              | –               | –                                                                                                              | –         | –     | 5.0             | 7.5       | –     | –         | pF        |
| Input Capacitance<br>MC14599B — Data (pin 3)<br>( $V_{in} = 0$ )                                                                                                                                         | $C_{in}$              | –               | –                                                                                                              | –         | –     | 15              | 22.5      | –     | –         | pF        |
| Quiescent Current<br>(Per Package)                                                                                                                                                                       | $I_{DD}$              | 5.0             | –                                                                                                              | 5.0       | –     | 0.005           | 5.0       | –     | 150       | $\mu$ Adc |
|                                                                                                                                                                                                          |                       | 10              | –                                                                                                              | 10        | –     | 0.010           | 10        | –     | 300       |           |
|                                                                                                                                                                                                          |                       | 15              | –                                                                                                              | 20        | –     | 0.015           | 20        | –     | 600       |           |
| Total Supply Current (Notes 3 & 4)<br>(Dynamic plus Quiescent,<br>Per Package)<br>( $C_L = 50$ pF on all outputs, all<br>buffers switching)                                                              | $I_T$                 | 5.0<br>10<br>15 | $I_T = (1.5 \mu A/kHz) f + I_{DD}$<br>$I_T = (3.0 \mu A/kHz) f + I_{DD}$<br>$I_T = (4.5 \mu A/kHz) f + I_{DD}$ |           |       |                 |           |       |           | $\mu$ Adc |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.

3. The formulas given are for the typical characteristics only at 25°C.

4. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) Vfk$$

where:  $I_T$  is in  $\mu A$  (per package),  $C_L$  in pF,  $V = (V_{DD} - V_{SS})$  in volts,  $f$  in kHz is input frequency, and  $k = 0.004$ .

# MC14099B

## SWITCHING CHARACTERISTICS (Note 5) ( $C_L = 50$ pF, $T_A = 25^\circ\text{C}$ )

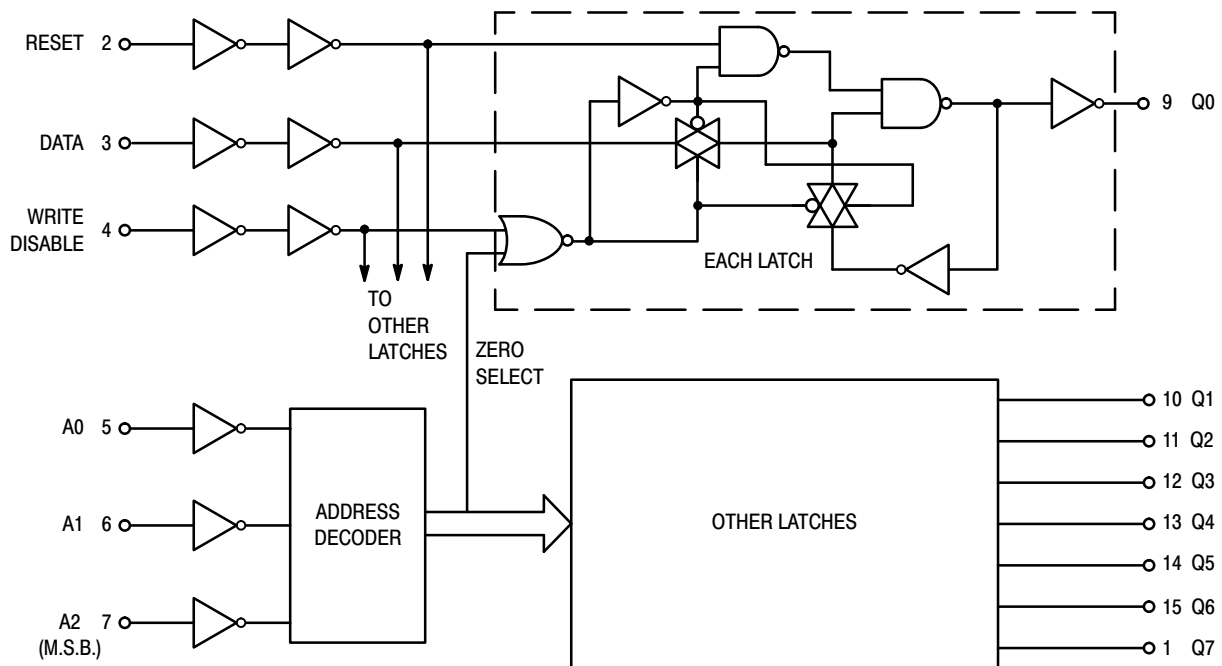
| Characteristic                                                                                                                                                                                                             | Symbol                   | $V_{DD}$<br>Vdc | Min               | Typ<br>(Note 6)      | Max               | Unit |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------|-----------------|-------------------|----------------------|-------------------|------|
| Output Rise and Fall Time<br>$t_{TLH}, t_{THL} = (1.35 \text{ ns/pF}) C_L + 32 \text{ ns}$<br>$t_{TLH}, t_{THL} = (0.6 \text{ ns/pF}) C_L + 20 \text{ ns}$<br>$t_{TLH}, t_{THL} = (0.4 \text{ ns/pF}) C_L + 20 \text{ ns}$ | $t_{TLH},$<br>$t_{THL}$  | 5.0<br>10<br>15 | –<br>–<br>–       | 100<br>50<br>40      | 200<br>100<br>80  | ns   |
| Propagation Delay Time<br>Data to Output Q                                                                                                                                                                                 | $t_{PHL},$<br>$t_{PLH}$  | 5.0<br>10<br>15 | –<br>–<br>–       | 200<br>75<br>50      | 400<br>150<br>100 | ns   |
| Write Disable to Output Q                                                                                                                                                                                                  |                          | 5.0<br>10<br>15 | –<br>–<br>–       | 200<br>80<br>60      | 400<br>160<br>120 | ns   |
| Reset to Output Q                                                                                                                                                                                                          |                          | 5.0<br>10<br>15 | –<br>–<br>–       | 175<br>80<br>65      | 350<br>160<br>130 | ns   |
| CE to Output Q (MC14599B only)                                                                                                                                                                                             |                          | 5.0<br>10<br>15 | –<br>–<br>–       | 225<br>100<br>75     | 450<br>200<br>150 | ns   |
| Propagation Delay Time, MC14599B only<br>Chip Enable, Write/Read to Data                                                                                                                                                   | $t_{PHL},$<br>$t_{PLH}$  | 5.0<br>10<br>15 | –<br>–<br>–       | 200<br>80<br>65      | 400<br>160<br>130 | ns   |
| Address to Data                                                                                                                                                                                                            |                          | 5.0<br>10<br>15 | –<br>–<br>–       | 200<br>90<br>75      | 400<br>180<br>150 | ns   |
| Pulse Widths<br>Reset                                                                                                                                                                                                      | $t_{w(H)}$<br>$t_{w(L)}$ | 5.0<br>10<br>15 | 150<br>75<br>50   | 75<br>40<br>25       | –<br>–<br>–       | ns   |
| Write Disable                                                                                                                                                                                                              |                          | 5.0<br>10<br>15 | 320<br>160<br>120 | 160<br>80<br>60      | –<br>–<br>–       | ns   |
| Set Up Time<br>Data to Write Disable                                                                                                                                                                                       | $t_{su}$                 | 5.0<br>10<br>15 | 100<br>50<br>35   | 50<br>25<br>20       | –<br>–<br>–       | ns   |
| Hold Time<br>Write Disable to Data                                                                                                                                                                                         | $t_h$                    | 5.0<br>10<br>15 | 150<br>75<br>50   | 75<br>40<br>25       | –<br>–<br>–       | ns   |
| Set Up Time<br>Address to Write Disable                                                                                                                                                                                    | $t_{su}$                 | 5.0<br>10<br>15 | 100<br>80<br>40   | 45<br>30<br>10       | –<br>–<br>–       | ns   |
| Removal Time<br>Write Disable to Address                                                                                                                                                                                   | $t_{rem}$                | 5.0<br>10<br>15 | 0<br>0<br>0       | – 80<br>– 40<br>– 40 | –<br>–<br>–       | ns   |

5. The formulas given are for the typical characteristics only at  $25^\circ\text{C}$ .

6. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

# MC14099B

## FUNCTION DIAGRAM



## TRUTH TABLE

| Write Disable | Reset | Addressed Latch | Unaddressed Latches |
|---------------|-------|-----------------|---------------------|
| 0             | 0     | Data            | $Q_n^*$             |
| 0             | 1     | Data            | Reset <sup>†</sup>  |
| 1             | 0     | $Q_n^*$         | $Q_n^*$             |
| 1             | 1     | Reset           | Reset               |

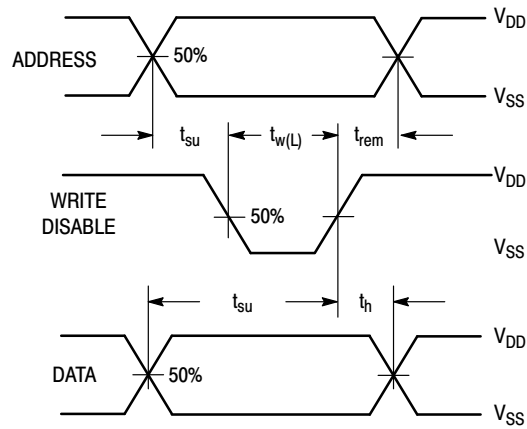
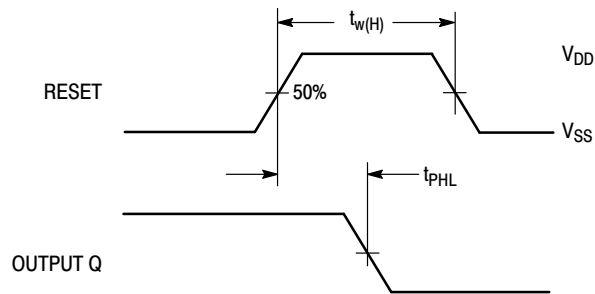
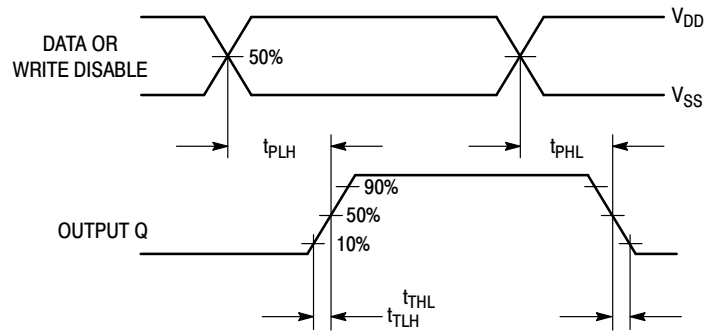
\* $Q_n$  is previous state of latch.

<sup>†</sup>Reset to zero state.

**CAUTION:** To avoid unintentional data changes in the latches, Write Disable must be active (high) during transitions on the address inputs A0, A1, and A2.

# MC14099B

## SWITCHING WAVEFORMS



## MC14099B

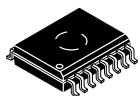
### ORDERING INFORMATION

| Device          | Package                 | Shipping <sup>†</sup>    |
|-----------------|-------------------------|--------------------------|
| MC14099BDWG     | SOIC-16 WB<br>(Pb-Free) | 47 Units / Rail          |
| MC14099BDWR2G   | SOIC-16 WB<br>(Pb-Free) | 1000 Units / Tape & Reel |
| NLV14099BDWR2G* | SOIC-16 WB<br>(Pb-Free) | 1000 Units / Tape & Reel |

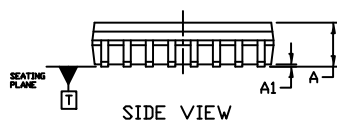
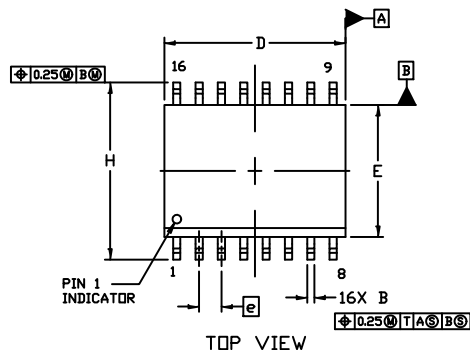
<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

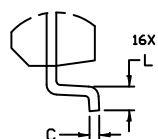
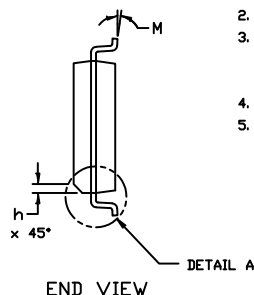


1  
SCALE 1:1



SOIC-16 WB  
CASE 751G  
ISSUE E

DATE 08 OCT 2021



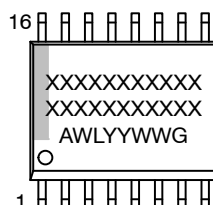
DETAIL A  
2X SCALE

## NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.  
ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION OR FLASH TO BE 0.15 PER SIDE.

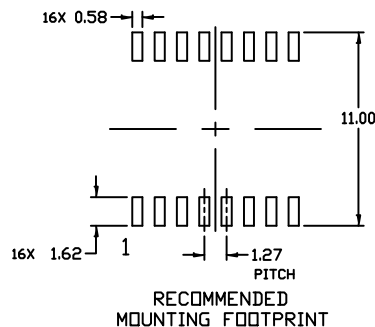
| DIM | MILLIMETERS |       |
|-----|-------------|-------|
|     | MIN.        | MAX.  |
| A   | 2.35        | 2.65  |
| A1  | 0.10        | 0.25  |
| B   | 0.35        | 0.49  |
| C   | 0.23        | 0.32  |
| D   | 10.15       | 10.45 |
| E   | 7.40        | 7.60  |
| e   | 1.27 BSC    |       |
| H   | 10.05       | 10.55 |
| h   | 0.53 REF    |       |
| L   | 0.50        | 0.90  |
| M   | 0°          | 7°    |

## GENERIC MARKING DIAGRAM\*



XXXXX = Specific Device Code  
A = Assembly Location  
WL = Wafer Lot  
YY = Year  
WW = Work Week  
G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



|                  |             |                                                                                                                                                                                     |
|------------------|-------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
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| DESCRIPTION:     | SOIC-16 WB  | PAGE 1 OF 1                                                                                                                                                                         |

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