NB672/NB673

24V, High Current Synchronous Buck Converter With +/-1.5A LDO and Buffed Reference

The Future of Analog IC Technology

DESCRIPTION

The NB672/NB673 provides a complete power supply for DDR3, DDR3L and LPDDR2 memory with the highest power density. It integrates a high frequency synchronous rectified step-down switch mode converter (VDDQ) with a 1.5A sink/source LDO (VTT) and buffered low noise reference (VTTREF).

The fully integrated Buck converter of NB672/NB673 is able to deliver 6A/8A continuous output current and 8A/10A peak output current over a wide input supply range with excellent load and line regulation. The Buck converter employs the Constant-On-Time (COT) control scheme, which provides fast transient response and eases loop stabilization.

The VTT LDO provides 1.5A sink/source current capability and requires only 10uF ceramic capacitance.

The VTTREF tracks VDDQ/2 with an excellent 1% accuracy.

Under voltage lockout is internally set as 4.5V. An open drain power good signal indicates VDDQ is within its nominal voltage range.

Full protection features include OCP, OVP, and thermal shut down.

These two parts require minimum number of external components and are available in QFN21 (3mmx4mm) package.

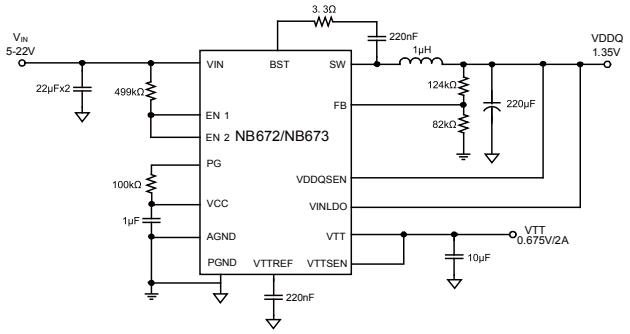
FEATURES

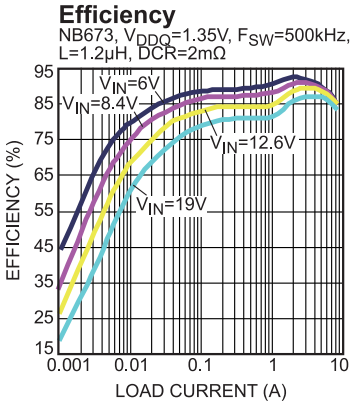
- Wide 5V to 24V Operating Input Range
- 6A Continuous Output Current and 8A Peak Output Current (NB672)
- 8A Continuous Output Current and 10A Peak Output Current (NB673)
- Built-in +/- 1.5A VTTLDO
- Low R_{DS}(ON) Internal Power MOSFETs
- Proprietary Switching Loss Reduction Technique
- Internal Soft Start
- Output Discharge
- 500kHZ Switching Frequency
- OCP, OVP, UVP Protection and Thermal Shutdown
- Latch off Reset via EN or Power Cycle.
- VDDQ Adjustable from 0.604V to 5.5V

APPLICATIONS

- Laptop Computer
- Tablet PC
- Networking Systems
- Server
- Personal Video Recorders
- Flat Panel Television and Monitors
- Distributed Power Systems

TYPICAL APPLICATION





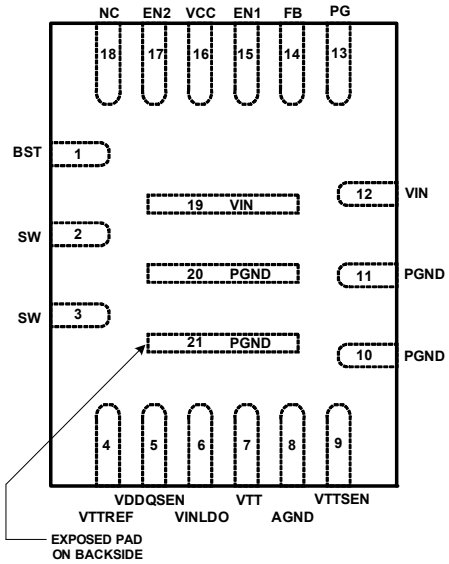
ORDERING INFORMATION

Part Number	Package	Top Marking
NB672GL*	QFN21 (3mmx4mm)	NB672
NB673GL	QFN21 (3mmx4mm)	NB673

* For Tape & Reel, add suffix –Z (e.g. NB672GL–Z)

PACKAGE REFERENCE

TOP VIEW



ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage V_{IN} 24V
V_{SW} ..... -0.3V to 24.3V
V_{SW} (30ns) ..... -3V to 28V
V_{SW} (5ns) ..... -6V to 28V
V_{BST} ..... V_{SW} + 5.5V
V_{EN} 12V
Enable Current I_{EN} (2) 2.5mA
All Other Pins ..... –0.3V to +5.5V
Continuous Power Dissipation (T_A=+25°) (3)
QFN21 ..... 2.5W
Junction Temperature ..... 150°C
Lead Temperature ..... 260°C
Storage Temperature ..... -65°C to +150°C

Recommended Operating Conditions (4)

Supply Voltage V_{IN} ..... 5V to 22V
Output Voltage V_{OUT} ..... 0.604V to 5.5V
Enable Current I_{EN} 1mA
Operating Junction Temp. (T_J). -40°C to +125°C

Thermal Resistance (5)

	θ_{JA}	θ_{JC}	
QFN21 (3mmx4mm)	50	12	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) Refer to Page 13 of Configuring the EN Control.
3) The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D(MAX)=(T_J(MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) The device is not guaranteed to function outside of its operating conditions.
5) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_J = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Supply Current						
Supply Current (Shutdown)	I_{IN}	V_{EN} = 0V		0	1	μA
Supply Current (In S0 Mode)	I_{IN}	V_{EN1} = V_{EN1} =2V, V_{FB} = 0.65V, I_{VTT} = 0A	300	400	500	μA
Supply Current (In S3 Mode)	I_{IN}	V_{EN1} = 0V, V_{EN2} = 2V, V_{FB} = 0.65V	160	190	220	μA
MOSFET						
High-side Switch On Resistance	HS_{RDS-ON}	NB672, T_J =25°C		28		mΩ
		NB673, T_J =25°C		24		
Low-side Switch On Resistance	LS_{RDS-ON}	NB672, T_J =25°C		10		mΩ
		NB673, T_J =25°C		9		
Switch Leakage	SW_{LKG}	V_{EN} = 0V, V_{SW} = 0V		0	1	μA
Current Limit						
Low-side Valley Current Limit	I_{LIMIT}	NB672	7.5	8.5	9.5	A
		NB673	8.5	9.5	10.5	A
Switching frequency and minimum off time						
Switching frequency	F_S		400	500	600	kHz
Minimum Off Time(6)	T_{OFF}		250	300	350	ns
Over-voltage and Under-voltage Protection						
OVP Threshold	V_{OVP}		125	130	135	$\%V_{REF}$
OVP Delay	T_{OVPDEL}			2.5		μs
UVP Threshold	V_{UVP}		55	60	65	$\%V_{REF}$
UVP Delay	T_{UVPDEL}			12		μs
Reference And Soft Start						
Reference Voltage	V_{REF}		598	604	610	mV
Feedback Current	I_{FB}	V_{FB} = 0.604V		10	50	nA
Soft Start Time	T_{SS}			1.6	1.95	ms
Enable And UVLO						
Enable Input Low Voltage	VIL_{EN}		1.15	1.25	1.35	V
Enable Hysteresis	V_{EN-HYS}			100		mV
Enable Input Current	I_{EN}	V_{EN} = 2V		3		μA
		V_{EN} = 0V		0		
VCC Under Voltage Lockout Threshold Rising	VCC_{Vth}			4.5	4.85	V
VCC Under Voltage Lockout Threshold Hysteresis	VCC_{HYS}			500		mV

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, T_J = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
VCC Regulator						
VCC Regulator	V_{CC}		4.8	5.1	5.3	V
VCC Load Regulation		Icc=8mA		5		%
Power Good						
FB Rising (Good)	PG_{Vth-Hi}			95		%V_{REF}
FB Falling (Fault)	PG_{Vth-Lo}			85		
FB Rising (Fault)	PG_{Vth-Hi}			115		
FB Falling (Good)	PG_{Vth-Lo}			105		
Power Good Low to High Delay	PG_{Td}			450		µs
Power Good Sink Current Capability	V_{PG}	Sink 4mA			0.4	V
Power Good Leakage Current	$I_{PG\ LEAK}$	V_{PG} = 3.3V			1	µA
VTTREF Output						
VTTREF Output Voltage	V_{TTREF}			V_{DDQSEN}/2		
Output Voltage tolerance to VDDQ		I_{VTTREF}<0.1mA, 1V<V_{DDQ}<1.4V	48.2%	50%	51.8%	
		I_{VTTREF}<10mA, 1V<V_{DDQ}<1.4V	48%	50%	52%	
Current Limit	$I_{LIMIT\ VTTREF}$		10	15		mA
VTT LDO						
VTT Output Voltage	V_{TT}			V_{TTREF}		
VTT tolerance to VTTREF		-10mA<I_{VTT}<10mA, 1V<V_{DDQ}<1.4V	-20		20	mV
		-1A<I_{VTT}<1A, 1V<V_{DDQ}<1.4V	-45		45	mV
Source Current Limit	$I_{LIMIT\ SOUCE}$			1.8		A
Sink Current Limit	$I_{LIMIT\ SINK}$			1.6		A
Thermal Protection						
Thermal Shutdown(6)	T_{SD}			150		°C
Thermal Shutdown Hysteresis				25		°C

Note:

6) Guaranteed by design.

PIN FUNCTIONS

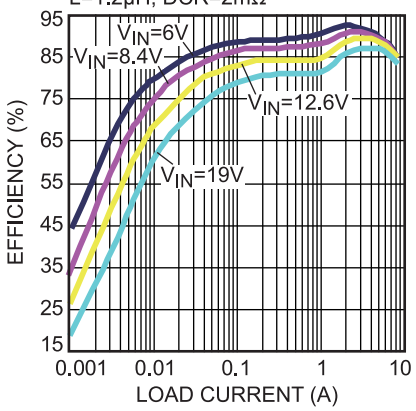
PIN #	Name	Description
1	BST	Bootstrap. A capacitor connected between SW and BST pins is required to form a floating supply across the high-side switch driver.
2, 3	SW	Switch Output. Connect this pin to the inductor and bootstrap capacitor. This pin is driven up to the VIN voltage by the high-side switch during the on-time of the PWM duty cycle. The inductor current drives the SW pin negative during the off-time. The on-resistance of the low-side switch and the internal diode fixes the negative voltage. Use wide and short PCB traces to make the connection. Try to minimize the area of the SW pattern.
4	VTTREF	Buffered VTT reference output. Decouple with a minimum 0.22µF ceramic capacitor as close to the pin as possible. X7R or X5R grade dielectric ceramic capacitors are recommended for their stable temperature characteristics.
5	VDDQSEN	Buck regulator output voltage sense. Connect this pin to the output capacitor of the regulator directly
6	VINLDO	VTT LDO regulator input. Connect VINLDO to VDDQ in typical application.
7	VTT	VTT LDO output. Decouple with a minimum 10uF ceramic capacitor as close to the pin as possible. X7R or X5R grade dielectric ceramic capacitors are recommended for their stable temperature characteristics.
8	AGND	Analog ground. The internal reference is referred to AGND. Connect the GND of the FB divider resistor to AGND for better load regulation.
9	VTTSEN	VTT output sense. Connect this pin to the output capacitor of the VTT regulator directly
10,11 Exposed Pad 20,21	PGND	Power Ground. Use wide PCB traces and multiple vias to make the connection.
12 Exposed Pad 19	VIN	Supply Voltage. The VIN pin supplies power for internal MOSFET and regulator. The NB672/NB673 operate from a +5V to +22V input rail. An input capacitor is needed to decouple the input rail. Use wide PCB traces and multiple vias to make the connection.
13	PG	Power good output, the output of this pin is an open drain signal and is high if the output voltage is higher than 95% of the nominal voltage. There is a delay from FB ≥ 95% to PG goes high.
14	FB	Feedback. An external resistor divider from the output to GND, tapped to the FB pin, sets the output voltage. Place the resistor divider as close to FB pin as possible. Avoid vias on the FB traces. It is recommend to set the current through FB resistors around 10uA.
15	EN1	Enable. EN1 and EN2 are digital inputs, which are used to enable or disable the internal regulators. Once EN1=EN2=1, the VDDQ regulator, VTT LDO and VTTREF output will be turned on; when EN1=0 and EN2=1, the VDDQ regulator and VTTREF are active while VTT LDO is off; all the regulators will be turned off when EN1=EN2=0.
16	VCC	Internal 5V LDO output. The driver and control circuits are powered from this voltage. Decouple with a minimum 1µF ceramic capacitor as close to the pin as possible. X7R or X5R grade dielectric ceramic capacitors are recommended for their stable temperature characteristics.
17	EN2	Enable. EN1 and EN2 are digital inputs, which are used to enable or disable the internal regulators. Once EN1=EN2=1, the VDDQ regulator, VTT LDO and VTTREF output will be turned on; when EN1=0 and EN2=1, the VDDQ regulator and VTTREF are active while VTT LDO is off; all the regulators will be turned off when EN1=EN2=0.
18	NC	Not connected.

TYPICAL PERFORMANCE CHARACTERISTICS

NB673, V_{IN} =20V, V_{DDQ} =1.35V, L=1.2µH, T_J=+25°C, unless otherwise noted.

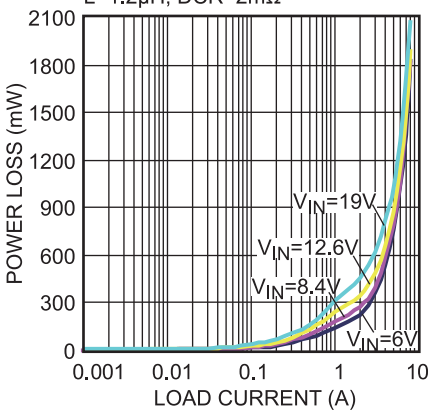
Efficiency

NB673, V_{DDQ}=1.35V, F_{SW}=500kHz, L=1.2µH, DCR=2mΩ

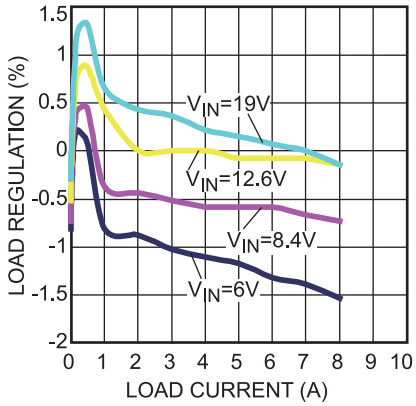


Power Loss

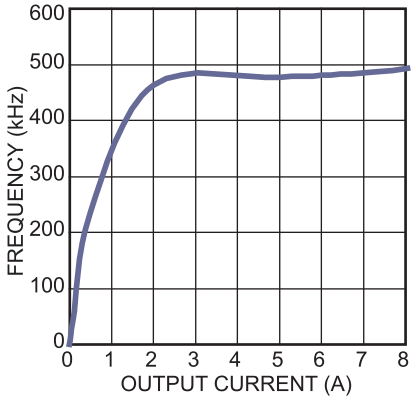
V_{DDQ}=1.35V, F_{SW}=500kHz, L=1.2µH, DCR=2mΩ



Load Regulation

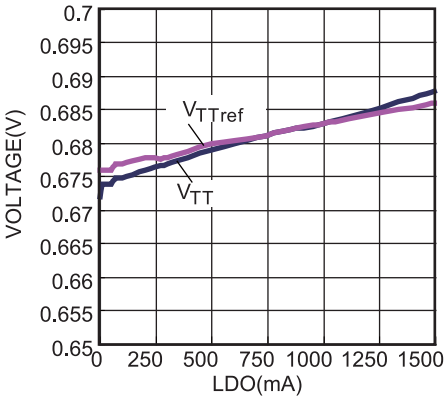


Switching Frequency vs. Output Current



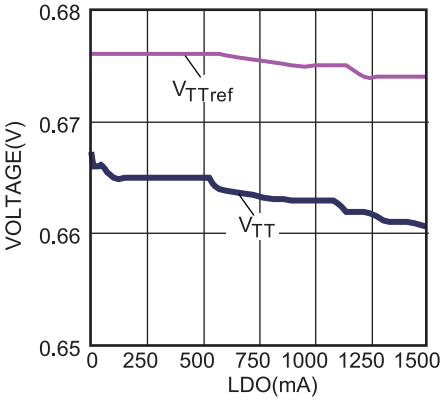
V_{TT} LDO Sink Current Load Regulation

V_{DDQ}=1.35V, V_{TT}=$V_{DDQ/2}$



V_{TT} LDO Source Current Load Regulation

V_{DDQ}=1.35V, V_{TT}=$V_{DDQ/2}$

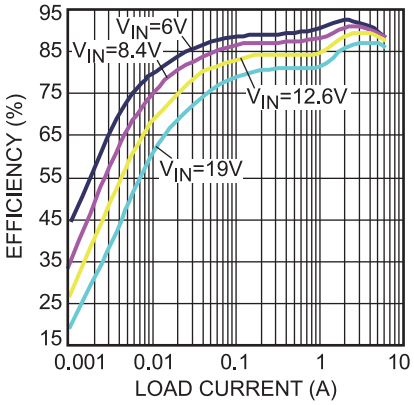


TYPICAL PERFORMANCE CHARACTERISTICS

NB672, V_{IN} =20V, V_{DDQ} =1.35V, L=1.2µH, T_J=+25°C, unless otherwise noted.

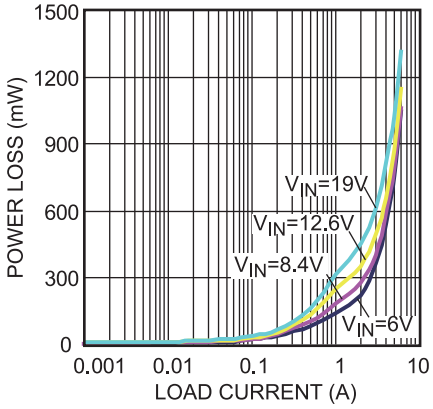
Efficiency

V_{DDQ}=1.35V, F_{SW}=500kHz, L=1.2µH, DCR=2mΩ

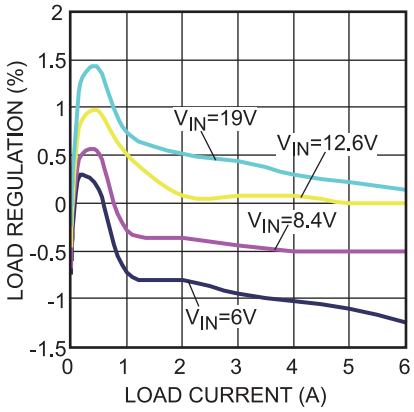


Power Loss

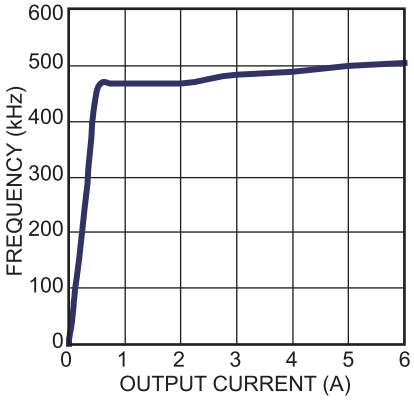
V_{DDQ}=1.35V, F_{SW}=500kHz, L=1.2µH, DCR=2mΩ



Load Regulation

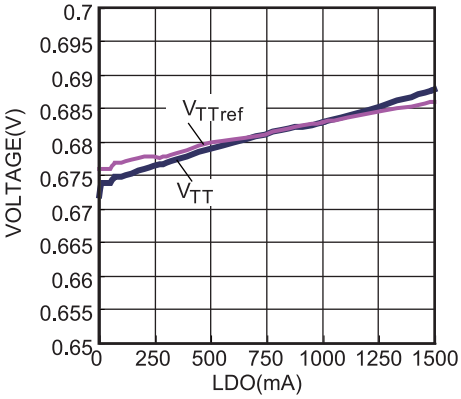


Switching Frequency vs. Output Current



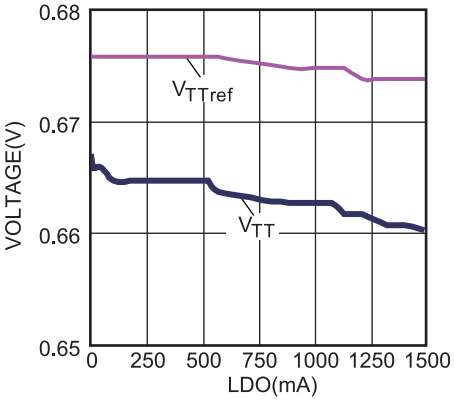
V_{TT} LDO Sink Current Load Regulation

V_{DDQ}=1.35V, V_{TT}=V_{DDQ}/2



V_{TT} LDO Source Current Load Regulation

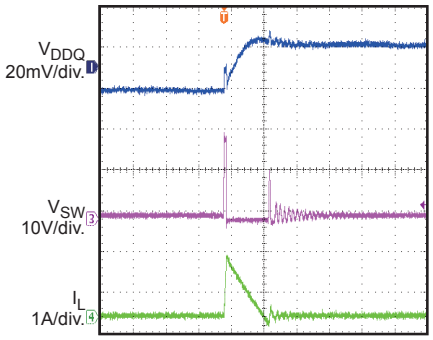
V_{DDQ}=1.35V, V_{TT}=V_{DDQ}/2



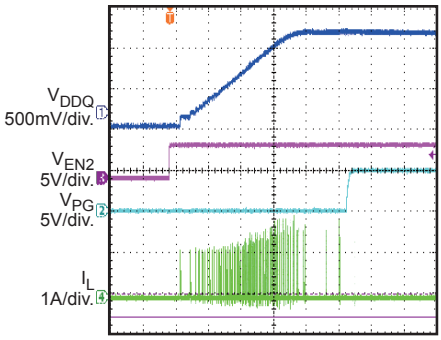
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} =20V, V_{DDQ} =1.35V, L=1.2µH, T_J=+25°C, unless otherwise noted.

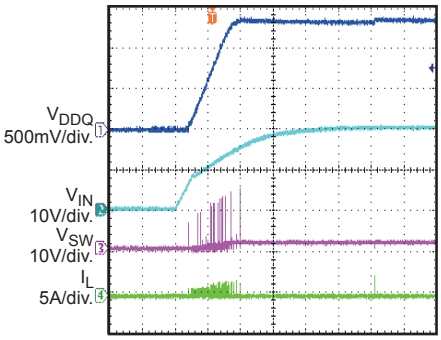
Output Voltage Ripple



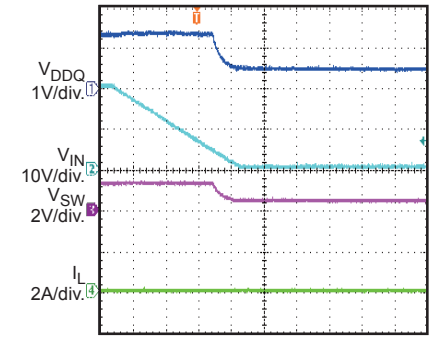
Power Good through EN Start-Up



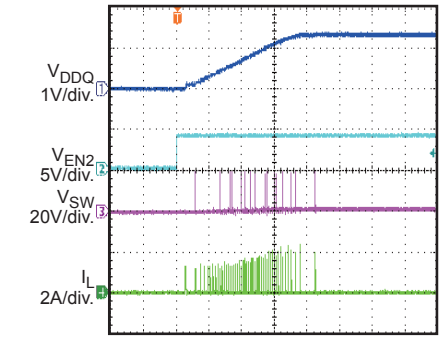
Start Up through V_{IN}



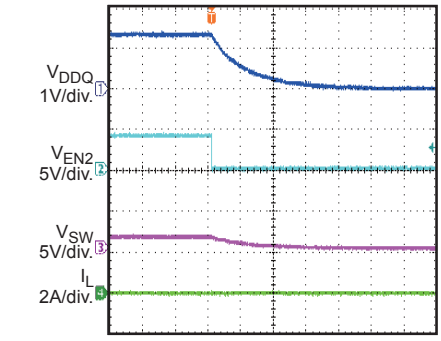
Shutdown through V_{IN}



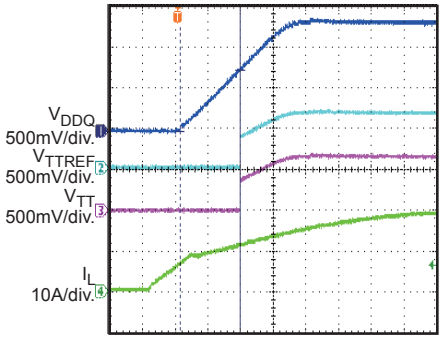
Start Up through EN



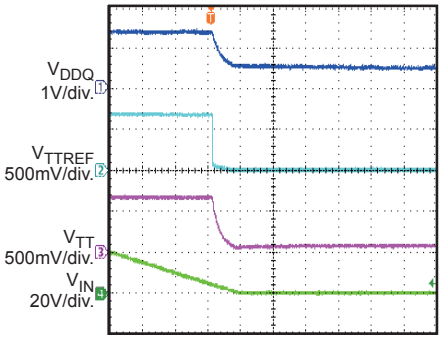
Shutdown through EN



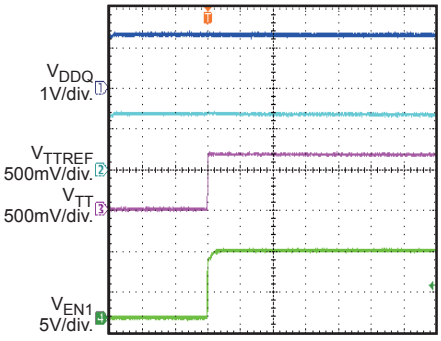
V_{TT} & V_{TTREF} Start Up through V_{IN}



V_{TT} & V_{TTREF} Shutdown through V_{IN}



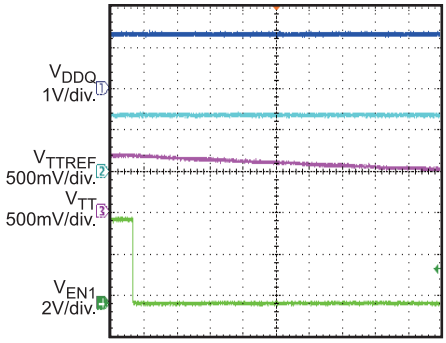
V_{TT} Start Up through EN1



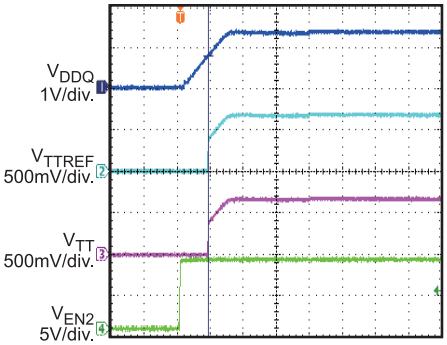
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} =20V, V_{DDQ} =1.35V, L=1.2µH, T_J=+25°C, unless otherwise noted.

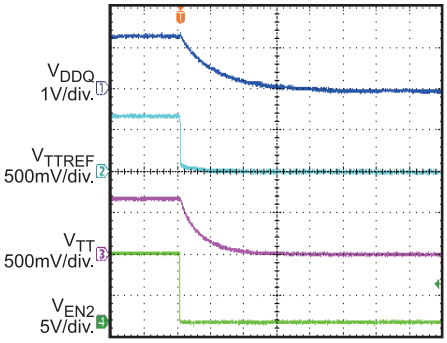
V_{TT} Shutdown through EN1



V_{TT} & V_{TTREF} Start Up through EN2

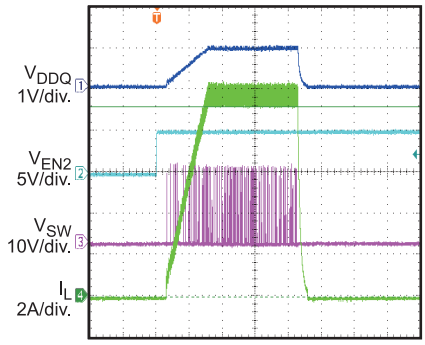


V_{TT} & V_{TTREF} Shutdown through EN2



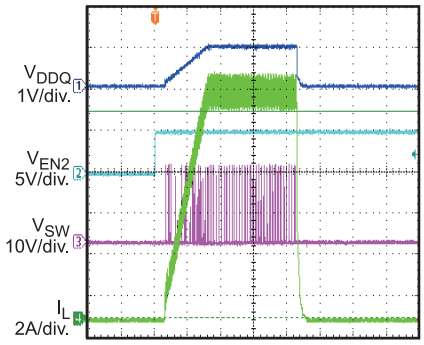
NB672 EN Short Circuit Protection

V_{IN}=19V



NB673 EN Short Circuit Protection

V_{IN}=19V



BLOCK DIAGRAM

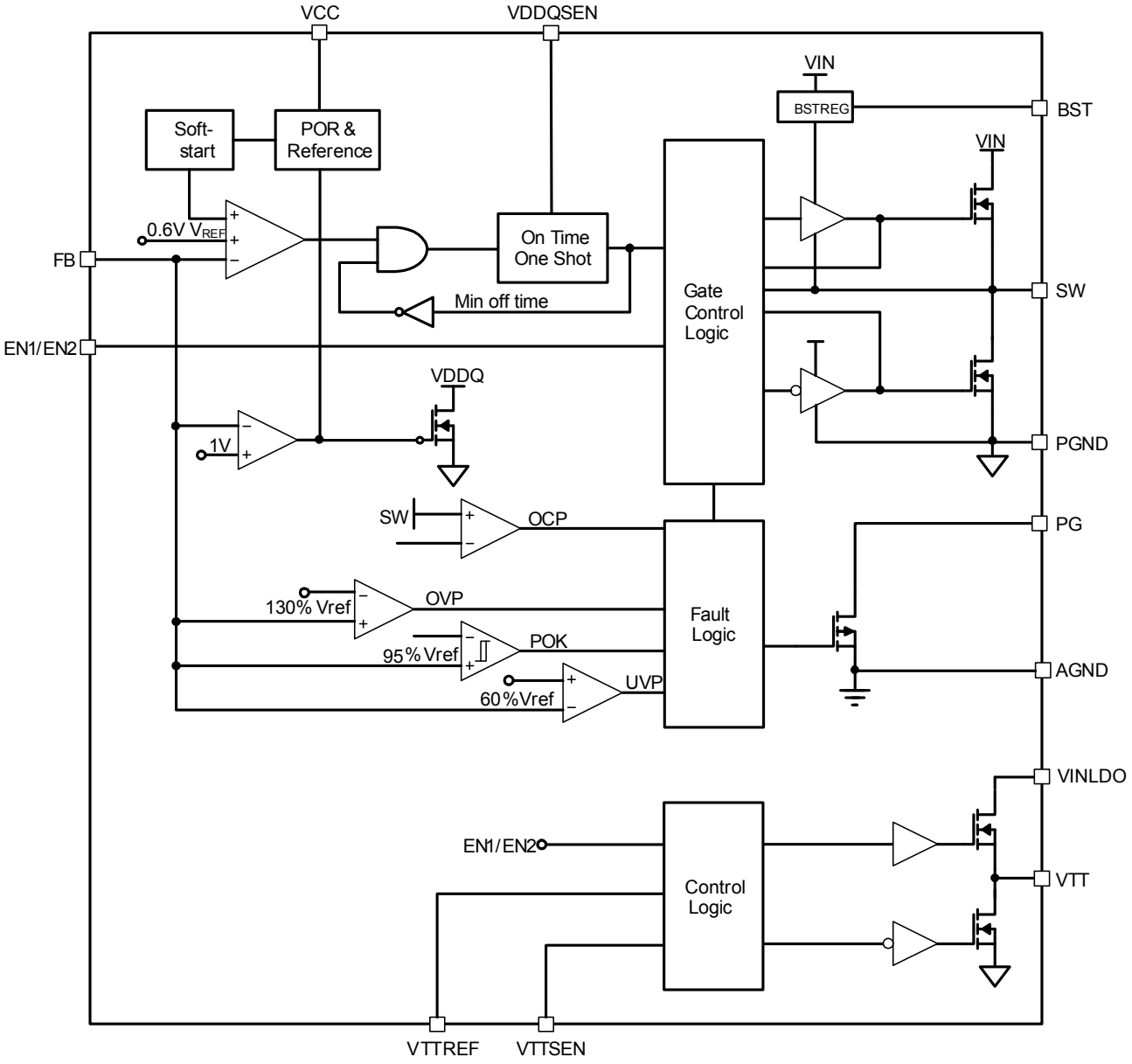


Figure 1—Functional Block Diagram

OPERATION

PWM Operation

The NB672/NB673 is fully integrated synchronous rectified step-down switch mode converter. Constant-on-time (COT) control is employed to provide fast transient response and easy loop stabilization. At the beginning of each cycle, the high-side MOSFET (HS-FET) is turned ON when the feedback voltage (V_{FB}) is below the reference voltage (V_{REF}), which indicates insufficient output voltage. The ON period is determined by both the output voltage and input voltage to make the switching frequency fairy constant over input voltage range.

After the ON period elapses, the HS-FET is turned off, or becomes OFF state. It is turned ON again when VFB drops below V_{REF}. By repeating operation this way, the converter regulates the output voltage. The integrated low-side MOSFET (LS-FET) is turned on when the HS-FET is in its OFF state to minimize the conduction loss. There will be a dead short between input and GND if both HS-FET and LS-FET are turned on at the same time. It's called shoot-through. In order to avoid shoot-through, a dead-time (DT) is internally generated between HS-FET off and LS-FET on, or LS-FET off and HS-FET on.

An internal compensation is applied for COT control to make a more stable operation even when ceramic capacitors are used as output capacitors, this internal compensation will then improve the jitter performance without affect the line or load regulation.

Heavy-Load Operation

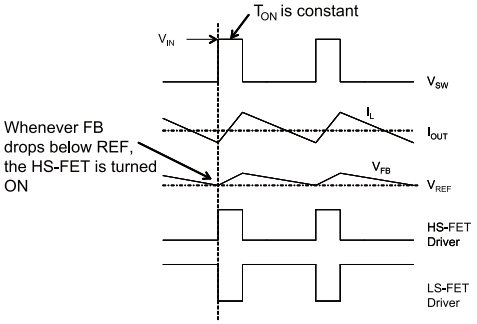


Figure 2—Heavy Load Operation

When the output current is high and the inductor current is always above zero amps, it is called continuous-conduction-mode (CCM). The CCM mode operation is shown in Figure 2 shown. When V_{FB} is below V_{REF}, HS-MOSFET is turned on for a fixed interval which is determined by one- shot on-timer as equation 1 shown. When the HS-MOSFET is turned off, the LS-MOSFET is turned on until next period.

In CCM mode operation, the switching frequency is fairly constant and it is called PWM mode.

Light-Load Operation

With the load decrease, the inductor current decrease too. Once the inductor current touch zero, the operation is transition from continuous-conduction-mode (CCM) to discontinuous-conduction-mode (DCM).

The light load operation is shown in Figure 3. When V_{FB} is below V_{REF}, HS-MOSFET is turned on for a fixed interval which is determined by one- shot on-timer as equation 1 shown. When the HS-MOSFET is turned off, the LS-MOSFET is turned on until the inductor current reaches zero. In DCM operation, the V_{FB} does not reach V_{REF} when the inductor current is approaching zero. The LS-FET driver turns into tri-state (high Z) whenever the inductor current reaches zero. A current modulator takes over the control of LS-FET and limits the inductor current to less than -1mA. Hence, the output capacitors discharge slowly to GND through LS-FET. As a result, the efficiency at light load condition is greatly improved. At light load condition, the HS-FET is not turned ON as frequently as at heavy load condition. This is called skip mode.

At light load or no load condition, the output drops very slowly and the NB672/NB673 reduces the switching frequency naturally and then high efficiency is achieved at light load.

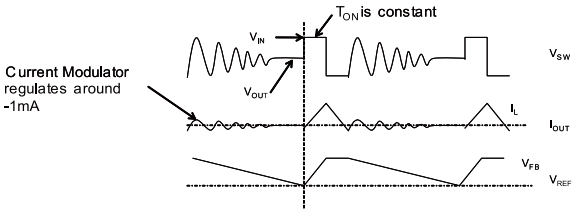


Figure 3—Light Load Operation

As the output current increases from the light load condition, the time period within which the current modulator regulates becomes shorter. The HS-FET is turned ON more frequently. Hence, the switching frequency increases correspondingly. The output current reaches the critical level when the current modulator time is zero. The critical level of the output current is determined as follows:

$$I_{OUT} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times F_S \times V_{IN}} \quad (1)$$

It turns into PWM mode once the output current exceeds the critical level. After that, the switching frequency stays fairly constant over the output current range.

Jitter and FB Ramp Slope

Jitter occurs in both PWM and skip modes when noise in the V_{FB} ripple propagates a delay to the HS-FET driver, as shown in Figures 4 and 5. Jitter can affect system stability, with noise immunity proportional to the steepness of V_{FB}'s downward slope. However, V_{FB} ripple does not directly affect noise immunity.

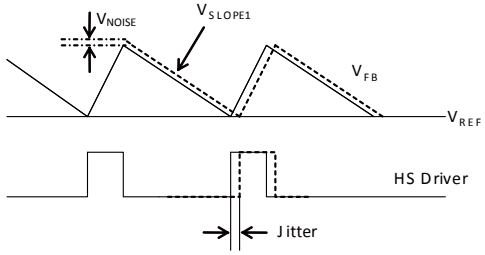


Figure 4—Jitter in PWM Mode

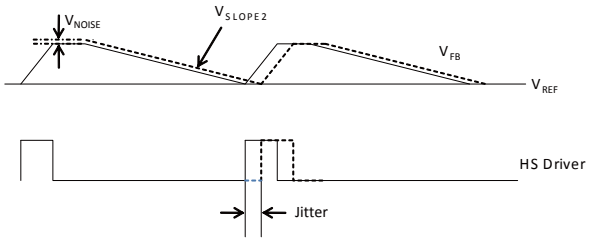


Figure 5—Jitter in Skip Mode

Operating without external ramp

The traditional constant-on-time control scheme is intrinsically unstable if output capacitor's ESR is not large enough as an effective current-sense resistor. Ceramic capacitors usually can not be used as output capacitor.

To realize the stability, the ESR value should be chosen as follow:

$$R_{ESR} \geq \frac{\frac{T_{SW}}{0.7 \times \pi} + \frac{T_{ON}}{2}}{C_{OUT}} \quad (2)$$

T_{SW} is the switching period.

The NB672/NB673 has built in internal ramp compensation to make sure the system is stable even without the help of output capacitor's ESR; and thus the pure ceramic capacitor solution can be applicant. The pure ceramic capacitor solution can significantly reduce the output ripple, total BOM cost and the board area.

Figure 6 shows a typical output circuit in PWM mode without an external ramp circuit. Turn to application information section for design steps without external compensation.

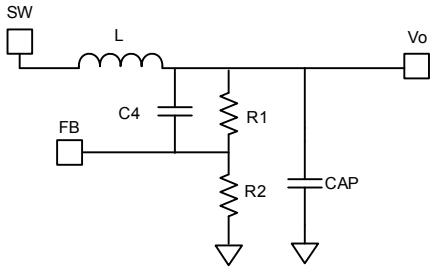


Figure 6—Simplified Circuit in PWM Mode without External Ramp Compensation

When using a large-ESR capacitor on the output, add a ceramic capacitor with a value of 10uF or less to in parallel to minimize the effect of ESL.

Operating with external ramp compensation

The NB672/NB673 is usually able to support ceramic output capacitors without external ramp, however, in some of the cases, the internal ramp may not be enough to stabilize the system, and external ramp compensation is needed. Skip to application information section for design steps with external ramp compensation.

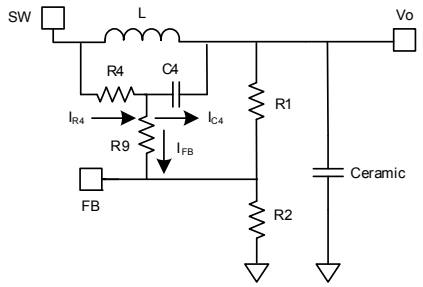


Figure 7—Simplified Circuit in PWM Mode with External Ramp Compensation

Figure 7 shows a simplified external ramp compensation (R4 and C4) for PWM mode, with HS-FET off. Chose R1, R2, R9 and C4 of the external ramp to meet the following condition:

$$\frac{1}{2\pi \times F_{SW} \times C_4} < \frac{1}{5} \times \left(\frac{R_1 \times R_2}{R_1 + R_2} + R_9 \right) \quad (3)$$

Where:

$$I_{R4} = I_{C4} + I_{FB} \approx I_{C4} \quad (4)$$

And the Vramp on the V_{FB} can then be estimated as:

$$V_{RAMP} = \frac{V_{IN} - V_{OUT}}{R_4 \times C_4} \times T_{ON} \times \frac{R_1 // R_2}{R_1 // R_2 + R_9} \quad (5)$$

The downward slope of the V_{FB} ripple then follows

$$V_{SLOPE1} = \frac{-V_{RAMP}}{T_{off}} = \frac{-V_{OUT}}{R_4 \times C_4} \quad (6)$$

As can be seen from equation 6, if there is instability in PWM mode, we can reduce either R4 or C4. If C4 can not be reduced further due to limitation from equation 3, then we can only reduce R4. For a stable PWM operation, the V_{slope1} should be design follow equation 7.

$$-V_{slope1} \geq \frac{\frac{T_{SW}}{0.7 \times \pi} + \frac{T_{ON}}{2} - R_{ESR} C_{OUT}}{2 \times L \times C_{OUT}} V_{OUT} + \frac{Io \times 10^{-3}}{T_{SW} - T_{on}} \quad (7)$$

Io is the load current.

In skip mode, the downward slope of the V_{FB} ripple is the same whether the external ramp is used or not. Figure 8 shows the simplified circuit of the skip mode when both the HS-FET and LS-FET are off.

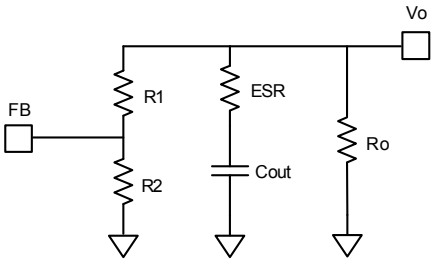


Figure 8—Simplified Circuit in skip Mode

The downward slope of the V_{FB} ripple in skip mode can be determined as follow:

$$V_{SLOPE2} = \frac{-V_{REF}}{((R_1 + R_2) // Ro) \times C_{OUT}} \quad (8)$$

Where Ro is the equivalent load resistor.

As described in Figure 5, V_{SLOPE2} in the skip mode is lower than that is in the PWM mode, so it is reasonable that the jitter in the skip mode is larger. If one wants a system with less jitter during light load condition, the values of the V_{FB} resistors should not be too big, however, that will decrease the light load efficiency.

When using a large-ESR capacitor on the output, add a ceramic capacitor with a value of 10uF or less to in parallel to minimize the effect of ESL.

Configuring the EN Control

The NB672/NB673 has two enable pins to control the on/off of the internal regulators. All of VDDQ, VTTREF and VTT are turned on at S0 state (EN1=EN2=high). In S3 mode (EN1=low, EN2=high), VDDQ and VTTREF voltages are kept on while VTT is turned off and left at high impedance state (high-Z). The VTT output floats and doesn't sink/source current in this state. In S4/S5 mode (EN1=EN2=low), all of the regulators are kept off and discharged to GND.

Table 1—EN1/EN2 Control

State	EN1	EN2	VDDQ	VTTREF	VTT
S0	High	High	ON	ON	ON
S3	Low	High	ON	ON	OFF(High-Z)
S4/S5	Low	Low	OFF	OFF	OFF
Others	High	Low	OFF	OFF	OFF

For automatic start-up the EN pin can be pulled up to input voltage through a resistive voltage divider. Choose the values of the pull-up resistor (R_{UP} from Vin pin to EN pin) and the pull-down

resistor (R_{DOWN} from EN pin to GND) to determine the automatic start-up voltage:

$$V_{IN-START} = 1.25 \times \frac{R_{UP} + R_{DOWN}}{R_{DOWN}} (V) \quad (9)$$

For example, for R_{UP}=150kΩ and R_{DOWN}=51kΩ, the $V_{IN-START}$ is set at 4.93V.

To avoid noise, a 10nF ceramic capacitor from EN to GND is recommended.

There is an internal Zener diode on the EN pin, which clamps the EN pin voltage to prevent it from running away. The maximum pull up current assuming a worst case 12V internal Zener clamp should be less than 1mA.

Therefore, when EN is driven by an external logic signal, the EN voltage should be lower than 12V.when EN is connected with VIN through a pull-up resistor or a resistive voltage divider, the resistance selection should ensure the maximum pull up current less than 1mA.

If using a resistive voltage divider and VIN higher than 12V, the allowed minimum pull-up resistor R_{UP} should meet the following equation:

$$\frac{V_{IN}(V) - 12}{R_{UP}(k\Omega)} - \frac{12}{R_{DOWN}(k\Omega)} < 1(mA) \quad (10)$$

Especially, just using the pull-up resistor R_{UP} (the pull-down resistor is not connected), the $V_{IN-START}$ is determined by input UVLO, and the minimum resistor value is:

$$R_{UP}(k\Omega) > \frac{V_{IN}(V) - 12}{1(mA)} \quad (11)$$

A typical pull-up resistor is 100kΩ.

Soft Start

The NB672/NB673 employs soft start (SS) mechanism to ensure smooth output during power-up. When the EN pin becomes high, the internal reference voltage ramps up gradually; hence, the output voltage ramps up smoothly, as well. Once the reference voltage reaches the target value, the soft start finishes and it enters into steady state operation.

If the output is pre-biased to a certain voltage during startup, the IC will disable the switching of both high-side and low-side switches until the voltage on the internal reference exceeds the sensed output voltage at the FB node.

VTT and VTTREF

This part integrates two high performance, low-drop-out linear regulators, VTT and VTTREF, to provide complete DDR3/DDR3L power solutions. The VTTREF has a 10-mA sink/source current capability, and track 1/2 of VDDQSEN using an on-chip divider. A minimum 0.22μF ceramic capacitor must be connected close to the VTTREF terminal for stable operation.

The VTT regulator responses quickly to track VTTREF with +/-45mV under all conditions. The current capability of the VTT regulator is up to 1.5A for both sink and source modes. A minimum 10μF ceramic capacitor need to be connected close to the VTT terminal. The VTTSEN should be connected to the positive node of VTT output capacitor as a separated trace from the high-current line to the VTT pin.

VDDQ Power Good (PG)

The NB672/NB673 has power-good (PGOOD) output used to indicate whether the output voltage of the VDDQ regulator is ready or not. The PGOOD pin is the open drain of a MOSFET. It should be connected to V_{CC} or other voltage source through a resistor (e.g. 100k,). After the input voltage is applied, the MOSFET is turned on so that the PGOOD pin is pulled to GND before SS is ready. After FB voltage reaches 95% of REF voltage, the PGOOD pin is pulled high after a delay. The PGOOD delay time is 1ms.

When the FB voltage drops to 85% of REF voltage, the PGOOD pin will be pulled low.

VDDQ Over Current Protection

NB672/NB673 has cycle-by-cycle over current limiting control. The current-limit circuit employs a "valley" current-sensing algorithm. The part use the Rds(on) of the low side MOSFET as a current-sensing element. If the magnitude of the current-sense signal is above the current-limit threshold, the PWM is not allowed to initiate a new cycle.

The trip level is fixed internally. The inductor current is monitored by the voltage between GND

pin and SW pin. GND is used as the positive current sensing node so that GND should be connected to the source terminal of the bottom MOSFET.

Since the comparison is done during the high side MOSFET OFF and low side MOSFET ON state, the OC trip level sets the valley level of the inductor current. Thus, the load current at over-current threshold, IOC, can be calculated as follows:

$$I_{OC} = I\_limit + \frac{\Delta I_{inductor}}{2} \quad (13)$$

In an over-current condition, the current to the load exceeds the current to the output capacitor; thus the output voltage tends to fall off. Eventually, it will end up with crossing the under voltage protection threshold and shutdown. And fault latching can be reset by EN going low or Power-cycling of VIN.

VTT Over-Current Protection

The VTT LDO has an internally fixed current limit of 1.8A for source operation, and 1.6A for sink.

VDDQ Over/Under-Voltage Protection (OVP/UVP)

NB672/NB673 monitors a resistor divided feedback voltage to detect over and under voltage. When the feedback voltage becomes higher than 115% of the target voltage, the controller will enter Dynamic Regulation Period. During this period, the LS will off when the LS current goes to -1A, this will then discharge the output and try to keep it within the normal range. If the dynamic regulation can not limit the increasing of the Vo, once the feedback voltage becomes higher than 130% of the feedback voltage, the OVP comparator output goes high and the circuit latches as the high-side MOSFET driver OFF and the low-side MOSFET turn on acting as an -1A current source.

When the feedback voltage becomes lower than 60% of the target voltage, the UVP comparator output goes high if the UV still occurs after 26us delay; then the fault latch will be triggered---latches HS off and LS on; the LS FET keeps on until the inductor current goes zero. Also fault latching can be reset by EN going low or Power-cycling of VIN.

UVLO Protection

The NB672/NB673 has under-voltage lock-out protection (UVLO). When the VCC voltage is higher than the UVLO rising threshold voltage, the part will be powered up. It shuts off when the VIN voltage is lower than the UVLO falling threshold voltage. This is non-latch protection. The part is disabled when the VCC voltage falls below 4.5V. Besides fault latching can be reset by EN going low or Power-cycling of VIN. If an application requires a higher under-voltage lockout (UVLO), use the EN pin as shown in Figure 9 to adjust the input voltage UVLO by using two external resistors. It is recommended to use the enable resistors to set the UVLO falling threshold (VSTOP) above 4.5V. The rising threshold (VSTART) should be set to provide enough hysteresis to allow for any input supply variations.

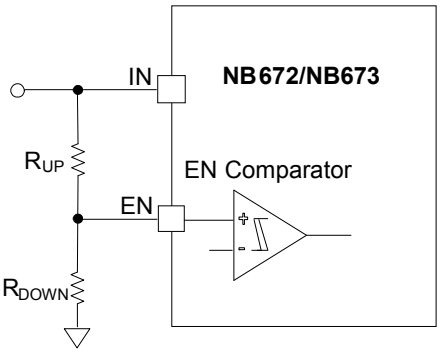


Figure 9—Adjustable UVLO

Thermal Shutdown

Thermal shutdown is employed in the NB672/NB673. The junction temperature of the IC is internally monitored. If the junction temperature exceeds the threshold value (typical 150ºC), the converter shuts off. This is a non-latch protection. There is about 25ºC hysteresis. Once the junction temperature drops to about 125ºC, it initiates a SS.

Output Discharge

NB672/NB673 discharges all the outputs, including VDDQ, VTTREF and VTT when EN2=low, or the controller is turned off by the protection functions (UVP & OCP, OCP, OVP, UVLO, and thermal shutdown). The part discharge the outputs using an internal 6Ω MOSFET.

APPLICATION INFORMATION

Setting the Output Voltage---without external compensation

The NB672/NB673 can usually support different type of output capacitors, including POSCAP, electrolytic capacitor and also ceramic capacitors without external ramp compensation, The output voltage is then set by feedback resistors R1 and R2. As Figure 10 shows.

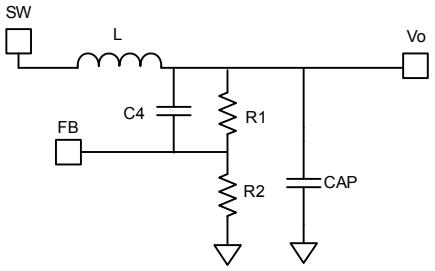


Figure10—Simplified Circuit of POS Capacitor

First, choose a value for R2. R2 should be chosen reasonably, a small R2 will lead to considerable quiescent current loss while too large R2 makes the FB noise sensitive. Typically, set the current through R2 at around 5-10uA will make a good balance between system stability and also the no load loss. Then R1 is determined as follow with the output ripple considered:

$$R_1 = \frac{V_{OUT} - \frac{1}{2}\Delta V_{OUT} - V_{REF}}{V_{REF}} \cdot R_2 \quad (13)$$

ΔV_{OUT} is the output ripple, refer to equation (23)

Other than feedback resistors, a feed forward cap C4 is usually applied for a better transient performance, especially when ceramic caps are applied for their small capacitance, a cap value around 100pF-1nF is suggested for a better transient while also keep the system stable with enough noise immunity. In case the system is noise sensitive because of the zero induced by this cap, add a resistor-usually named as R9 between this cap and FB to form a pole, this resistor can be set according to equation (16) as in the following section.

Setting the Output Voltage —with external compensation

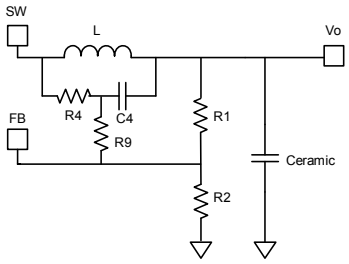


Figure11—Simplified Circuit of Ceramic Capacitor

If the system is not stable enough when low ESR ceramic capacitor is used in the output, an external voltage ramp should be added to FB through resistor R4 and capacitor C4.

The output voltage is influenced by ramp voltage V_{RAMP} besides R divider as shown in Figure 11. The V_{RAMP} can be calculated as shown in equation 7. R2 should be chosen reasonably, a small R2 will lead to considerable quiescent current loss while too large R2 makes the FB noise sensitive. It is recommended to choose a value within 5kΩ-50kΩ for R2, using a comparatively larger R2 when Vo is low, etc., 1.05V, and a smaller R2 when Vo is high. And the value of R1 then is determined as follow:

$$R_1 = \frac{R_2}{\frac{V_{FB(AVG)}}{(V_{OUT} - V_{FB(AVG)})} - \frac{R_2}{R_4 + R_9}} \quad (14)$$

The $V_{FB(AVG)}$ is the average value on the FB, $V_{FB(AVG)}$ varies with the Vin, Vo, and load condition, etc., its value on the skip mode would be lower than that of the PWM mode, which means the load regulation is strictly related to the $V_{FB(AVG)}$. Also the line regulation is related to the $V_{FB(AVG)}$. If one wants to gets a better load or line regulation, a lower Vramp is suggested, as long as the criterion shown in equation 8 can be met.

For PWM operation, $V_{FB(AVG)}$ value can be deduced from the equation below.

$$V_{FB(AVG)} = V_{REF} + \frac{1}{2} V_{RAMP} \times \frac{R_1 // R_2}{R_1 // R_2 + R_9} \quad (15)$$

Usually, R9 is set to 0Ω, and it can also be set following equation 16 for a better noise immunity. It should also set to be 5 times smaller than R1//R2 to minimize its influence on Vramp.

$$R_9 = \frac{1}{2\pi \times C_4 \times 2F_{SW}} \quad (16)$$

Using equation 14 to calculate the R1 can be complicated. To simplify the calculation, a DC-blocking capacitor Cdc can be added to filter the DC influence from R4 and R9. Figure 12 shows a simplified circuit with external ramp compensation and a DC-blocking capacitor. With this capacitor, R1 can easily be obtained by using the simplified equation for PWM mode operation:

$$R_1 = \frac{(V_{OUT} - V_{REF} - \frac{1}{2}V_{RAMP})}{V_{REF} + \frac{1}{2}V_{RAMP}} R_2 \quad (17)$$

Cdc is suggested to be at least 10 times larger than C4 for better DC blocking performance, and should also not larger than 0.47uF considering start up performance. In case one wants to use larger Cdc for a better FB noise immunity, combined with reduced R1 and R2 to limit the Cdc in a reasonable value without affecting the system start up. Be noted that even when the Cdc is applied, the load and line regulation are still Vramp related.

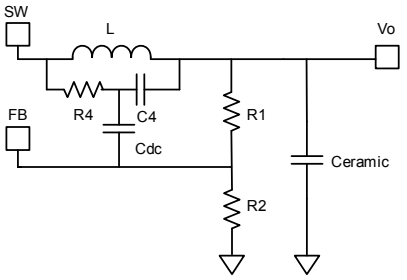


Figure12—Simplified Circuit of Ceramic Capacitor with DC blocking capacitor

Input Capacitor

The input current to the step-down converter is discontinuous and therefore requires a capacitor to supply the AC current to the step-down converter while maintaining the DC input voltage. Ceramic capacitors are recommended for best performance and should be placed as close to the V_{IN} pin as possible. Capacitors with X5R and X7R ceramic dielectrics are recommended because they are fairly stable with temperature fluctuations.

The capacitors must also have a ripple current rating greater than the maximum input ripple current of the converter. The input ripple current can be estimated as follows:

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (18)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, where:

$$I_{CIN} = \frac{I_{OUT}}{2} \quad (19)$$

For simplification, choose the input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitance value determines the input voltage ripple of the converter. If there is an input voltage ripple requirement in the system, choose the input capacitor that meets the specification.

The input voltage ripple can be estimated as follows:

$$\Delta V_{IN} = \frac{I_{OUT}}{F_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (20)$$

Under worst-case conditions where $V_{IN} = 2V_{OUT}$:

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{F_{SW} \times C_{IN}} \quad (21)$$

Output Capacitor

The output capacitor is required to maintain the DC output voltage. Ceramic or POSCAP capacitors are recommended. The output voltage ripple can be estimated as:

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times F_{SW} \times C_{OUT}}) \quad (22)$$

In the case of ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly caused by the capacitance. For simplification, the output voltage ripple can be estimated as:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times F_{SW}^{2} \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (23)$$

The output voltage ripple caused by ESR is very small. Therefore, an external ramp is needed to stabilize the system. The external ramp can be generated through resistor R4 and capacitor C4.

In the case of POSCAP capacitors, the ESR dominates the impedance at the switching frequency. The ramp voltage generated from the ESR is high enough to stabilize the system. Therefore, an external ramp is not needed. A minimum ESR value around 12mΩ is required to ensure stable operation of the converter. For simplification, the output ripple can be approximated as:

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (24)$$

Maximum output capacitor limitation should be also considered in design application. NB672/NB673 has an around 1.6ms soft-start time period. If the output capacitor value is too high, the output voltage can't reach the design value during the soft-start time, and then it will fail to regulate. The maximum output capacitor value C_{o_max} can be limited approximately by:

$$C_{O\_MAX} = (I_{LIM\_AVG} - I_{OUT}) \times T_{ss} / V_{OUT} \quad (25)$$

Where, I_{LIM_AVG} is the average start-up current during soft-start period. T_{ss} is the soft-start time.

Inductor

The inductor is necessary to supply constant current to the output load while being driven by the switched input voltage. A larger-value inductor will result in less ripple current that will result in lower output ripple voltage. However, a larger-value inductor will have a larger physical footprint, higher series resistance, and/or lower saturation current. A good rule for determining the inductance value is to design the peak-to-peak ripple current in the inductor to be in the range of 30% to 40% of the maximum output current, and that the peak inductor current is below the maximum switch current limit. The inductance value can be calculated by:

$$L = \frac{V_{OUT}}{F_{SW} \times \Delta I_{L}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (26)$$

Where ΔI_L is the peak-to-peak inductor ripple current.

The inductor should not saturate under the maximum inductor peak current, where the peak inductor current can be calculated by:

$$I_{LP} = I_{OUT} + \frac{V_{OUT}}{2F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (27)$$

PCB Layout Guide

1. The high current paths (GND, IN, and SW) should be placed very close to the device with short, direct and wide traces.
2. Put the input capacitors as close to the IN and GND pins as possible.
3. Put the decoupling capacitor as close to the VCC and GND pins as possible. Place the Cap close to VCC if the distance is long. And place >3 Vias if via is required to reduce the leakage inductance.
4. Keep the switching node SW short and away from the feedback network.
5. The external feedback resistors should be placed next to the FB pin. Make sure that there is no via on the FB trace.
6. Keep the BST voltage path (BST, C3, and SW) as short as possible.
7. Keep the IN and GND pads connected with large copper and use at least two layers for IN and GND trace to achieve better thermal performance. Also, add several Vias with 10mil_drill/18mil_copper_width close to the IN and GND pads to help on thermal dissipation.
8. Four-layer layout is strongly recommended to achieve better thermal performance.

Note

Please refer to the PCB Layout Application Note for more details.

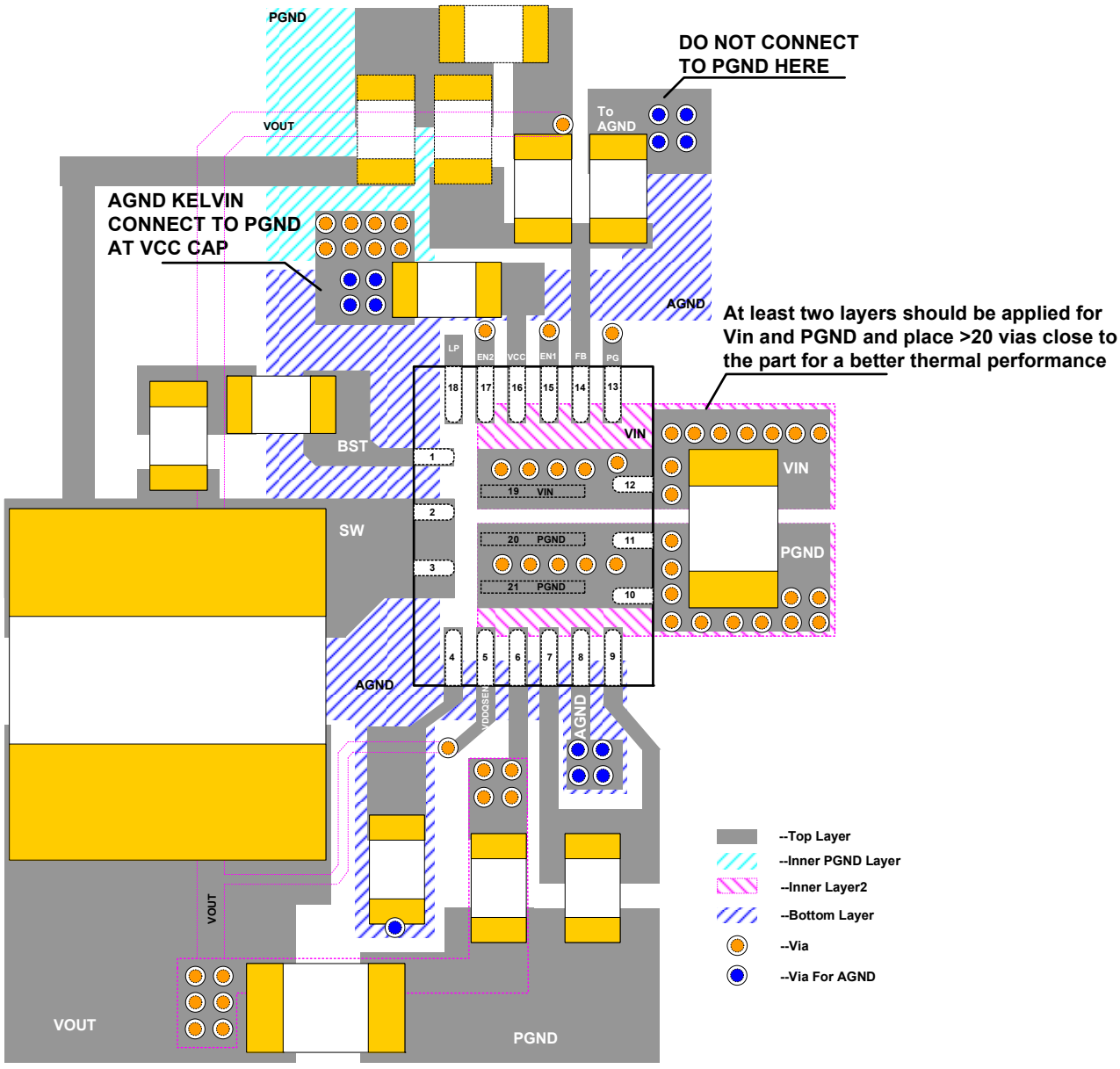


Figure 13—Recommend Layout

Recommend Design Example

Some design examples are provided below when the ceramic capacitors are applied:

Table 2—Design Example

V_{OUT} (V)	Cout (F)	L (µH)	R4 (Ω)	C4 (F)	R1 (kΩ)	R2 (kΩ)
1.05	22µx3	1.2	NS	220p	59	82
1.2	22µx3	1.2	NS	220p	100	102
1.35	22µx3	1.2	NS	220p	100	82

The detailed application schematic is shown in Figure 14 when large ESR caps are used and Figure 15 when low ESR caps are applied. The typical performance and circuit waveforms have been shown in the Typical Performance Characteristics section. For more possible applications of this device, please refer to related Evaluation Board Data Sheets.

TYPICAL APPLICATION

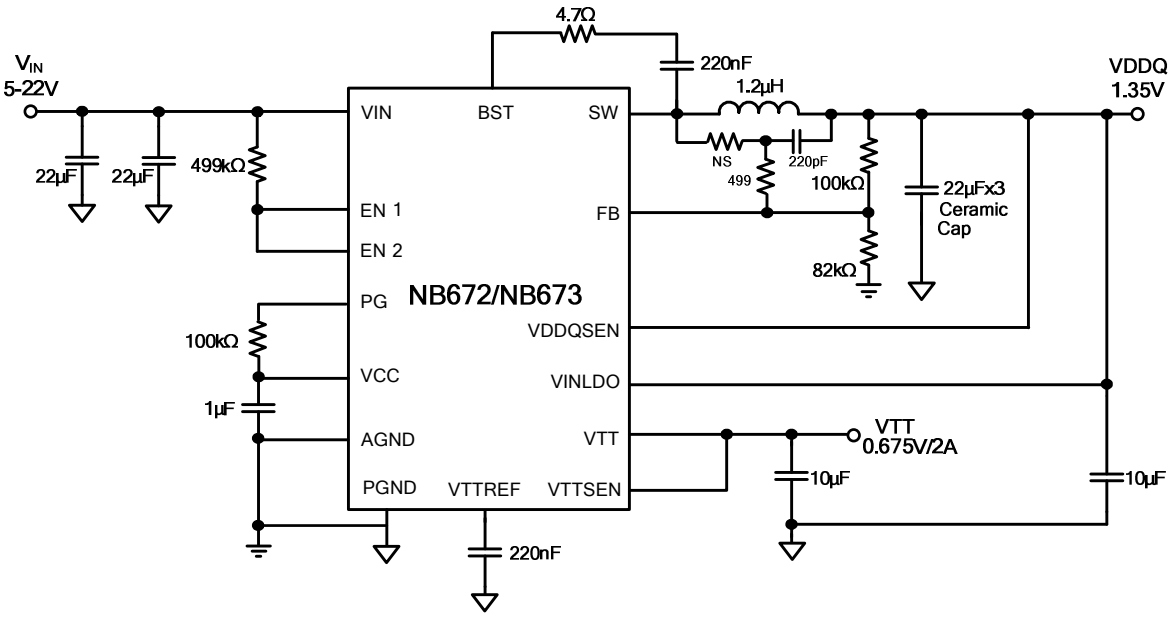


Figure 14 — Typical Application Circuit with Low ESR Ceramic Output Capacitor

V_{IN}=5-22V, V_{OUT}=1.35V

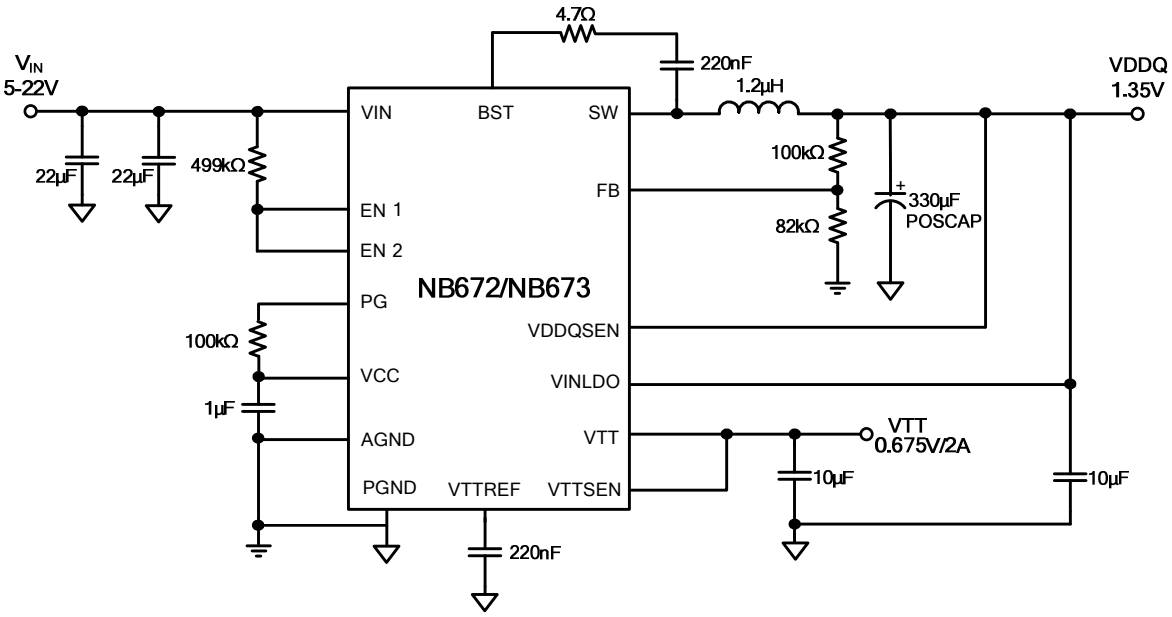


Figure 15 — Typical Application Circuit with Large ESR POSCAP Output Capacitor

V_{IN}=5-22V, V_{OUT}=1.35V

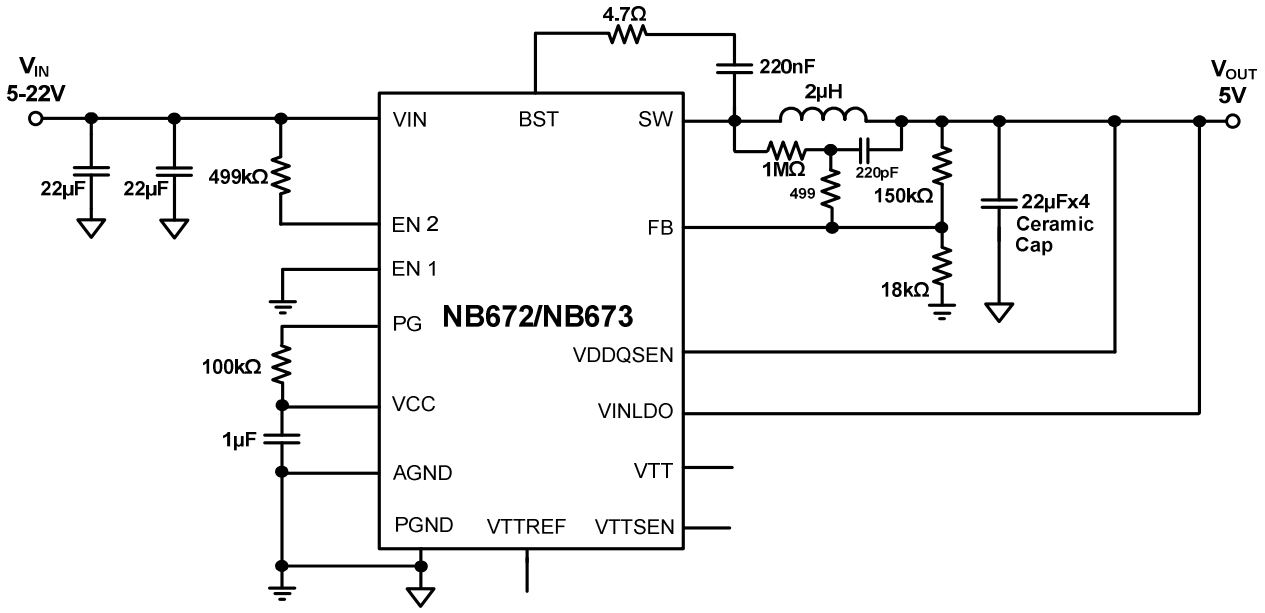
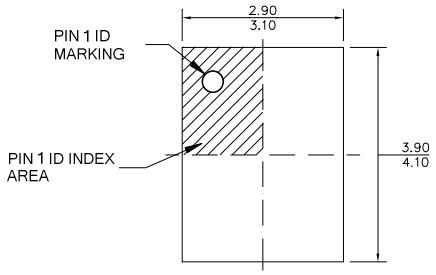


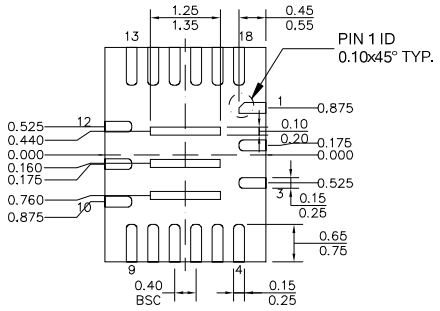
Figure 16 – Typical Application Circuit with Low ESR Ceramic Output Capacitor
V_{IN}=7-22V, V_{OUT}=5V

PACKAGE INFORMATION

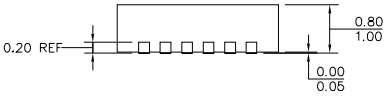
QFN21 (3mmX4mm)



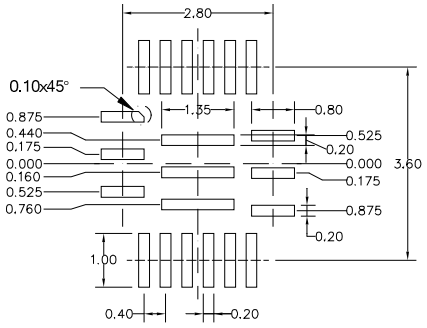
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.