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RTL8231

SMI Interface and Serial Interface control LED Display Controller

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USING THIS DOCUMENT

This document is intended for the hardware engineer's general information on the Realtek RTL8389M chips.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

REVISION HISTORY

Revision	Release Date	Summary
0.3	2009/09/28	First release.

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1. General Description

The RTL8231 is a serial data interface LED display controller that transmits:

- Serial data to parallel LED (Shift Register Mode)
- SMI data to Scan LED (SMI Mode)
- SMI data to GPIO (SMI Mode)

Shift Register Mode

In Shift Register Mode, the RTL8231 supports 36 LEDs. The RTL8231 receives serial data and serial clock, and via the shift register changes it to parallel output. The SO (Serial Out) pin outputs any serial data input that exceeds 36 bits for cascading to another RTL8231. The Reset pin clears the shift register data and the strapping pin sets the initial values when the RTL8231 is reset.

SMI Mode

In SMI Mode, the RTL8231 supports MDC/MDIO and SMI Slave bus data format. In SMI Slave mode, 8-bit and 16-bit data accesses are both supported. The MDC/MDIO or SMI Slave interface can set the address from 0 to 31 (MDC/MDIO) or from 0 to 7 (SMI Slave). The RTL8231 controls SCAN LED and GPIOs via LED and GPIO status registers.

The RTL8231 scanning single color LED supports maximal 24-port per port 3 single color LED application or 24-port per port 2 single LED for fast Ethernet and 8-port per port one bi-color, and one single color LED for Giga Ethernet application. The RTL8231 scanning bi-color LED supports maximal 24-port per port one single color and one bi-color LED application.

The RTL8231 provides 37 GPIOs. Any unused Single color or Bi-color LED pins can be switched to become a GPIO pin.

2. Feature Items

- Controlled Interface
  - Serial Interface
    - CLK_IN and SI provide clock and data to enable the internal shift register.
  - MDC/MDIO Interface
    - Supports the IEEE compliant Management Data Input/Output (MDIO) Interface
    - Slave mode MDC/MDIO.
    - Can set PHY addresses from 0 to 31 (default value: 31).
  - SMI Slave Interface
    - Supports 8-bit and 16-bit data access.
    - Can set the device ID from 0 to 7 (default value: 7).
- Functions support
  - Shift Register Mode
    - Supports 36 parallel data outputs.
    - The SO (Serial Out) pin outputs any serial data input that exceeds 36 bits (for cascading to another RTL8231).
  - Single Color Scan LED in SMI mode
    - Supports 24 ports Single Color scanning LED, each port includes 3 single-color LEDs.
    - Provides 8 bi-color LEDs for 24 FE+8G application
    - Each LED has a respective status register that is controlled by the SMI interface.
  - Bi-Color Scan LED in SMI Mode
    - Supports 24 ports Bi-color scanning LED, each port includes one bi-color and one single color LED.
    - Each LED has a respective status register that is controlled by the SMI interface.
  - GPIO in SMI Mode
    - Provides 37 GPIOs.
    - Any unused Single color or Bi-color LED pins can be switched to become a GPIO pin
    - Any GPIO can be controlled by GPI or GPO (except for 8 strapping pins)
    - Strapping pins only use GPO in GPIO applications
    - Each GPO output default driving current is 8mA (can be changed to 4mA via register setting)
    - Each GPIO has a respective status register that is controlled by the SMI interface.
  - Buzzer Single output
    - GPIO[35] can be set to Buzzer output mode.
    - The buzzer output frequency can be set to: 1.5K, 2K, 2.5K, 3K, 3.5K, 4K, 5K, and 6K square waveform.
  - Push Button De-bouncing
    - The GPIO[31]~[36] supports input de-bouncing function.

- The GPI pin can be latched only if the same input signal continues for 100ms.

- LED Output Synchronization
  - All LEDs (Single color mode 72+8 LEDs, Bi-color mode 48 LEDs) can change synchronization status via register commands
- GPIO Output Synchronization
  - All 37 GPIOs output synchronization status can be changed via register commands.
- LED Blinking Speed Change
  - Each LED blinking speed can be changed via LED status registers.
  - Each LED status register has 3-bits that control LED speed (32ms to 1024ms).

■ Chip Package

- LQFP-48 package

3. Application Examples

3.1. Serial LED Application

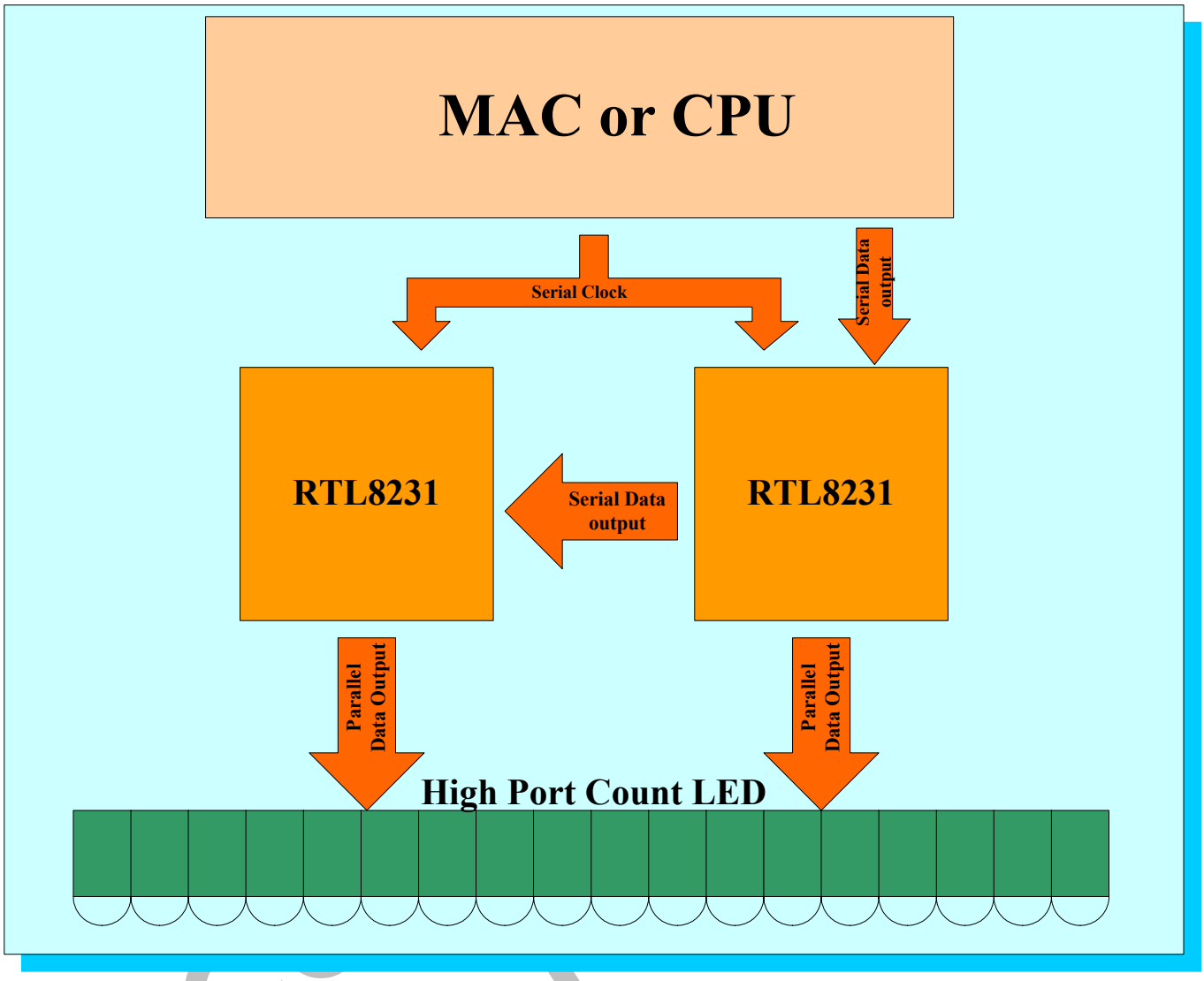


Figure 1. Serial LED Application in Shift Register Mode

3.2. Scan LED Application

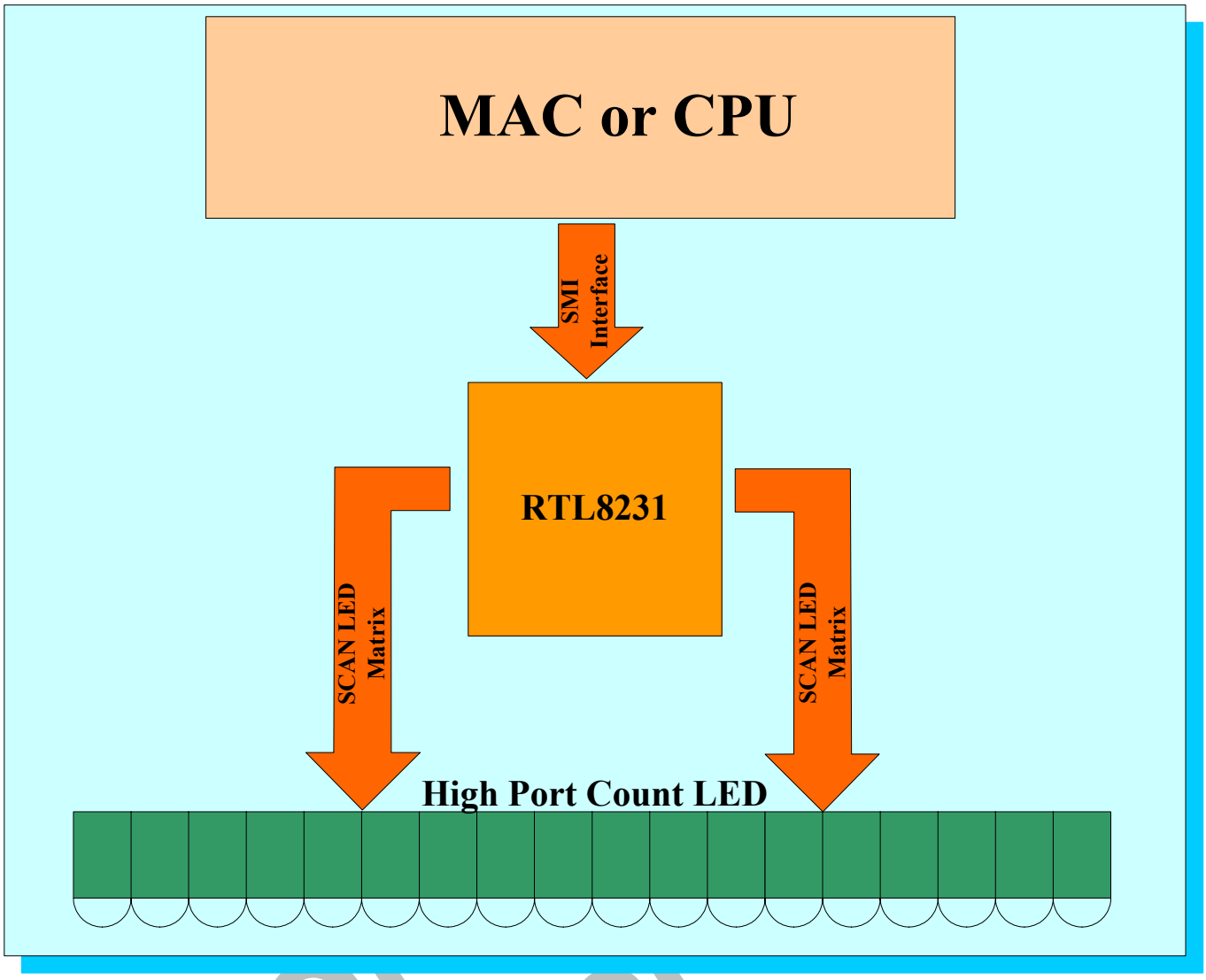


Figure 2. Scan LED in High Port Count Switch Application

3.3. Scan LED and GPIO Application

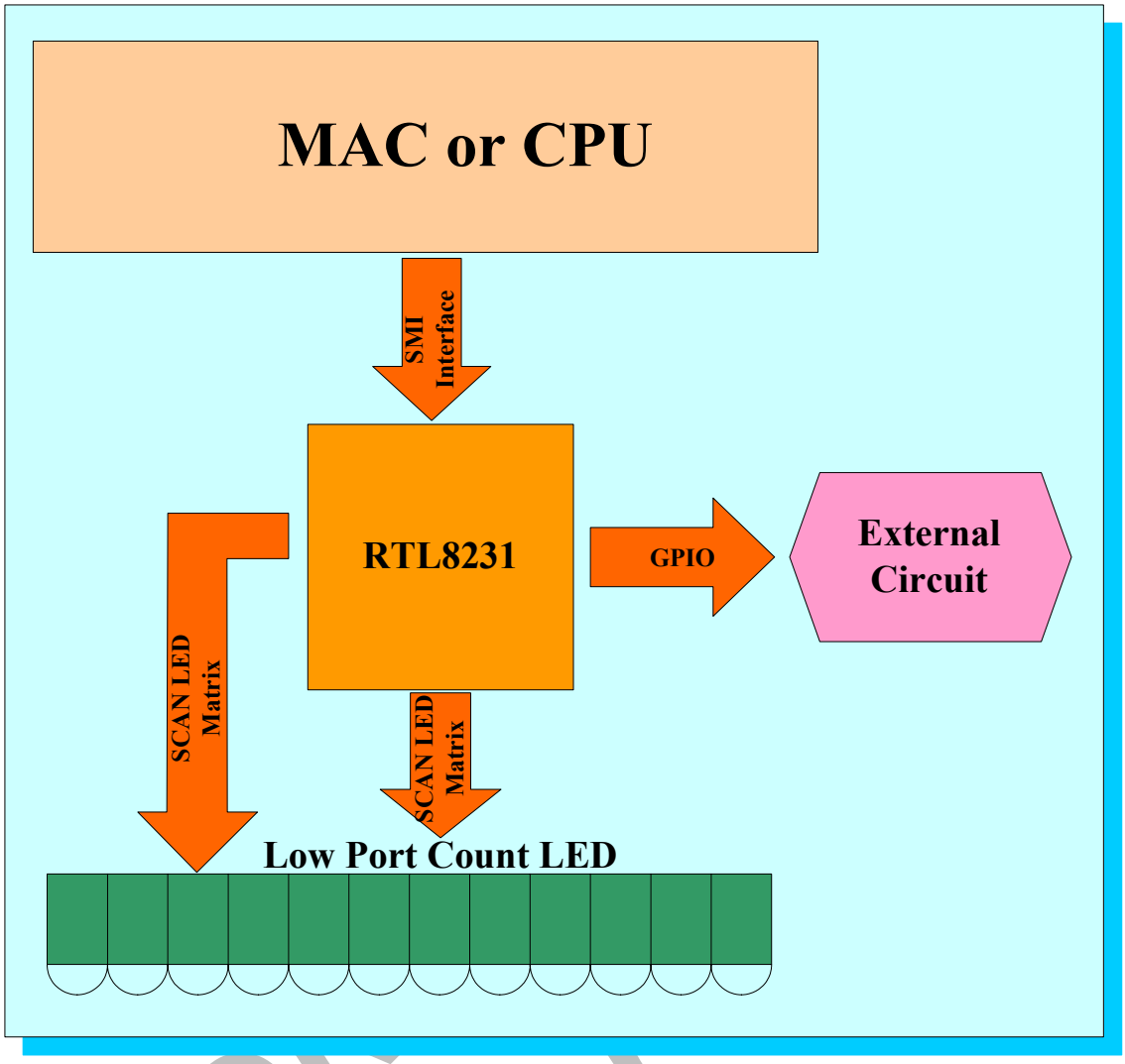


Figure 3. Scan LED and GPIO in Low Port Count Switch Application

4. Block Diagram

4.1. RTL8231 Block Diagram

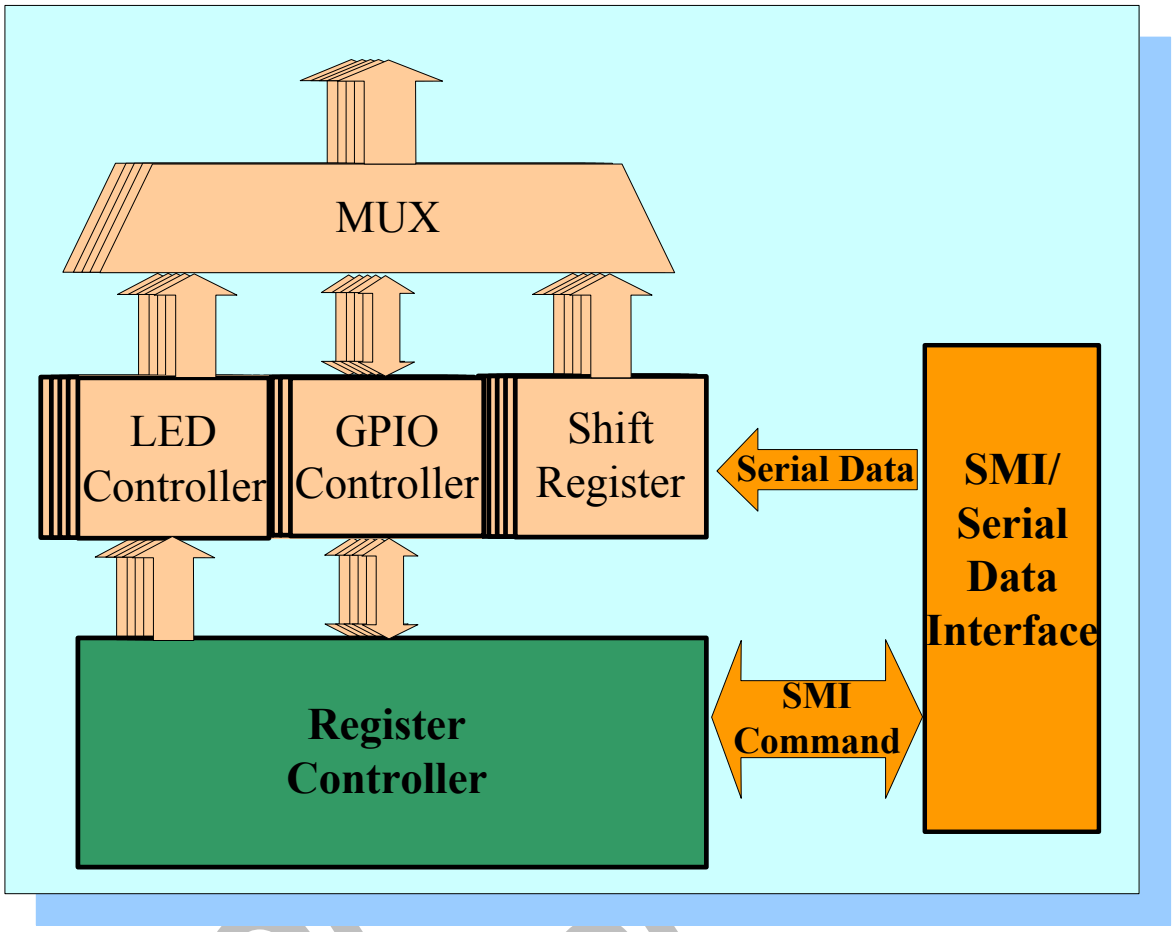
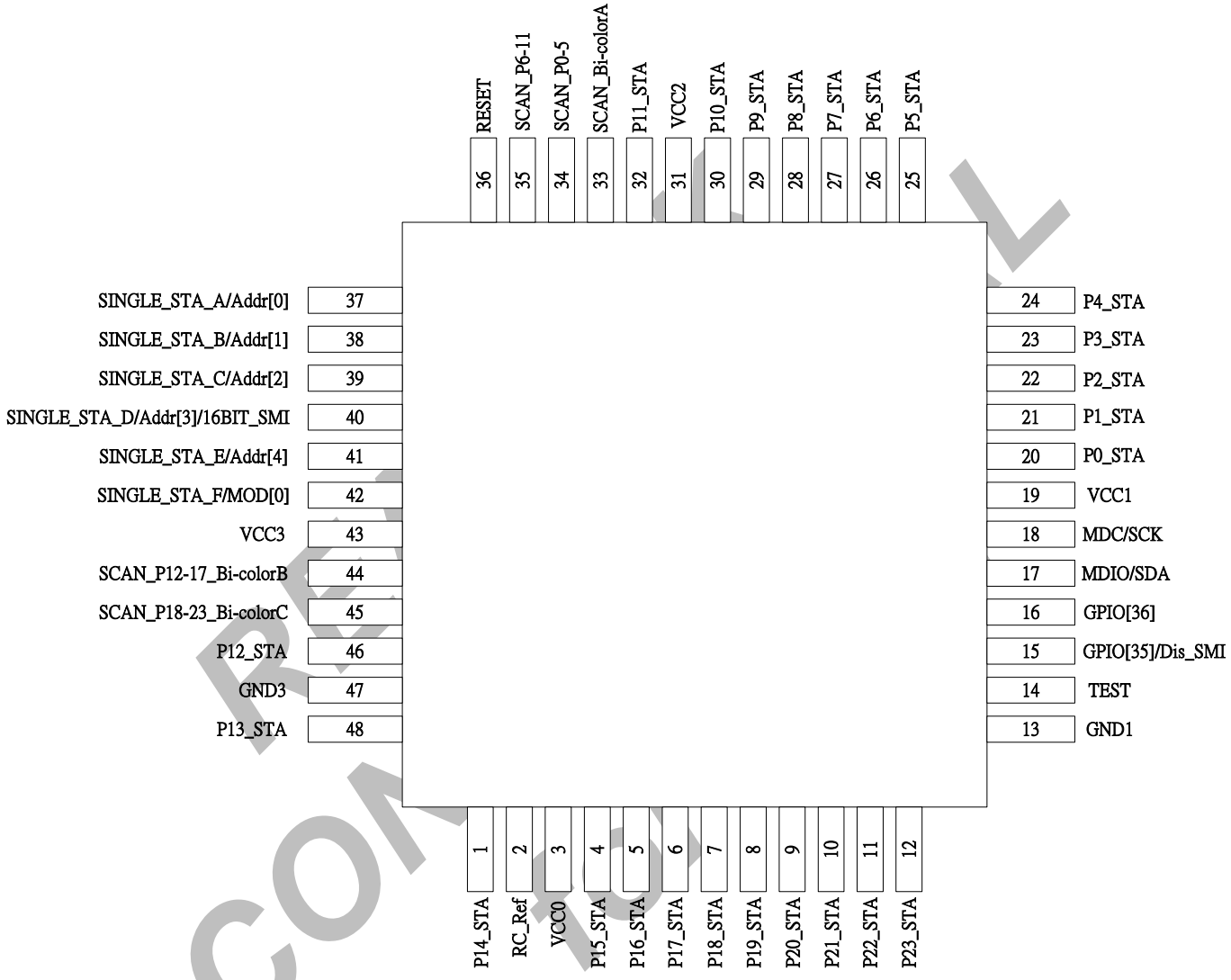


Figure 4. RTL8231 Block Diagram

5. Pin Assignments

5.1. SMI Mode Scan Bi-color Pin Assignment



5.1.1. SMI Mode Scan Bi-color Pin Assignment Table

Upon Reset: Defined as a short time after the end of a hardware reset.

After Reset: Defined as the time after the specified 'Upon Reset' time.

I: Input Pin

O: Output Pin

I/O: Bi-Direction Input/Output Pin

P: Digital Power Pin

G: Digital Ground Pin

$I_{PU:}$ Input Pin With Pull-Up Resistor;
(Typical Value = 75K ohm)

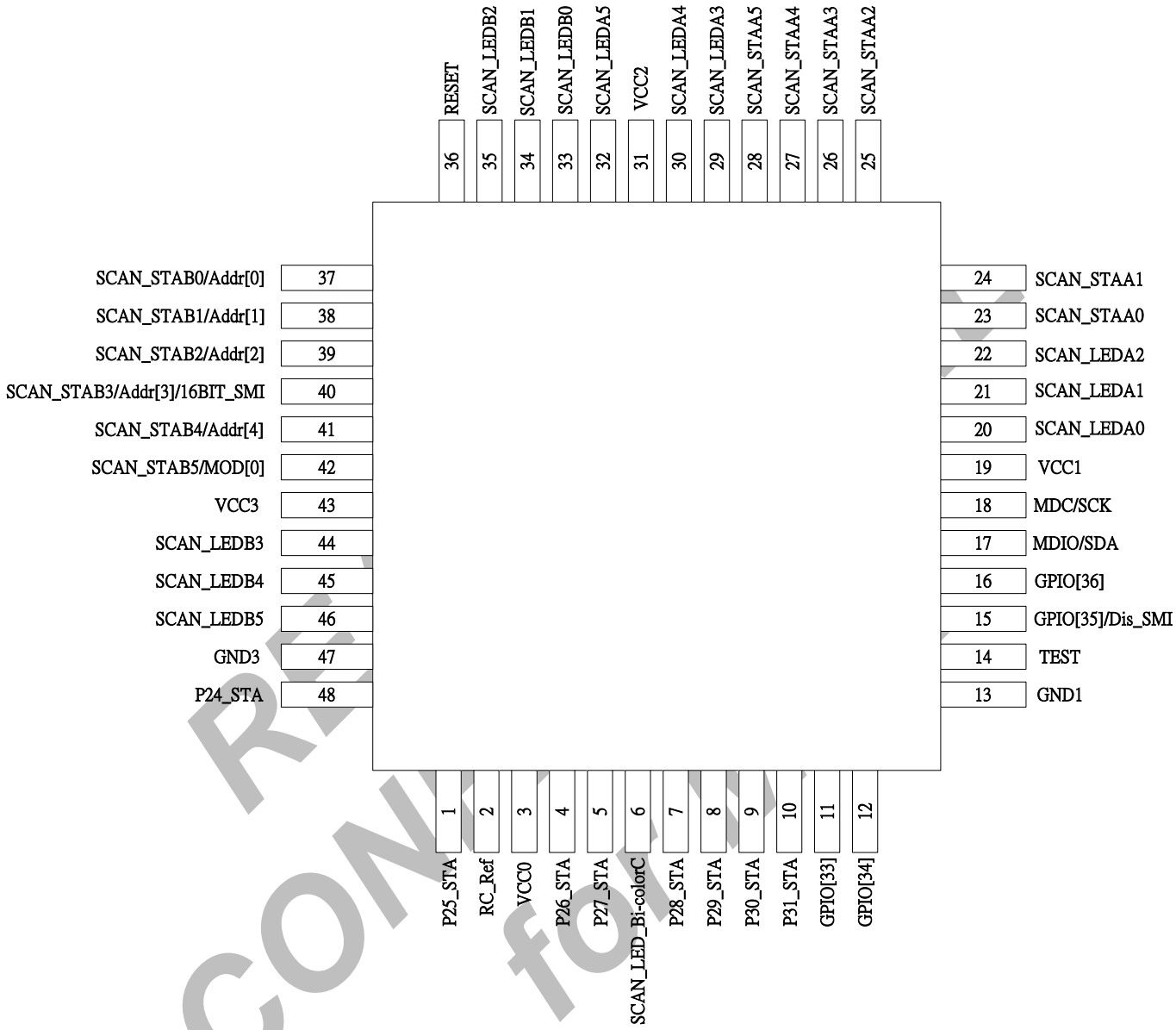
$O_{PU:}$ Output Pin With Pull-Up Resistor;
(Typical Value = 75K ohm)

Table 1. Pin Assignment Table

Name	Pin No.	Type	Driving Current (mA)	Name	Pin No.	Type	Driving Current (mA)
P14_STA	1	I/O	8	GPIO[35]/Dis_SMI	15	I/O_{PD}	8
RC_Ref	2	I/O	-	GPIO[36]	16	I/O	8
VCC0	3	P	-	MDIO/SDA	17	I/O_{PU}	-
P15_STA	4	I/O	8	MDC/SCK	18	O	-
P16_STA	5	I/O	8	VCC1	19	P	-
P17_STA	6	I/O	8	P0_STA	20	I/O	8
P18_STA	7	I/O	8	P1_STA	21	I/O	8
P19_STA	8	I/O	8	P2_STA	22	I/O	8
P20_STA	9	I/O	8	P3_STA	23	I/O	8
P21_STA	10	I/O	8	P4_STA	24	I/O	8
P22_STA	11	I/O	8	P5_STA	25	I/O	8
P23_STA	12	I/O	8	P6_STA	26	I/O	8
GND1	13	G	-	P7_STA	27	I/O	8
TEST	14	I	-	P8_STA	28	I/O	8

Name	Pin No.	Type	Driving Current (mA)
P9_STA	29	I/O	8
P10_STA	30	I/O	8
VCC2	31	P	-
P11_STA	32	I/O	8
SCAN_Bi-colorA	33	I/O	24
SCAN_P0-5	34	I/O	24
SCAN_P6-11	35	I/O	24
RESET	36	I	-
SINGLE_STA_A/Addr[0]	37	I/O_{PU}	4
SINGLE_STA_B/Addr[1]	38	I/O_{PU}	4
SINGLE_STA_C/Addr[2]	39	I/O_{PU}	4
SINGLE_STA_D/Addr[3]/16BIT_SMI	40	I/O_{PU}	4
SINGLE_STA_E/Addr[4]	41	I/O_{PU}	4
SINGLE_STA_E/MOD[0]	42	I/O_{PU}	4
VCC3	43	P	-
SCAN_P12-17_BicolorB	44	I/O	24
SCAN_P18-23_BicolorC	45	I/O	24
P12_STA	46	I/O	8
GND	47	G	-
P13_STA	48	I/O	8

5.2. SMI Mode Scan Single color Pin Assignment



5.2.1. SMI Mode GPIO Pin Assignment Table

Upon Reset: Defined as a short time after the end of a hardware reset.

After Reset: Defined as the time after the specified 'Upon Reset' time.

I: Input Pin

O: Output Pin

I/O: Bi-Direction Input/Output Pin

P: Digital Power Pin

G: Digital Ground Pin

$I_{PU:}$ Input Pin With Pull-Up Resistor;
(Typical Value = 75K ohm)

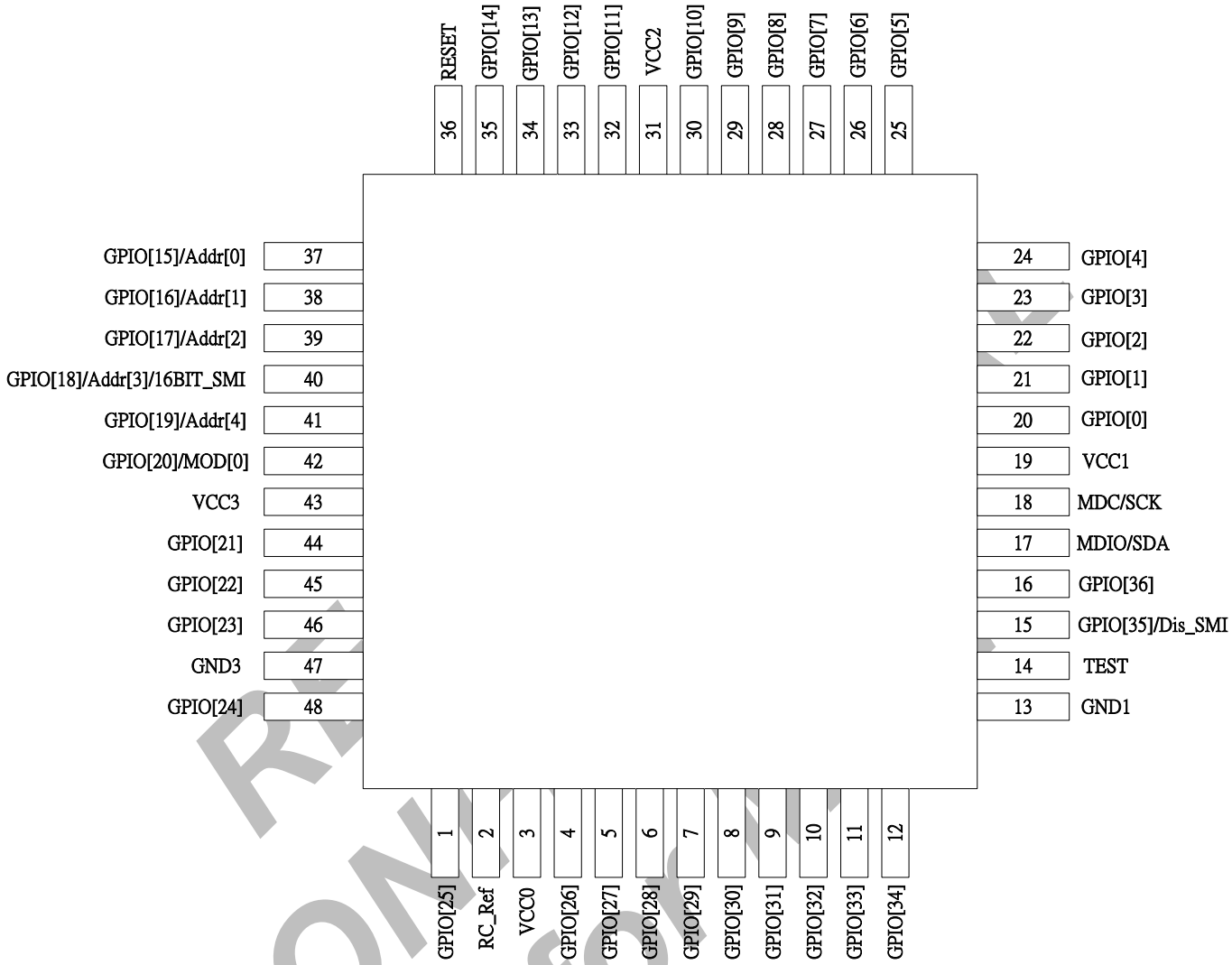
$O_{PU:}$ Output Pin With Pull-Up Resistor;
(Typical Value = 75K ohm)

Table 2. Pin Assignment Table

Name	Pin No.	Type	Driving Current (mA)	Name	Pin No.	Type	Driving Current (mA)
P25_STA	1	I/O	8	TEST	14	I	-
RC_Ref	2	O	-	GPIO[35]/Dis_SMI	15	I/O_{PD}	8
VCC0	3	P	-	GPIO[36]	16	I/O	8
P26_STA	4	I/O	8	MDIO/SDA	17	I/O_{PU}	-
P27_STA	5	I/O	8	MDC/SCK	18	O	-
SCAN_LED_Bi-colorC	6	I/O	24	VCC1	19	P	-
				SCAN_LEDA0	20	I/O	24
P28_STA	7	I/O	8	SCAN_LEDA1	21	I/O	24
P29_STA	8	I/O	8	SCAN_LEDA2	22	I/O	24
P30_STA	9	I/O	8	SCAN_STAA0	23	I/O	4
P31_STA	10	I/O	8	SCAN_STAA1	24	I/O	4
GPIO[33]	11	I/O	8	SCAN_STAA2	25	I/O	4
GPIO[34]	12	I/O	8	SCAN_STAA3	26	I/O	4
GND1	13	G	-	SCAN_STAA4	27	I/O	4

Name	Pin No.	Type	Driving Current (mA)
SCAN_STAA5	28	I/O	4
SCAN_LEDA3	29	I/O	24
SCAN_LEDA4	30	I/O	24
VCC2	31	P	-
SCAN_LEDA5	32	I/O	24
SCAN_LEDB0	33	I/O	24
SCAN_LEDB1	34	I/O	24
SCAN_LEDB2	35	I/O	24
RESET	36	I	-
SCAN_STAB0/Addr[0]	37	I/O_{PU}	4
SCAN_STAB1/Addr[1]	38	I/O_{PU}	4
SCAN_STAB2/Addr[2]	39	I/O_{PU}	4
SCAN_STAB3/Addr[3]/16BIT_SMI	40	I/O_{PU}	4
SCAN_STAB4/Addr[4]	41	I/O_{PU}	4
SCAN_STAB5/MOD[0]	42	I/O_{PU}	4
VCC3	43	P	-
SCAN_LEDB3	44	I/O	24
SCAN_LEDB4	45	I/O	24
SCAN_LEDB5	46	I/O	24
GND	47	G	-
P24_STA	48	I/O	8

5.3. SMI Mode GPIO Pin Assignment



5.3.1. SMI Mode GPIO Pin Assignment Table

Upon Reset: Defined as a short time after the end of a hardware reset.

After Reset: Defined as the time after the specified 'Upon Reset' time.

I: Input Pin

O: Output Pin

I/O: Bi-Direction Input/Output Pin

P: Digital Power Pin

G: Digital Ground Pin

$I_{PU:}$ Input Pin With Pull-Up Resistor;
(Typical Value = 75K ohm)

$O_{PU:}$ Output Pin With Pull-Up Resistor;
(Typical Value = 75K ohm)

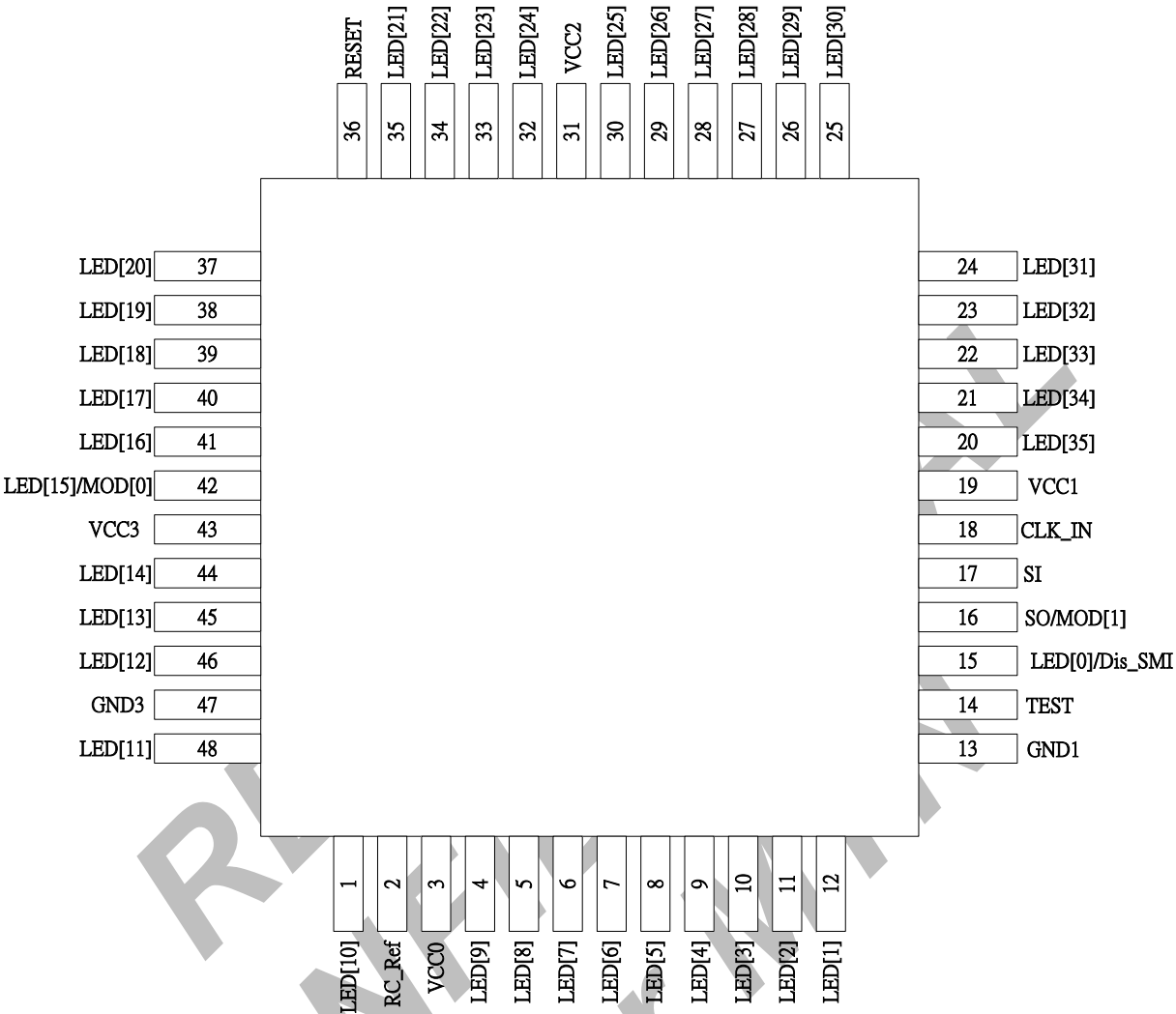
Table 3. Pin Assignment Table

Name	Pin No.	Type	Driving Current (mA)	Name	Pin No.	Type	Driving Current (mA)
GPIO[25]	1	I/O	8	GPIO[35]/Dis_SMI	15	I/O_{PD}	8
RC_Ref	2	O	-	GPIO[36]	16	I/O	8
VCC0	3	P	-	MDIO	17	I/O_{PU}	-
GPIO[26]	4	I/O	8	MDC	18	O	-
GPIO[27]	5	I/O	8	VCC1	19	P	-
GPIO[28]	6	I/O	8	GPIO[0]	20	I/O	8
GPIO[29]	7	I/O	8	GPIO[1]	21	I/O	8
GPIO[30]	8	I/O	8	GPIO[2]	22	I/O	8
GPIO[31]	9	I/O	8	GPIO[3]	23	I/O	8
GPIO[32]	10	I/O	8	GPIO[4]	24	I/O	8
GPIO[33]	11	I/O	8	GPIO[5]	25	I/O	8
GPIO[34]	12	I/O	8	GPIO[6]	26	I/O	8
GND1	13	G	-	GPIO[7]	27	I/O	8
TEST	14	I	-	GPIO[8]	28	I/O	8

Name	Pin No.	Type	Driving Current (mA)
GPIO[9]	29	I/O	8
GPIO[10]	30	I/O	8
VCC2	31	P	-
GPIO[11]	32	I/O	8
GPIO[12]	33	I/O	8
GPIO[13]	34	I/O	8
GPIO[14]	35	I/O	8
RESET	36	I	-
GPIO[15]/Addr[0]	37	I/O_{PU}	8
GPIO[16]/Addr[1]	38	I/O_{PU}	8
GPIO[17]/Addr[2]	39	I/O_{PU}	8

Name	Pin No.	Type	Driving Current (mA)
GPIO[18]/Addr[3]/16BIT_SMI	40	I/O_{PU}	8
GPIO[19]/Addr[4]	41	I/O_{PU}	8
GPIO[20]/MOD[0]	42	I/O_{PU}	8
VCC3	43	P	-
GPIO[21]	44	I/O	8
GPIO[22]	45	I/O	8
GPIO[23]	46	I/O	8
GND	47	G	-
GPIO[24]	48	I/O	8

5.4. Shift Register Mode Pin Assignment



5.5. Shift Register Mode Pin Assignment Table

Upon Reset: Defined as a short time after the end of a hardware reset.

After Reset: Defined as the time after the specified 'Upon Reset' time.

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O: Output Pin

I/O: Bi-Direction Input/Output Pin

P: Digital Power Pin

G: Digital Ground Pin

$I_{PU:}$ Input Pin With Pull-Up Resistor;
(Typical Value = 75K ohm)

$O_{PU:}$ Output Pin With Pull-Up Resistor;
(Typical Value = 75K ohm)

Table 4. Pin Assignment Table

Name	Pin No.	Type	Driving Current (mA)	Name	Pin No.	Type	Driving Current (mA)
LED[10]	1	I/O	4	LED[0]/Dis_SMI	15	I/O_{PD}	4
RC_Ref	2	O	-	SO/MOD[1]*a	16	I/O	4
VCC0	3	P	-	SI	17	I/O_{PU}	-
LED[9]	4	I/O	4	CLK_IN	18	O	-
LED[8]	5	I/O	4	VCC1	19	P	-
LED[7]	6	I/O	4	LED[35]	20	I/O	4
LED[6]	7	I/O	4	LED[34]	21	I/O	4
LED[5]	8	I/O	4	LED[33]	22	I/O	4
LED[4]	9	I/O	4	LED[32]	23	I/O	4
LED[3]	10	I/O	4	LED[31]	24	I/O	4
LED[2]	11	I/O	4	LED[30]	25	I/O	4
LED[1]	12	I/O	4	LED[29]	26	I/O	4
GND1	13	G	-	LED[28]	27	I/O	4
TEST	14	I	-	LED[27]	28	I/O	4

Name	Pin No.	Type	Driving Current (mA)
LED[26]	29	I/O	4
LED[25]	30	I/O	4
VCC2	31	P	-
LED[24]	32	I/O	4
LED[23]	33	I/O	4
LED[22]	34	I/O	4
LED[21]	35	I/O	4
RESET	36	I	-
LED[20]	37	I/O_{PU}	4
LED[19]	38	I/O_{PU}	4
LED[18]	39	I/O_{PU}	4

Name	Pin No.	Type	Driving Current (mA)
LED[17]	40	I/O_{PU}	4
LED[16]	41	I/O_{PU}	4
LED[15]/MOD[0]	42	I/O_{PU}	4
VCC3	43	P	-
LED[14]	44	I/O	4
LED[13]	45	I/O	4
LED[12]	46	I/O	4
GND	47	G	-
LED[11]	48	I/O	4

a. Pin 16 SO/MOD[1] internal floating. Must be pull high or low to select the active high or active low application.

6. Pin Descriptions

6.1. SMI Mode Scan Single Color LED Output Pins

Table 5. Media Dependent Interface Pins

Pin Name	Pin No.	Type	Drive (mA)	Description
Port 0-11 SCAN_STAA1~ SCAN_STAA5	23, 24, 25, 26, 27, 28	I/O	4	Scan LED Status Pins for Port 0~11。
SCAN_LEDA0~ SCAN_LEDA5	20, 21, 22, 29, 30, 32	I/O	24	Scan LED Scan pin for port 0~11。
Port 12-23 SCAN_STAB0~ SCAN_STAB5	37, 38, 39, 40, 41, 42	I/O	4	Scan LED Status Pins for Port 12~23。
SCAN_LEDB0~ SCAN_LEDB5	33, 34, 35, 44, 45, 46	I/O	24	Scan LED Scan pin for port 12~23。
Port 24-31 Bi-color P24_STA~ P31_STA	48, 1, 4, 5, 7, 8, 9, 10, 11	I/O	8	Scan LED Bi-color Status Pins for Port 24~31。
SCAN_LED_Bi-colorC	6	I/O	24	Scan LED Bi-color Scan Pins foe Port 24~31。
GPIO[33]	11			GPIO pin
GPIO[34]	12			GPIO pin
GPIO[35]	15			GPIO pin
GPIO[36]	16			GPIO pin

6.2. SMI Mode Scan Bi-color LED Output Pins

Table 6. Media Dependent Interface Pins

Pin Name	Pin No.	Type	Drive (mA)	Description
Port 0-11 P0_STA~ P11_STA	20,21,22,23, 24,25,26,27, 28,29,30,32	O	8	Scan LED Bi-color Status Pins for Port 0~11。
SCAN_Bi-colorA	33		24	Scan LED Bi-color Scan Pins foe Port 0~11。
Port 12-23 P12_STA~ P23_STA	46,48,1,4, 5,6,7,8, 9,10,11,12	O	8	Scan LED Bi-color Status Pins for Port 12~23。
SCAN_P12-17_Bi-colorB	44		24	Scan LED Bi-color Scan Pins foe Port 12~17。
SCAN_P18-23_Bi-colorC	45		24	Scan LED Bi-color Scan Pins foe Port 18~23。
SINGLE_STA_A ~ SINGLE_STA_D		O	4	Scan LED per port Single color LED status Pins for Port 0~23。
SCAN_P0-5 SCAN_P6-11 SCAN_P11-17_Bi-colorB SCAN_P18-23_Bi-colorC			24	Scan LED Scan pin for per port LED2 Single-color LED。 These include port 0~23。
GPIO[35]	15			GPIO pin
GPIO[36]	16			GPIO pin

6.3. SMI Mode Miscellaneous Pins

Table 7. Miscellaneous Pins

Pin Name	Pin No.	Type	Description
RC_Ref	2	AO	RC oscillator circuit. Should be Parallel connection (+/- 1%) resistance 249 ohm and (+/- 1%) capacitance 1nF when operate at the SMI mode. *Note: The layout trace inductance must under 10nH.*

Pin Name	Pin No.	Type	Description
MDC/SCK	18	I/O_{PU}	Serial Management Data clock MDC operates speed at 0-25Mhz/SCK operates speed at 0-1Mhz *Note: SCK operates max speed 1M is depend on RC clock 10Mhz.*
MDIO/SDA	17	AI	Serial Management Data Input/Output
RESET	36	I_{PU}	System Pin Reset Input. When low active will reset the RTL8231
TEST	14	I_{PD}	Internal test pin. Must pull-down.

6.4. SMI Mode Configuration Strapping Pins

Table 8. Configuration Strapping Pins

Pin Name	Pin No.	Type	Description
GPIO[15]/Addr[0]	37	I/O_{PU}	When MDC/MDIO is selected, Addr[4:0] is Phy Address. When SMI Slave interface is selected, Addr[2:0] is Device ID, and the strapping Addr[3] change to the 16BIT_ SMI. 16BIT_SMI can define SMI Slave format is 16bit word addres when 16BIT_SMI set high. *When SMI Slave interface is selected，Addr[4] is reserved.*
GPIO[16]/Addr[1]	38	I/O_{PU}	
GPIO[17]/Addr[2]	39	I/O_{PU}	
GPIO[18]/Addr[3]/16BIT_SMI	40	I/O_{PU}	
GPIO[19]/Addr[4]	41	I/O_{PU}	
GPIO[20]/MOD[0]	42	I/O_{PU}	Select MDC/MDIO interface when this strapping pin pull-high and SMI is enabled.
LED[0]/Dis_SMI	15	I/O_{PD}	Select RTL8231 in the SMI mode or Shift Register mode. Pull-up is setting to shift register mode. Pull-down is setting to SMI mode. Internal value is Pull-down.

6.5. Shift Register Mode Pins

Table 9. Shift Register Mode Pins

Pin Name	Pin No.	Type	Drive (mA)	Description
SO/MOD[1]	16	I/O	8	For cascade to the RTL8231 of the next stage. Always output the same data with the pin of LED[35]. Never output data inversely.
LED[0]/Dis_SMI	15			The first output with the serial data output pin. Maybe output inversely when the strapping MOD[1:0] at the different compose. Must be pull-high when select Shift Register mode.
LED[15]/MOD[0]	42			The15th output with the serial data output pin. Maybe output inversely when the strapping MOD[1:0] at the different compose.
LED[2] ~ LED[35]		O	8	Serial data shift output pin.

6.6. Shift Register Mode Miscellaneous Pins

Table 10. Shift Register Miscellaneous Pins

Pin Name	Pin No.	Type	Description
RC_Ref	2	AO	RC oscillator circuit. Should be Parallel connection general resistance 249 ohm and general capacitance 1nF when operate at the shift register mode. *Note: The layout trace inductance must under 10nH.*
CLK_IN	18	I/O_{PU}	Serial Data clock. CLK_IN operates speed at 0-25Mhz
SI	17	AI	Serial Data Input
RESET	36	I_{PU}	System Pin Reset Input. When low active will reset the RTL8231
TEST	14	I_{PD}	Internal test pin. Must pull-down.

6.7. Shift Register Configuration Strapping Pins

Table 11. Shift Register Mode Configuration Strapping Pins

Pin Name	Pin No.	Type	Description
LED[0]/Dis_SMI	15	I/O_{PU}	Select RTL8231 in the SMI mode or Shift Register mode. Pull-up is setting to shift register mode. Pull-down is setting to SMI mode. Internal value is Pull-down.
MOD[1:0]	15 42	I/O	Define the shift register initial vale after the power on or reset. MOD[1:0] can define four compose of [active high, initial low]，[active high, initial high]，[active low, initial low]，and [active low, initial high]. MOD[1] defines that application circuit is active high or low. MOD[0] defines the initial value is output high or low. MOD[1:0] 00: Active low and initial value is low. At this mode, LED[15]/MOD[0] (pin42) output inverse data always. 01: Active low and initial value is high. 10: Active high and initial value is low. At this mode, LED[0]/Dis_SMI (pin15) output inverse data always. 11: Active high and initial value is high. At this mode, LED[0]/Dis_SMI (pin15) and LED[15]/MOD[0] (pin42) output inverse data always.

7. Controller Interfaces

The strapping “Dis_SMI” of the RTL8231 can set the chip at the GPIO mode or shift register mode. The RTL8231 is GPIO mode when the strapping “Dis_SMI” pull low and pull high at shift register mode. When the RTL8231 is the GPIO mode the control interface is the SMI interface, and the serial data interface at the shift register mode.

7.1. SMI (MDC, MDIO) Interface

SMI (MDC, MDIO) Management Packet Format

Table 12. SMI (MDC, MDIO) Management Packet Format

	Management Frame Fields							
	PRE	**ST**	**OP**	**PHYAD**	**REGAD**	**TA**	**DATA**	**IDLE**
Read	1…1	01	10	AAAAA	RRRRR	Z0	DDDDDDDDDDDDDDDD	Z
Write	1…1	01	01	AAAAA	RRRRR	10	DDDDDDDDDDDDDDDD	Z

PRE (Preamble)

At the beginning of each transaction, the station management entity shall send a sequence of 32 or 8 contiguous logic one bits on MDIO with 32 or 8 corresponding cycles on MDC.

Note：If the 8 Bits preamble MDIO format be used then the MDC must be a free run clock.

PHYAD (PHY Address)

The RTL8231 PHY address default is 5b’11111. Support PHY address from 0 to 31.

REGAD (Register Address)

The register address is five bits.

Data

The data field is 16 bits. The first data bit transmitted and received shall be bit 15 of the register being addressed.

Note：Because of the RL6129 clock is independence from whole system clock，MDC/MDIO circuit need the first two clock cycle to help RTL8231 start the MDC/MDIO circuit at the MDC/MDIO mode. That's mean the first command could be fail when the first command transmit with the first MDC clock cycle.

7.2. SMI Slave Interface

The strapping Pin "MOD[0]" can decide between MDC/MDIO and SMI_Slave interface. The switch MAC can access the RTL8231 by SDA and SCK。 The follow as the figure show that the SMI cycle of the MAC access ASIC which start and end by the Start state and the Stop state.

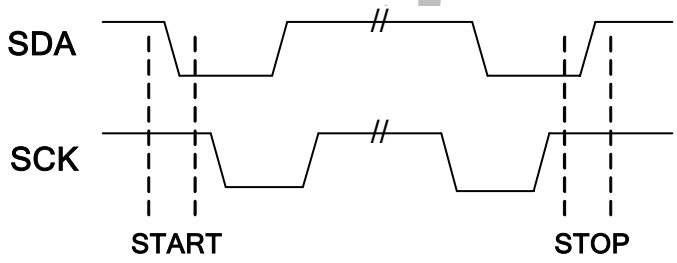

Figure 1 Start/Stop state waveform

SMI supports sequential Read / Write and a Read / Write a 16-bits data, which could control by strapping pin '16BIT_SMI' (pin40) to determine the support for 16 bits or 8 bits of word address. When the word address of 16 bits, its data format should be control byte (1) + address bytes (2) + data bytes (2N, N: integer, N ≠ 0) a combination of the following format shown below:

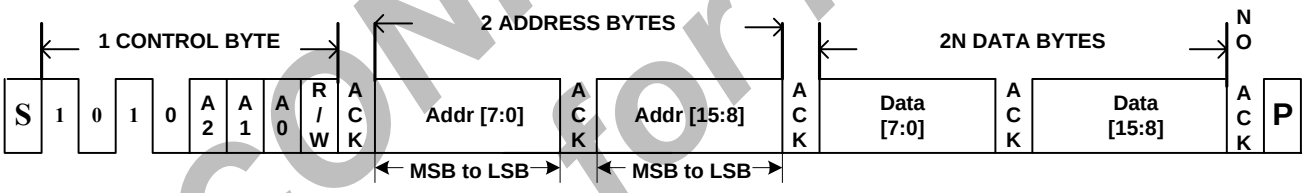

Figure 2 16 Bits Word Address Access sequence

When the CPU to Read / Write 16-bits data to the ASIC, the first control byte of the LSB will be set to 1 (R) / 0 (W), for every eight data clock to be more than one ACK (0) clock (ACK from the CPU to inform ASIC has received 8-bits data).

When the word address is 8bits, its data format should be control byte (1) + address byte (1) + data byte (2N, N: integer, N ≠ 0) a combination of the following format shown below:

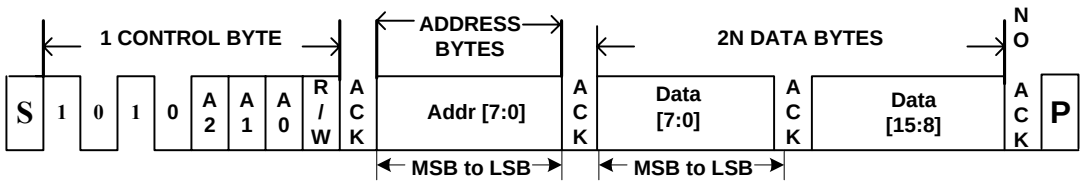

Figure 3 8 Bits Word Address Access sequence

Note：The fast frequency of SCK supports to 1Mhz at the SMI Slave interface.

8. Function Description

8.1. Reset

8.1.1. Hardware Reset

In a power-on reset, an internal power-on reset pulse is generated and the RTL8231 will start the reset initialization procedures. These are:

- Determine various default settings via the hardware strap pins at the end of the nRESET signal
- Initialize the internal registers

8.1.2. Software Reset

When Software Reset is set to 1'b1 (write and self-clear), the chip will take the following steps:

1. Initialize the internal registers

8.2. Shift Register Mode

The RTL8231 shift register mode could reserve the serial data, and output parallel data in order. There has the 36 shift register in the RTL8231. The output data sequence show below:

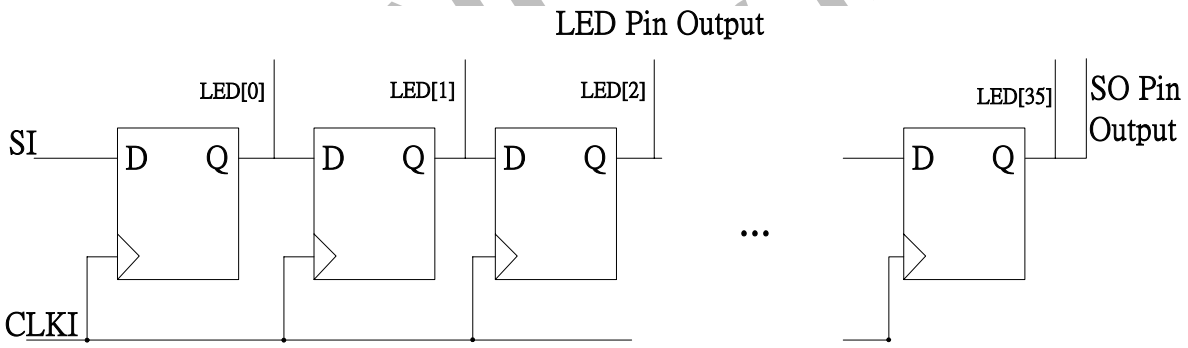

Figure 4 Start/Stop state waveform

To latch the currently serial data which receive at the SI pin and shift the preceding data to the next stage at the Each rising edge of the serial clock. At the first the serial data input the RTL8231 output from the

pin 15 LED[0]. At the last shift register, the serial data output to LED[35] pin and the SO pin at the same time.

8.2.1. Shift Register Mode System Application

The RTL8231 shift register mode is designed for LED circuit of the Switch application. The RTL8231 Shift Register mode have the four status corresponded to different LED status circuit of the Switch application. The status individual the [active low, initial low], [active low, initial high], [active high, initial low], and [active high, initial high]. The active high or low means that the Switch external serial LED circuit be blinked by high single or low single. The initial high or low means that the shift register initial output is high or low after power on or hardware pin reset. If the serial data stream is show as the below figure:

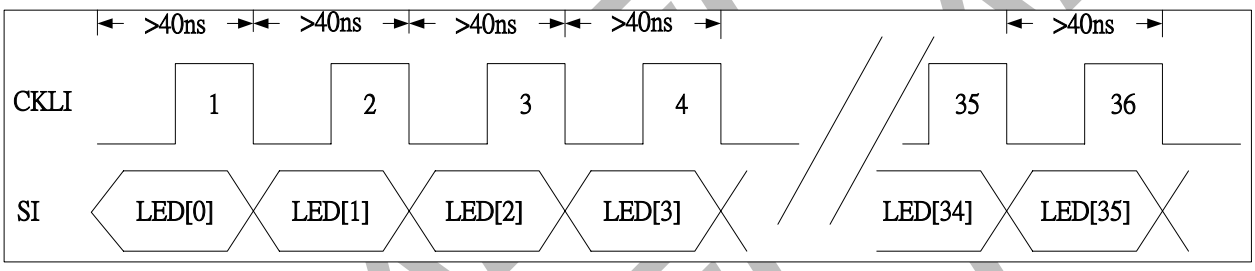

Figure 5, Serial Stream

The active low external serial to parallel LED circuit shown below:

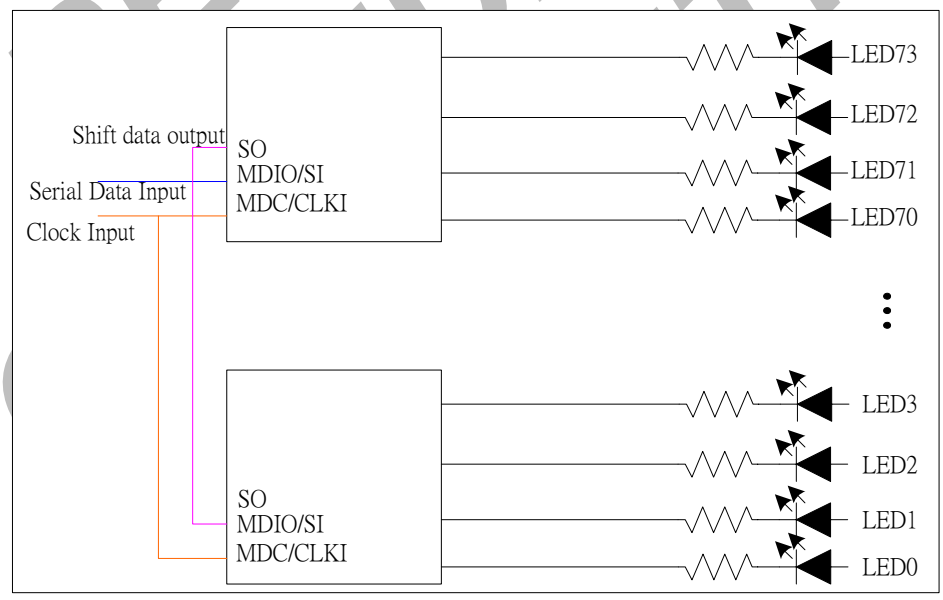

Figure 6, External Circuit for Serial to Parallel LED

Because of the parallel data output pin has the strapping pin be coexisted. The strapping pin value may has the inversely values which we don't want. The RTL8231 strapping outputs have the inverse or non-inverse data by different status [active low, initial low], [active low, initial high], [active high, initial low], and [active high, initial high].

Table 13. The inverse data by different LED application mode

LED[0]/Dis_SMI(pin15)		LED[15]/MOD[0] (pin42)		SO/MOD[1] (pin16)		
Initial pull-down		Initial pull-high		Initial floating		
Strapping value	Serial mod output value	Strapping value	Serial mod output value	Strapping value	Serial mod output value	Status Mode
1 **pull-high**	D Non-inverse	**0** **pull-down**	$\overline{D}$ (Serial output data will be inversed)	**0** **pull-down**	D Non-inverse	External LED Circuit Active low and initial output low after power on and or pin reset.
1 **pull-high**	D Non-inverse	**1** **pull-high**	D Non-inverse	**0** **pull-down**	D Non-inverse	External LED Circuit Active low and initial output high after power on and or pin reset.
1 **pull-high**	$\overline{D}$ (Serial output data will be inversed)	**0** **pull-down**	D Non-inverse	**1** **pull-high**	D Non-inverse	External LED Circuit Active high and initial output low after power on and or pin reset.
1 **pull-high**	$\overline{D}$ (Serial output data will be inversed)	**1** **pull-high**	$\overline{D}$ (Serial output data will be inversed)	**1** **pull-high**	D Non-inverse	External LED Circuit Active high and initial output high after power on and or pin reset.

8.3. Scan LED Single color Mode

The all of LEDs status be controlled by register. Each of LED has the 3 bits register to decide off, light, blinking 32ms, 64ms, 128ms, 256ms, 512ms, and 1024ms.*a MAC can control LED status register by SMI interface (MDC/MDIO or SMI_Slave).

a. The blinking timing is depend on the 10Mhz RC clock.

Scan LED Single Color Mode is compose of the twins 6x6 circuit matrix. Scan LED single color mode external circuit is shown below：

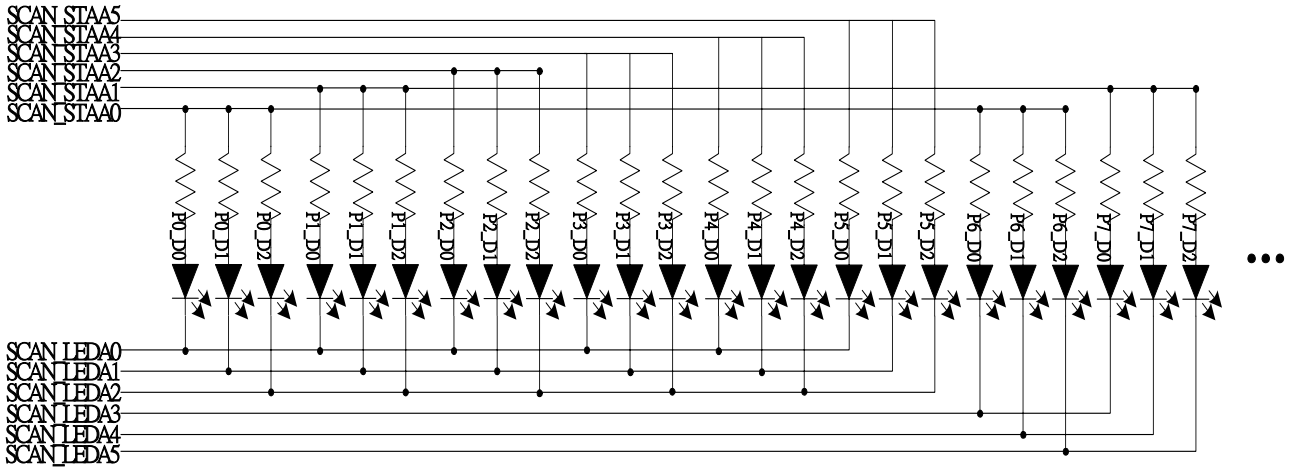

Figure 7, External Circuit for Single color Scan Mode

The Scan LED Single color mode timing diagram is shown below:

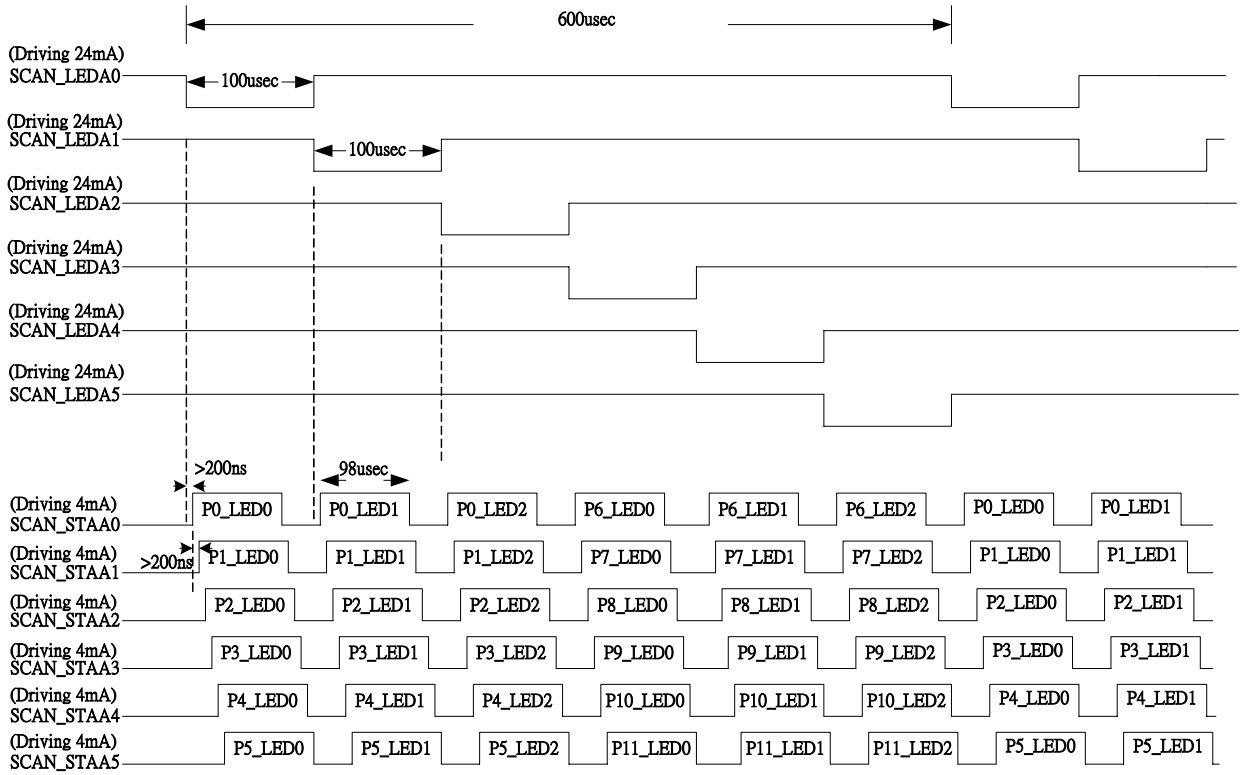

Figure 8, Scan LED Timing Diagram for Single color Mode*a

a. The Scan LED timing is depend on the 10Mhz RC clock.

The LED is turned on interval between 0.2usec to avoid rush current at all of Scan LED mode.

8.3.1. Scan Single Color Mode with RTL8328S Application

RTL8328S application is the 24ports Fast Ethernet + 4 Ports 1000 Base-T/1000 Base-X Switch. At the 24 ports 10/100M Ethernet, each port LED status could be used the two single color LED. There is use 48 LEDs in the twins 6x6 scan circuit matrix at the 24 port 10/100M Ethernet application. The remainder Single Color LED can use at 1000M Ethernet port Single Color status.

At the RTL8328S the 1000 Base-T and 1000 Base-X bi-color LED status are dividing. Because need to supporting 1000 Base-T/1000 Base-X at the same time，RTL8231 has the 8 bi-color LED at the Scan single color mode.

At the Scan single color LED mode the 8 port bi-color LED timing diagram is shown below:

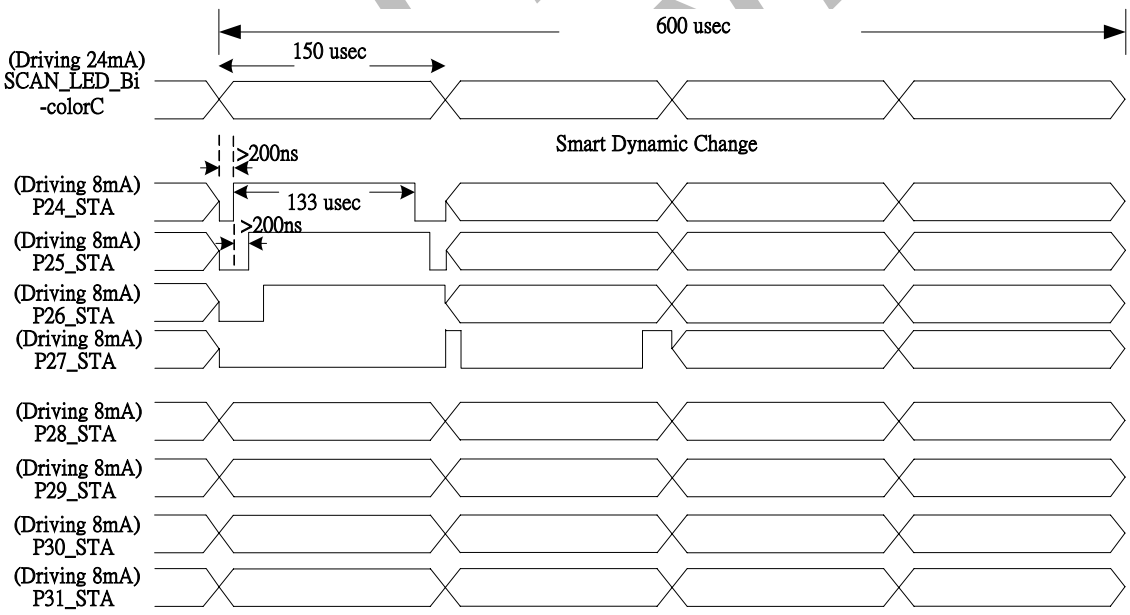

Figure 9, Scan LED Timing Diagram for Single color Mode with 28S Bi-color LED

8.3.2. Scan Single Color Output Matrix Maps to Control Register

The scan single color output pins constitute the scan matrix. In each of cross line in the scan matrix, which maps to the LED control register is show below:

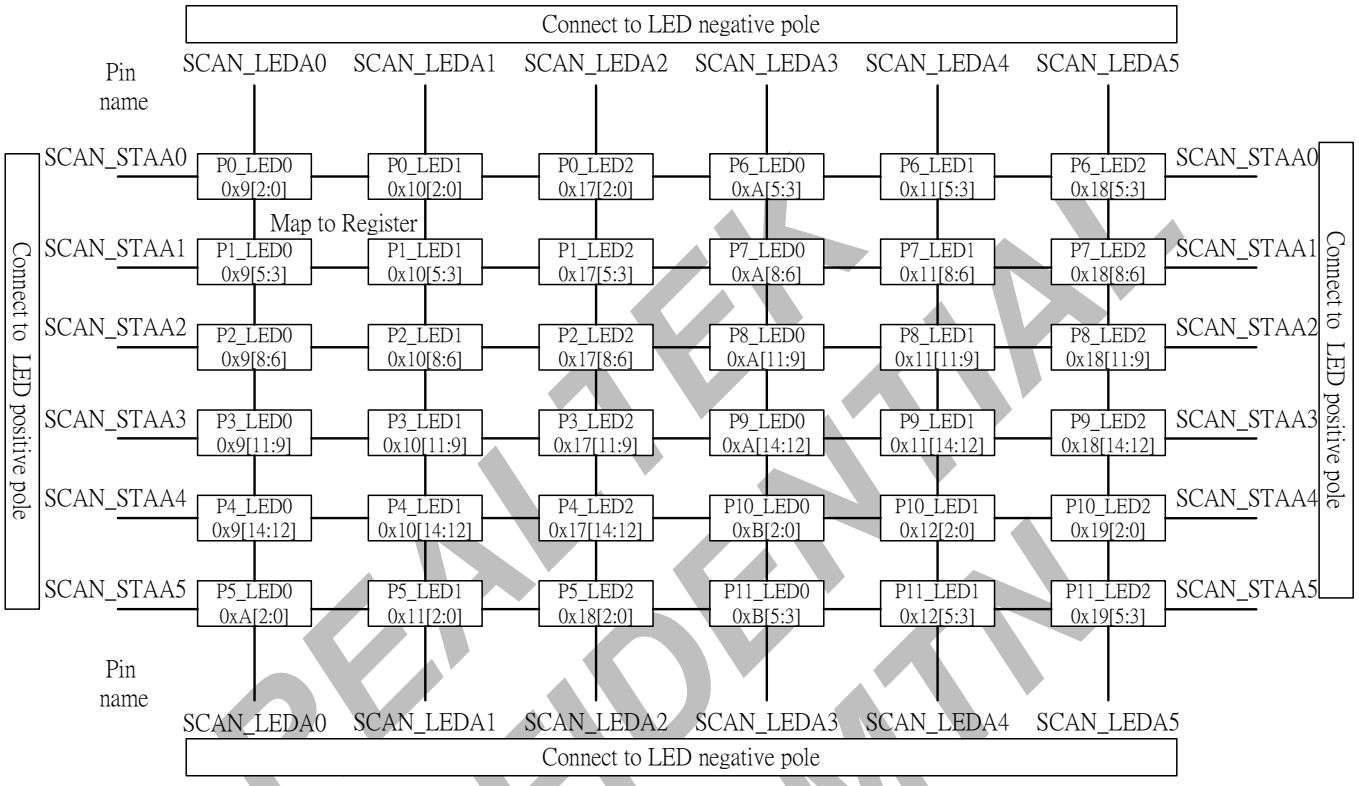

Figure 10, Scan single color LED circuit maps to control register at group A.

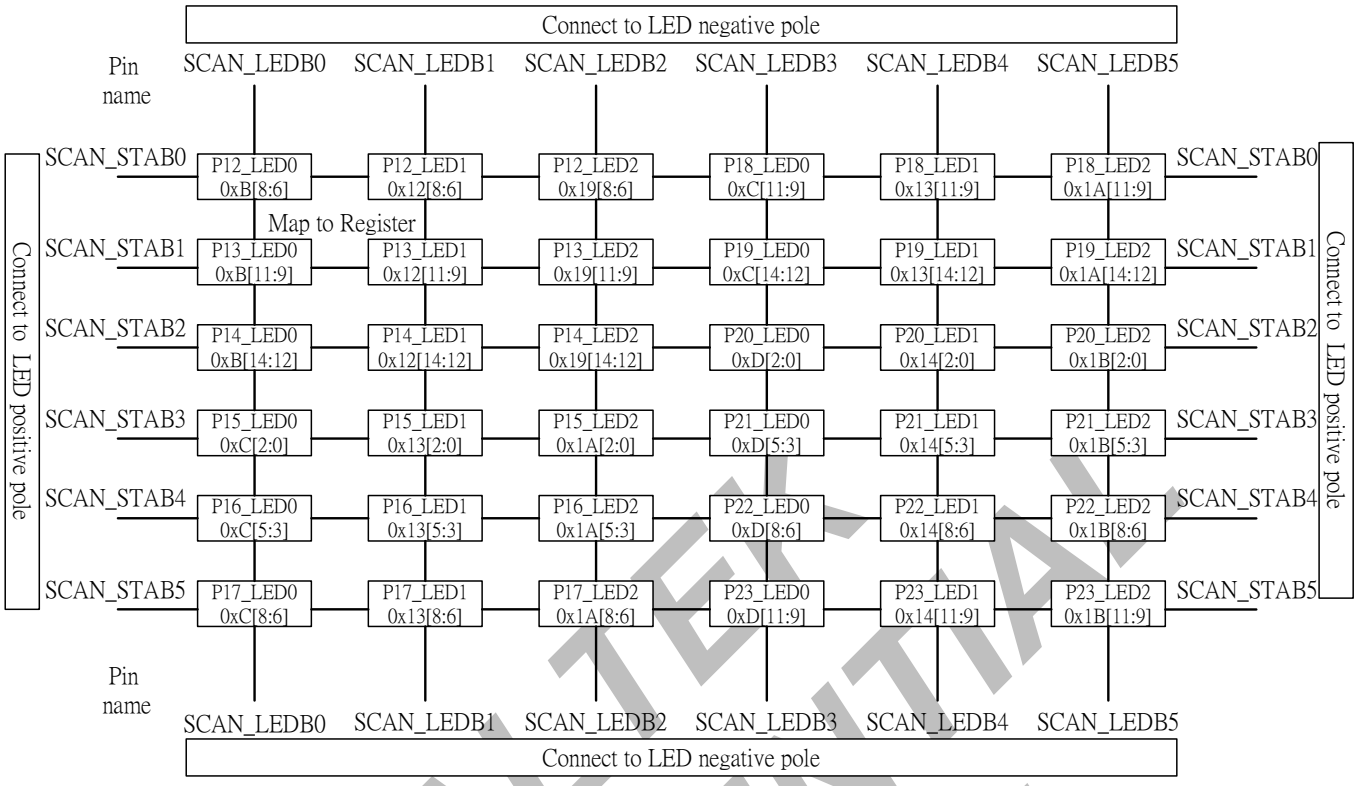

Figure 11, Scan single color LED circuit maps to control register at group B.

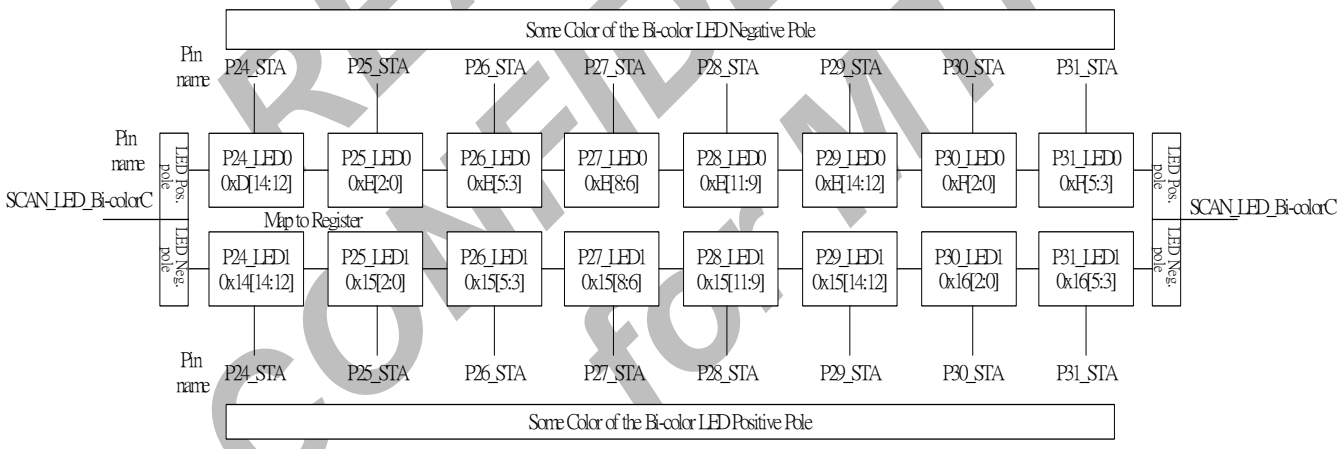

Figure 12, Scan single color LED circuit maps to control register at group C.

8.4. SCAN LED Bi-color Mode

Scan Bi-color mode supports 24 ports Bi-color scanning LED, each port includes one bi-color and one single color LED. Scan Bi-color mode compose of one 4x6 single color LED circuit matrix ，one 1x12 bi-color LED circuit matrix and two 1x6 scan bi-color LED circuit matrix. The output pin Scan Bi-color pin of the two (1x6) Scan Bi-color and the output pin scan_LED pin of the 4x6 single color are shared. The RTL8231 reach by the smart dynamic change mechanism.
In the Scan LED Bi-color, the SCAN_Bi-color high is lit the LED0, and the SCAN_Bi-color low is lit the LED1.

8.4.1. Smart Dynamic Change

In Scan Bi-color LED mode , the SCAN_LED pin to determine which LED to light a color, then through SCEN_STA to determine which Port needs to light up. As the Bi-color LED on the same port will not have the use of two kinds of colors also need to be turned on. Therefore, the period of the SCAN_LED could be divided into four equal parts, each time slot can simultaneously up to 4 port light LED, which is four time slot is automatically classified by RTL8231 between the different port must be lit in different color combinations. For example, when the port 0,2,4,5,11 need to light up bi-color Green while the other port needs light bi-color Yellow. Then the first and second time slot, when we let SCAN_LED for High, in a time slot for port 0,2,4,5 of SCEN_STA for Low light port 0,2,4,5 of the bi-color Green. Let the second time slot when port11's SCEN_STA for Low light port11 of the bi-color Green. The third and the fourth time slot, SCAN_LED compared to Low, in the allocation of the remaining port to light bi-color Yellow.

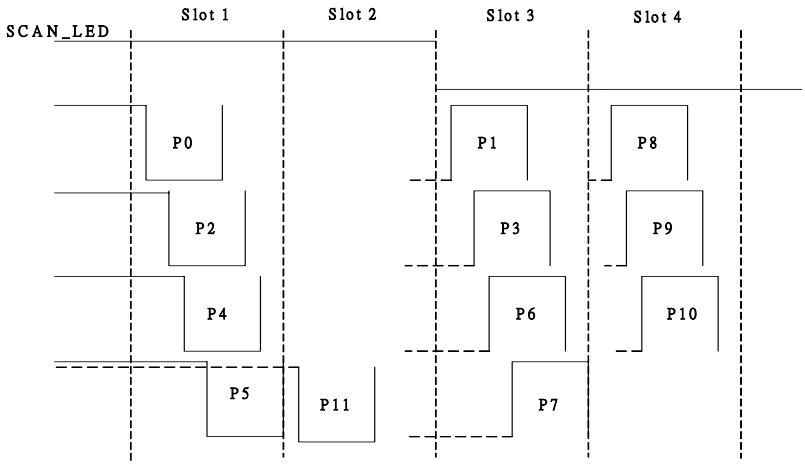

Figure 13, Smart Dynamic Change timing Diagram-1

8.4.2. SCAN Bi-color LED Mode Timing Diagram

The figure below is the first group Scan Bi-color LED, is the Matrix by a group composed of 1x12. The LED is used by Smart Dynamic Change mechanism, so can increase the Bi-color LED turn on time, in order to increase the Bi-color LED brightness.

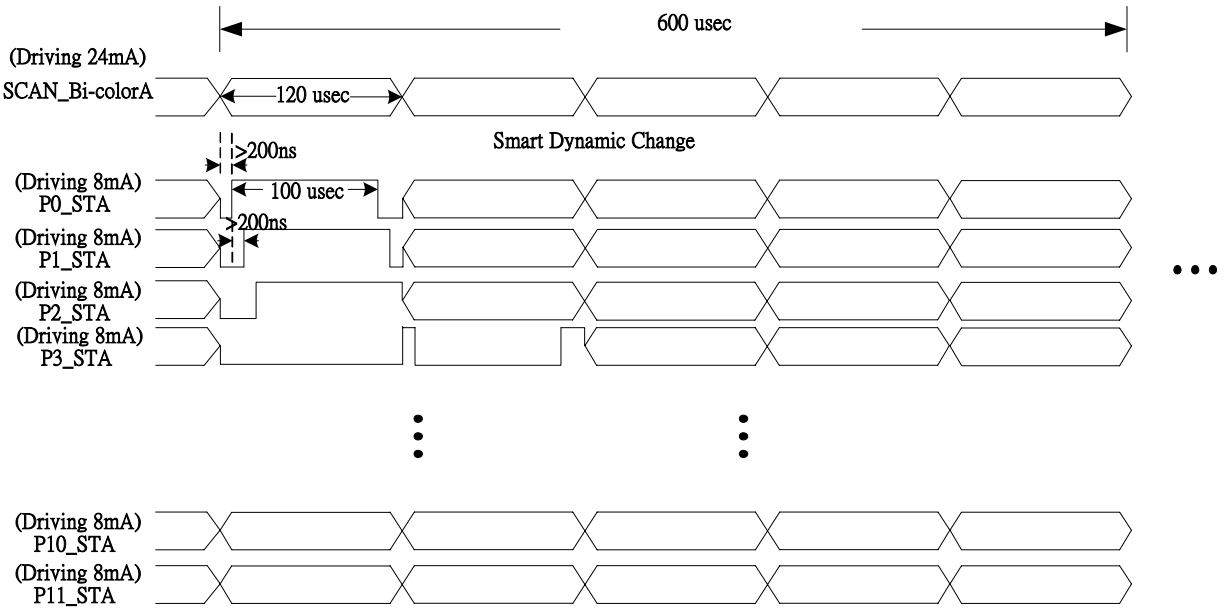

Figure 14, Scan LED Timing Diagram for Bi-color Mode, Bi-color Diagram 1

In the Bi-color LED Mode, the other two groups of bi-color LED is two 1x6's matrix, where 1 is the matrix of the SCAN_bi-color pin, and with the single color of the SCAN_LED pin sharing. The following figure is the Bi-color SCAN_LED into single color LED's SCAN_LED timing diagram, can be seen from the diagram belonging to the single color of the time slot, the P12_STA, P13_STA, ..., P17_STA will follow SCAN_P12-17_Bi-colorB change, and P18_STA , ..., P23_STA will follow SCAN_P18-23_Bi-colorC change, in order to avoid stealing Bi-color LED light.

In the single color LED connection, is a 4x6 = 24 single color. In the period of bi-color LED be lit, sharing the Pin SCAN_P12-17_Bi-colorB and SCAN_P18-23_Bi-colorC will be transformed into Smart Dynamic Change of status. At this time the all of single color SCAN_STA pins SCAN_STA_A, ..., SCAN_STA_F be maintained as the Low state. We can ensure that Bi-color status, it will not allow single color light.

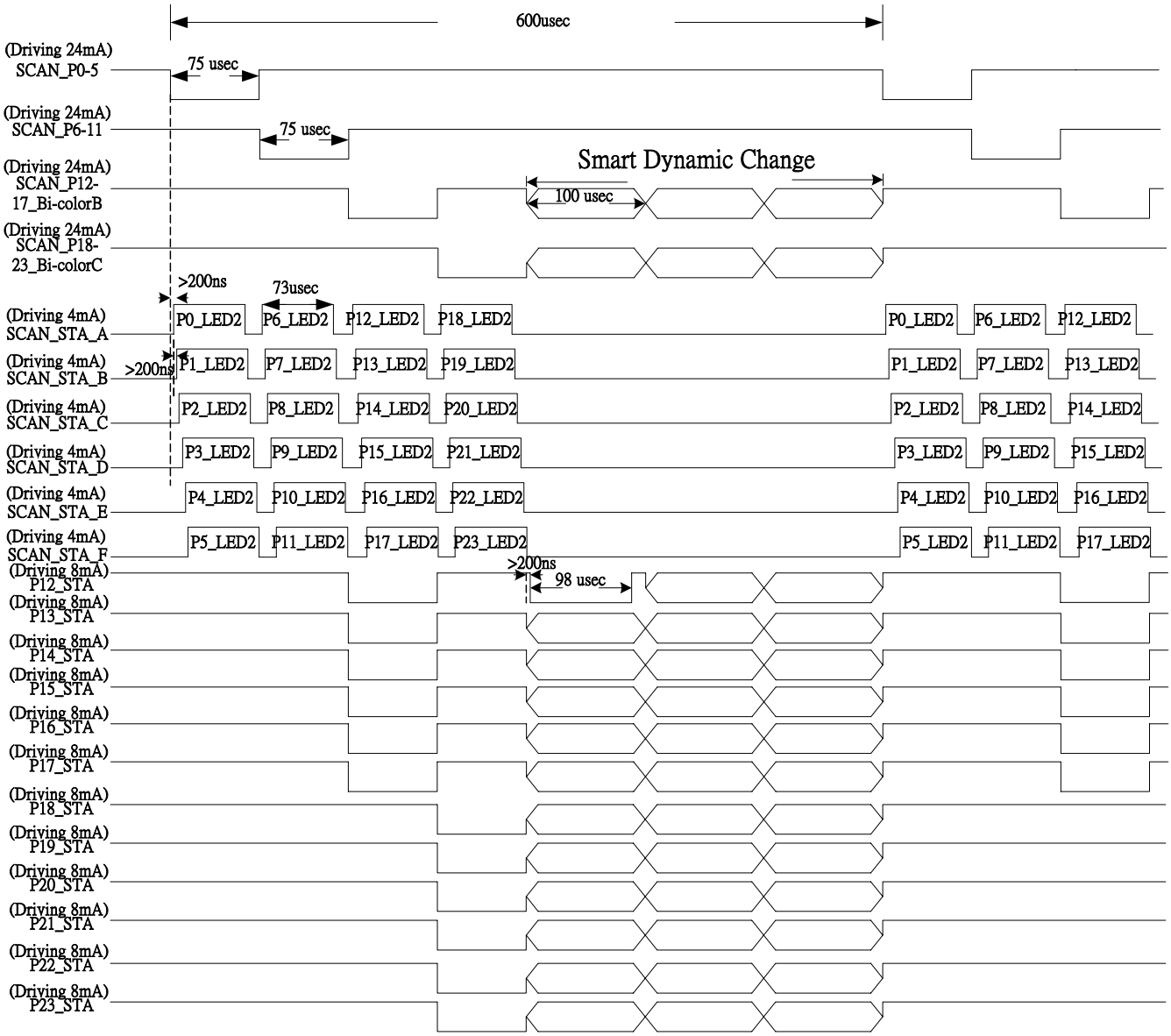

Figure 15, Scan LED Timing Diagram for Bi-color Mode, Single-color Diagram 2

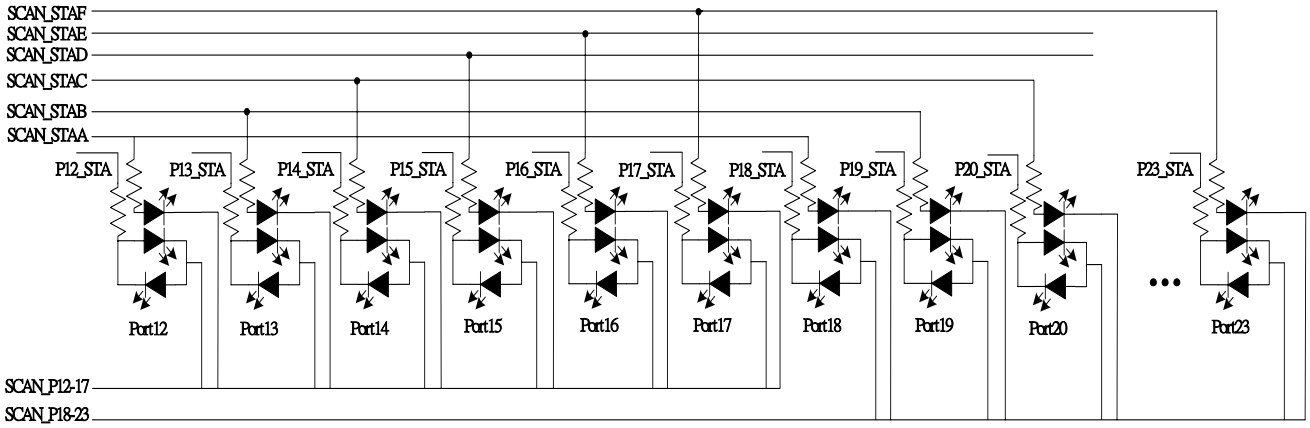

Figure 16, External Circuit for Bi-color Scan Mode

8.4.3. Scan Single Color Output Matrix Maps to Control Register

The scan single color output pins constitute the scan matrix. In each of cross line in the scan matrix, which maps to the LED control register is show below:

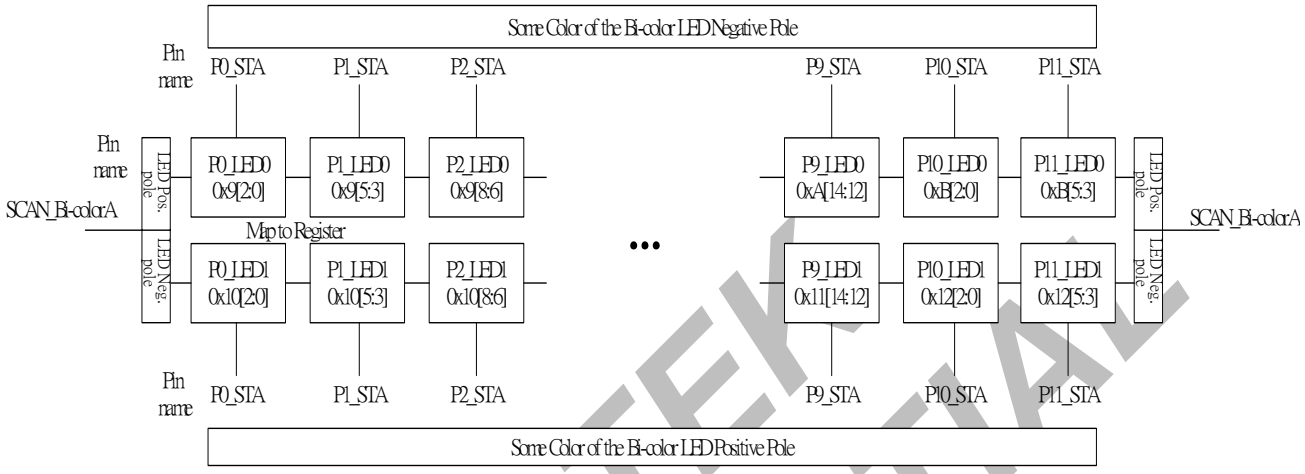

Figure 17, Scan Bi-color LED matrix maps to control register at group A.

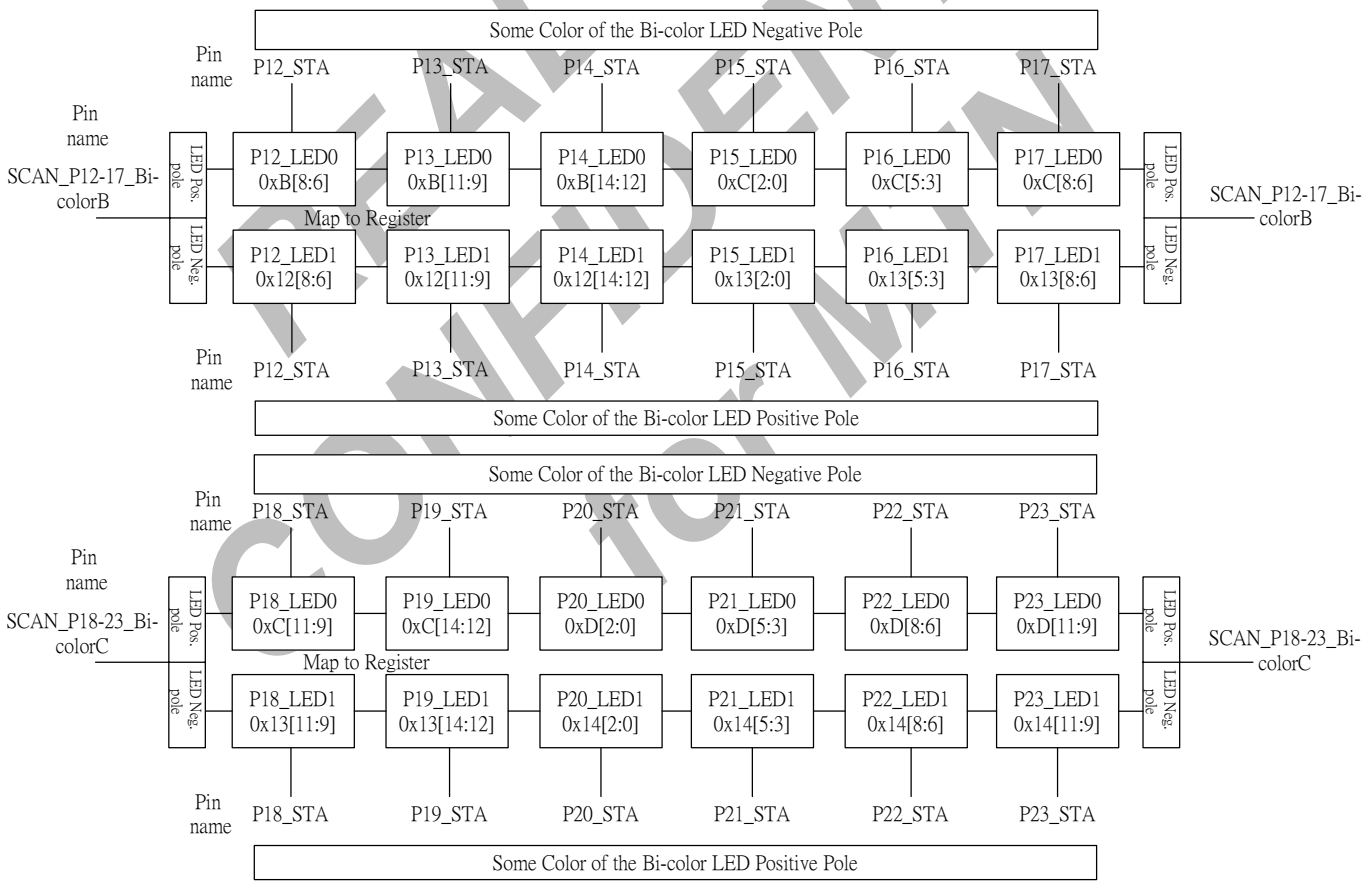

Figure 18, Scan Bi-color LED matrix maps to control register at group B.

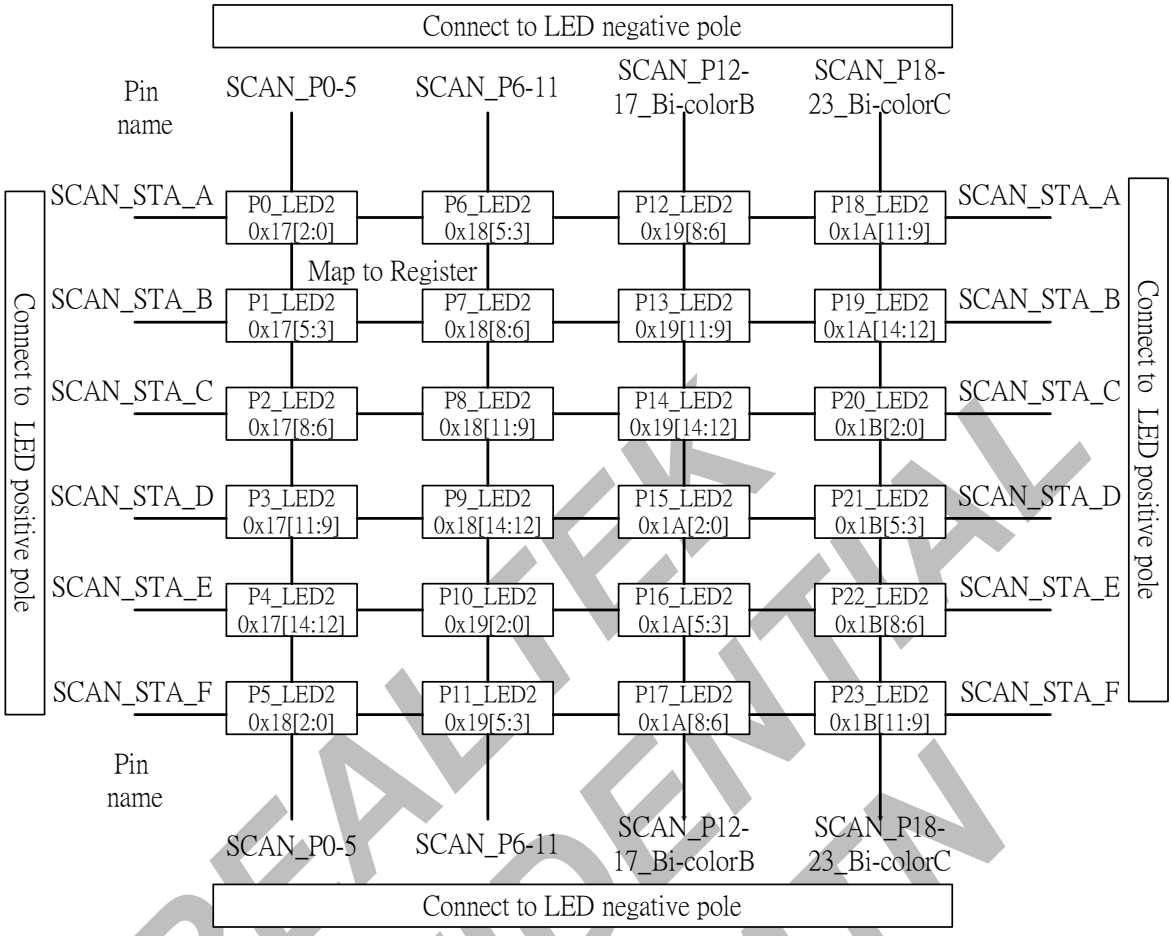

Figure 19, Scan Bi-color LED matrix maps to control register at group C.

8.5. GPIO Mode

In SMI mode, each of RTL8231 I/O pin could become the GPIO pin. The RTL8231 has the 37 GPIO pins which are set by register. The register 0x0002~0x0004 could select all I/O pins operate at the SCAN_LED mode or GPIO mode. The register 0x0004~0x0006 could select all of the GPIO are GPI or GPO.

8.5.1. Setting GPIO Pin Descriptions

In the SMI mode, the RTL8231 is allowed to choose each Pin whether or not to set GPIO or SCAN LED pin besides of the VCC / GND, Clock input, and the SMI Data input pin.

To Setting GPIO will be used by the Register as in the following shows:

- SEL_GPIO

Choose RTL8231 the use of Pin for SCAN LED or GPIO.
SEL_GPIO Register, when the Register value is 1'b0 indicates that the Pin for Scan LED. When the Register value is 1'b1, it said that the Pin for the GPIO Pin.

- IO_GPIO

When the Pin is set as a GPIO, the pin was input or output.
IO_GPIO Register, when the Register value is 1'b0, which the mapping SEL_GPIO value is 1'b1, said the GPIO pin as Output. When the Register value is 1'b1, which the mapping SEL_GPIO value is 1'b1, said the GPIO pin for the Input.

- INV_GPIO

When the Pin is set to GPO (output), it was decided Output data whether or not to inverse.
INV_GPIO Register, when the INV_GPIO Register value is 1'b1 which mapping the Pin was selected GPO, the Output data written to the data with the SMI contrast. The GPI (Input) is not affected by INV_GPIO. When INV_GPIO Register value is 1'b0, then the same.

- Buzzer_on

Only setting at Pin 15 GPIO [35]. The pin 15 is a general GPIO when Buzzer_on (0x0001 bit[3]) is set to 1'b0. When the Buzzer_on setting 1'b1, GPIO [35] was forced the output pin (ignore IO_GPIO [35] of the setting).At this moment, pin 15 will be sent to the frequency single for Buzzer. The frequency could set by the Buzzer_Freq [2:0] (0x0001 bits[2:0]) to decide.

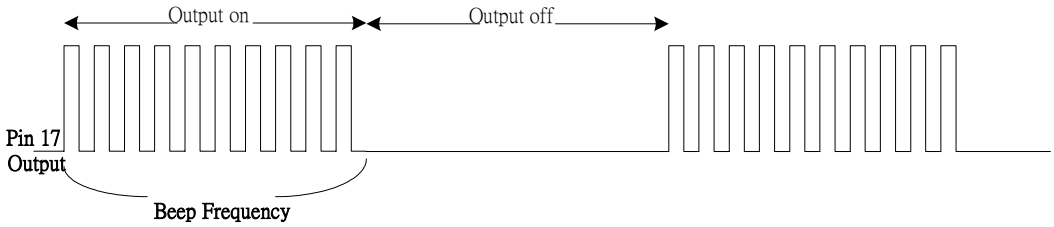

Figure 20, Buzzer signal Output

- En_Debouncing

When the Pin is set as a GPI state, the input signal required to continuously maintain the same status 100ms in order to be latch. Input data will be written in DATA_GPIO. Only part of the Pin can support En_Debouncing function. When the En_Debouncing is Enable, the corresponding Pin will be forced into GPI (input). At this moment, the corresponding register SEL_GPIO [X], and IO_GPIO [x] will be forced to write to 1'b1.

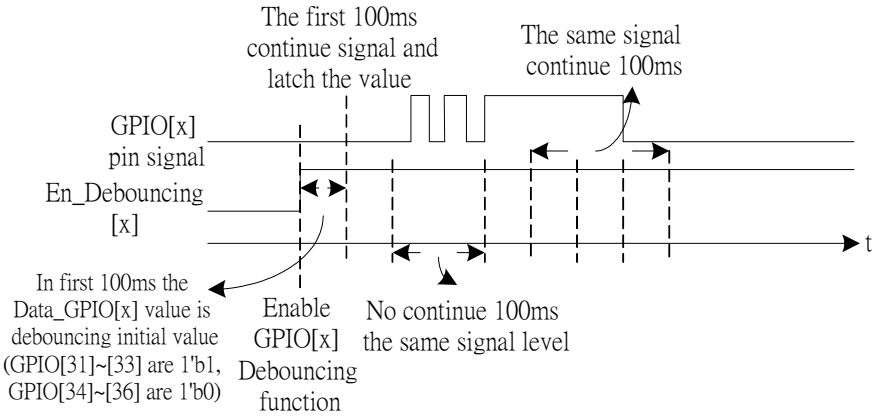

Figure 21, Dip Switch Debouncing

- 4mA_Driving

Each GPIO's output driving default driving current of 8mA. If you need to change the 4mA, you can set the 4mA_Driving (0x0000 bit[7]) register to 1'b1. This is a global register, all of the GPIO pin output driving current will be into 4mA when set to high.

- DATA_GPIO

DATA_GPIO Register, when the corresponding Pin was selected as GPIO, the GPIO is used to store the contents of the required output or input which the latch to the value.

9. Inter Register Description

Symbols:

R:	Read	V:	Configurable
W:	Write	P:	Partially Configurable
RW:	Read/Write	X:	Not Configurable

9.1. LED Mode System Configuration Register

In MDC/MDIO mode the Register table is at Page 30.
In SMI Slave mode the Register address are the same in the table Register Base Address column.

Register Base Address	Offset	Description	RW	Default	Pin
0x0000	0	En_bicolor 1'b0: Using single color LED, when in Scan LED mode. 1'b1: Using bi-color LED, when in Scan LED mode.	RW	1	-
	1	LED_Start When MAC setting RTL8231 ready MAC should write this bit 1'b1.	RW	0	
	2	PHY Address[0]/Device ID[0]	R	1	
	3	PHY Address[1]/Device ID[1]	R	1	
	4	PHY Address[2]/Device ID[2]	R	1	
	5	PHY Address[3]/16BIT_I2C	R	1	
	6	PHY Address[4]	R	1	
	7	4mA_Driving	RW	0	-
	8	All_light_LED0 (In the Scan LED Bi-color, the SCAN_Bi-color pin high is lit the LED0) 1'b1：all LED0 light	RW	0	-
	9	All_light_LED1 (In the Scan LED Bi-color, the SCAN_Bi-color pin low is lit the LED1. 1'b1：all LED1 light	RW	0	

Register Base Address	Offset	Description	RW	Default	Pin
	10	All_light_LED2 1'b1：all LED2 light	RW	0	
	11	All_blinking_LED0 1'b1：all LED0 blinking	RW	0	
	12	All_blinking_LED1 1'b1：all LED1 blinking	RW	0	
	13	All_blinking_LED2 1'b1：all LED2 blinking	RW	0	
	14	En_Sync_LED 1'b0：Scan LED output update status at real-time when LED status register value was be changed. (default value) 1'b1：Scan LED output only update status when 0x001B[15](Sync_LED) write to 1'b1.	RW	0	
	15	En_Sync_GPIO 1'b0：GPIO output update status at real-time when DATA_GPIO register value was be changed. (default value) 1'b1：GPIO output only update status when 0x001E[15](Sync_GPIO) write to 1'b1.	RW	0	

Register Base Address	Offset	Description	RW	Default	Pin
0x0001	2:0	Buzzer_Freq[2:0]	RW	1	-
		000:1.5K 011:3K 110:5K	RW	0	-
		001:2K(Default) 100:3.5K 111:6K 010:2.5K 101:4K *The frequency is depend on RC clock is 10Mhz.*	RW	0	-
	3	Buzzer_on(GPIO[35])	RW	0	-

Register Base Address	Offset	Description	RW	Default	Pin
	4	Ready_Code[0] The MAC can read the bit Ready_Code[5:0] value when LED_S2P is ready.	R	1	-
	5	Ready_Code[1]	R	1	-
	6	Ready_Code[2]	R	1	-
	7	Ready_Code[3]	R	0	-
	8	Ready_Code[4]	R	1	-
	9	Ready_Code[5]	R	1	-
	10	En_Debouncing[31]	RW	0	-
	11	En_Debouncing[32]	RW	0	-
	12	En_Debouncing[33]	RW	0	-
	13	En_Debouncing[34]	RW	0	-
	14	En_Debouncing[35]	RW	0	-
	15	En_Debouncing[36]	RW	0	-

Register Base Address	Offset	Description	RW	Default	Pin
0x0002	0	SEL_GPIO[0]	RW	0	-
	1	SEL_GPIO[1]	RW	0	-
	2	SEL_GPIO[2]	RW	0	-
	3	SEL_GPIO[3]	RW	0	-
	4	SEL_GPIO[4]	RW	0	-
	5	SEL_GPIO[5]	RW	0	-
	6	SEL_GPIO[6]	RW	0	-
	7	SEL_GPIO[7]	RW	0	-
	8	SEL_GPIO[8]	RW	0	-
	9	SEL_GPIO[9]	RW	0	-
	10	SEL_GPIO[10]	RW	0	-
	11	SEL_GPIO[11]	RW	0	-
	12	SEL_GPIO[12]	RW	0	-

Register Base Address	Offset	Description	RW	Default	Pin
	13	SEL_GPIO[13]	RW	0	-
	14	SEL_GPIO[14]	RW	0	-
	15	SEL_GPIO[15]	RW	0	-
Register Base Address	**Offset**	**Description**	**RW**	**Default**	**Pin**
0x0003	0	SEL_GPIO[16]	RW	0	-
	1	SEL_GPIO[17]	RW	0	-
	2	SEL_GPIO[18]	RW	0	-
	3	SEL_GPIO[19]	RW	0	-
	4	SEL_GPIO[20]	RW	0	-
	5	SEL_GPIO[21]	RW	0	-
	6	SEL_GPIO[22]	RW	1	-
	7	SEL_GPIO[23]	RW	0	-
	8	SEL_GPIO[24]	RW	0	-
	9	SEL_GPIO[25]	RW	0	-
	10	SEL_GPIO[26]	RW	0	-
	11	SEL_GPIO[27]	RW	1	-
	12	SEL_GPIO[28]	RW	1	-
	13	SEL_GPIO[29]	RW	1	-
	14	SEL_GPIO[30]	RW	1	-
	15	SEL_GPIO[31]	RW	1	-

Register Base Address	Offset	Description	RW	Default	Pin
0x0004	0	SEL_GPIO[32]	RW	1	-
	1	SEL_GPIO[33]	RW	1	-
	2	SEL_GPIO[34]	RW	1	-
	3	**Reserved**	RW	1	-
	4	**Reserved**	RW	1	-

Register Base Address	Offset	Description	RW	Default	Pin
	5	IO_GPIO[32] I/O Masker	RW	0	-
	6	IO_GPIO[33] I/O Masker	RW	0	-
	7	IO_GPIO[34] I/O Masker	RW	0	-
	8	IO_GPIO[35] I/O Masker	RW	0	-
	9	IO_GPIO[36] I/O Masker	RW	0	-
	10	INV_GPIO[32]	RW	0	-
	11	INV_GPIO[33]	RW	0	-
	12	INV_GPIO[34]	RW	0	-
	13	INV_GPIO[35]	RW	0	-
	14	INV_GPIO[36]	RW	0	-
	15	Software Reset	RW/SC	0	-

Register Base Address	Offset	Description	RW	Default	Pin
0x0005	0	IO_GPIO[0] I/O Masker	RW	0	-
	1	IO_GPIO[1] I/O Masker	RW	0	-
	2	IO_GPIO[2] I/O Masker	RW	0	-
	3	IO_GPIO[3] I/O Masker	RW	0	-
	4	IO_GPIO[4] I/O Masker	RW	0	-
	5	IO_GPIO[5] I/O Masker	RW	0	-
	6	IO_GPIO[6] I/O Masker	RW	0	-
	7	IO_GPIO[7] I/O Masker	RW	0	-
	8	IO_GPIO[8] I/O Masker	RW	0	-
	9	IO_GPIO[9] I/O Masker	RW	0	-
	10	IO_GPIO[10] I/O Masker	RW	0	-
	11	IO_GPIO[11] I/O Masker	RW	0	-
	12	IO_GPIO[12] I/O Masker	RW	0	-
	13	IO_GPIO[13] I/O Masker	RW	0	-
	14	IO_GPIO[14] I/O Masker	RW	0	-
	15	IO_GPIO[15] I/O Masker	RW	0	-

Register Base Address	Offset	Description	RW	Default	Pin
Register Base Address	Offset	Description	RW	Default	Pin
0x0006	0	IO_GPIO[16] I/O Masker	RW	0	-
	1	IO_GPIO[17] I/O Masker	RW	0	-
	2	IO_GPIO[18] I/O Masker	RW	0	-
	3	IO_GPIO[19] I/O Masker	RW	0	-
	4	IO_GPIO[20] I/O Masker	RW	0	-
	5	IO_GPIO[21] I/O Masker	RW	0	-
	6	IO_GPIO[22] I/O Masker	RW	0	-
	7	IO_GPIO[23] I/O Masker	RW	0	-
	8	IO_GPIO[24] I/O Masker	RW	0	-
	9	IO_GPIO[25] I/O Masker	R	0	-
	10	IO_GPIO[26] I/O Masker	R	0	-
	11	IO_GPIO[27] I/O Masker	R	0	-
	12	IO_GPIO[28] I/O Masker	R	0	-
	13	IO_GPIO[29] I/O Masker	R	0	-
	14	IO_GPIO[30] I/O Masker	R	0	-
	15	IO_GPIO[31] I/O Masker	R	0	-

Register Base Address	Offset	Description	RW	Default	Pin
0x0007	0	INV_GPIO[0] Inverter Masker	RW	0	-
	1	INV_GPIO[1] Inverter Masker	RW	0	-
	2	INV_GPIO[2] Inverter Masker	RW	0	-
	3	INV_GPIO[3] Inverter Masker	RW	0	-
	4	INV_GPIO[4] Inverter Masker	RW	0	-
	5	INV_GPIO[5] Inverter Masker	RW	0	-
	6	INV_GPIO[6] Inverter Masker	RW	0	-
	7	INV_GPIO[7] Inverter Masker	RW	0	-

Register Base Address	Offset	Description	RW	Default	Pin
	8	INV_GPIO[8] Inverter Masker	RW	0	-
	9	INV_GPIO[9] Inverter Masker	RW	0	-
	10	INV_GPIO[10] Inverter Masker	RW	0	-
	11	INV_GPIO[11] Inverter Masker	RW	0	-
	12	INV_GPIO[12] Inverter Masker	RW	0	-
	13	INV_GPIO[13] Inverter Masker	RW	0	-
	14	INV_GPIO[14] Inverter Masker	RW	0	-
	15	INV_GPIO[15] Inverter Masker	RW	0	-

Register Base Address	Offset	Description	RW	Default	Pin
0x0008	0	INV_GPIO[16] Inverter Masker	RW	0	-
	1	INV_GPIO[17] Inverter Masker	RW	0	-
	2	INV_GPIO[18] Inverter Masker	RW	0	-
	3	INV_GPIO[19] Inverter Masker	RW	0	-
	4	INV_GPIO[20] Inverter Masker	RW	0	-
	5	INV_GPIO[21] Inverter Masker	RW	0	-
	6	INV_GPIO[22] Inverter Masker	RW	0	-
	7	INV_GPIO[23] Inverter Masker	RW	0	-
	8	INV_GPIO[24] Inverter Masker	RW	0	-
	9	INV_GPIO[25] Inverter Masker	RW	0	-
	10	INV_GPIO[26] Inverter Masker	RW	0	-
	11	INV_GPIO[27] Inverter Masker	RW	0	-
	12	INV_GPIO[28] Inverter Masker	RW	0	-
	13	INV_GPIO[29] Inverter Masker	RW	0	-
	14	INV_GPIO[30] Inverter Masker	RW	0	-
	15	INV_GPIO[31] Inverter Masker	RW	0	-

Register Base Address	Offset	Description	RW	Default	Pin
0x0009	2:0	Port0_LED0_[2:0]	RW	0	-
	1	000：off 011：blinking 128ms	RW	0	-
	2	111：light 100：blinking 256ms 001：blinking 32ms 101：blinking 512ms 010：blinking 64ms 110：blinking 1024ms	RW	0	-
	3	Port1_LED0_[0] (In the Scan LED Bi-color, the SCAN_Bi-color pin high is lit the LED0)	RW	0	-
	4	Port1_LED0_[1]	RW	0	-
	5	Port1_LED0_[2]	RW	0	-
	6	Port2_LED0_[0]	RW	0	-
	7	Port2_LED0_[1]	RW	0	-
	8	Port2_LED0_[2]	RW	0	-
	9	Port3_LED0_[0]	RW	0	-
	10	Port3_LED0_[1]	RW	0	-
	11	Port3_LED0_[2]	RW	0	-
	12	Port4_LED0_[0]	RW	0	-
	13	Port4_LED0_[1]	RW	0	-
	14	Port4_LED0_[2]	RW	0	-
	15	**Reserved**	RW	0	-

Register Base Address	Offset	Description	RW	Default	Pin
0x000A	0	Port5_LED0_[0]	RW	0	-
	1	Port5_LED0_[1]	RW	0	-
	2	Port5_LED0_[2]	RW	0	-
	3	Port6_LED0_[0]	RW	0	-
	4	Port6_LED0_[1]	RW	0	-
	5	Port6_LED0_[2]	RW	0	-
	6	Port7_LED0_[0]	RW	0	-

Register Base Address	Offset	Description	RW	Default	Pin
	7	Port7_LED0_[1]	RW	0	-
	8	Port7_LED0_[2]	RW	0	-
	9	Port8_LED0_[0]	RW	0	-
	10	Port8_LED0_[1]	RW	0	-
	11	Port8_LED0_[2]	RW	0	-
	12	Port9_LED0_[0]	RW	0	-
	13	Port9_LED0_[1]	RW	0	-
	14	Port9_LED0_[2]	RW	0	-
	15	**Reserved**	RW	0	-

Register Base Address	Offset	Description	RW	Default	Pin
0x000B	0	Port10_LED0_[0]	RW	0	-
	1	Port10_LED0_[1]	RW	0	-
	2	Port10_LED0_[2]	RW	0	-
	3	Port11_LED0_[0]	RW	0	-
	4	Port11_LED0_[1]	RW	0	-
	5	Port11_LED0_[2]	RW	0	-
	6	Port12_LED0_[0]	RW	0	-
	7	Port12_LED0_[1]	RW	0	-
	8	Port12_LED0_[2]	RW	0	-
	9	Port13_LED0_[0]	RW	0	-
	10	Port13_LED0_[1]	RW	0	-
	11	Port13_LED0_[2]	RW	0	-
	12	Port14_LED0_[0]	RW	0	-
	13	Port14_LED0_[1]	RW	0	-
	14	Port14_LED0_[2]	RW	0	-
	15	**Reserved**	RW	0	-

Register Base Address	Offset	Description	RW	Default	Pin
0x000C	0	Port15_LED0_[0]	RW	0	-
	1	Port15_LED0_[1]	RW	0	-
	2	Port15_LED0_[2]	RW	0	-
	3	Port16_LED0_[0]	RW	0	-
	4	Port16_LED0_[1]	RW	0	-
	5	Port16_LED0_[2]	RW	0	-
	6	Port17_LED0_[0]	RW	0	-
	7	Port17_LED0_[1]	RW	0	-
	8	Port17_LED0_[2]	RW	0	-
	9	Port18_LED0_[0]	RW	0	-
	10	Port18_LED0_[1]	RW	0	-
	11	Port18_LED0_[2]	RW	0	-
	12	Port19_LED0_[0]	RW	0	-
	13	Port19_LED0_[1]	RW	0	-
	14	Port19_LED0_[2]	RW	0	-
	15	**Reserved**	RW	0	-

Register Base Address	Offset	Description	RW	Default	Pin
0x000D	0	Port20_LED0_[0]	RW	0	-
	1	Port20_LED0_[1]	RW	0	-
	2	Port20_LED0_[2]	RW	0	-
	3	Port21_LED0_[0]	RW	0	-
	4	Port21_LED0_[1]	RW	0	-
	5	Port21_LED0_[2]	RW	0	-
	6	Port22_LED0_[0]	RW	0	-
	7	Port22_LED0_[1]	RW	0	-
	8	Port22_LED0_[2]	RW	0	-
	9	Port23_LED0_[0]	RW	0	-
	10	Port23_LED0_[1]	RW	0	-

Register Base Address	Offset	Description	RW	Default	Pin
	11	Port23_LED0_[2]	RW	0	-
	12	Port24_LED0_[0]	RW	0	-
	13	Port24_LED0_[1]	RW	0	-
	14	Port24_LED0_[2]	RW	0	-
	15	**Reserved**	RW	0	-

Register Base Address	Offset	Description	RW	Default	Pin
0x000E	0	Port25_LED0_[0]	RW	0	-
	1	Port25_LED0_[1]	RW	0	-
	2	Port25_LED0_[2]	RW	0	-
	3	Port26_LED0_[0]	RW	0	-
	4	Port26_LED0_[1]	RW	0	-
	5	Port26_LED0_[2]	RW	0	-
	6	Port27_LED0_[0]	RW	0	-
	7	Port27_LED0_[1]	RW	0	-
	8	Port27_LED0_[2]	RW	0	-
	9	Port28_LED0_[0]	RW	0	-
	10	Port28_LED0_[1]	RW	0	-
	11	Port28_LED0_[2]	RW	0	-
	12	Port29_LED0_[0]	RW	0	-
	13	Port29_LED0_[1]	RW	0	-
	14	Port29_LED0_[2]	RW	0	-
	15	**Reserved**	RW	0	-

Register Base Address	Offset	Description	RW	Default	Pin
0x000F	0	Port30_LED0_[0]	RW	0	-
	1	Port30_LED0_[1]	RW	0	-
	2	Port30_LED0_[2]	RW	0	-
	3	Port31_LED0_[0]	RW	0	-
	4	Port31_LED0_[1]	RW	0	-
	5	Port31_LED0_[2]	RW	0	-
	6	**Reserved**	RW	0	-
	7	**Reserved**	RW	0	-
	8	**Reserved**	RW	0	-
	9	**Reserved**	RW	0	-
	10	**Reserved**	RW	0	-
	11	**Reserved**	RW	0	-
	12	**Reserved**	RW	0	-
	13	**Reserved**	RW	0	-
	14	**Reserved**	RW	0	-
	15	**Reserved**	RW	0	-

Register Base Address	Offset	Description	RW	Default	Pin
0x0010	0	Port0_LED1_[0] (In the Scan LED Bi-color, the SCAN_Bi-color pin low is lit the LED1)	RW	0	-
	1	Port0_LED1_[1]	RW	0	-
	2	Port0_LED1_[2]	RW	0	-
	3	Port1_LED1_[0]	RW	0	-
	4	Port1_LED1_[1]	RW	0	-
	5	Port1_LED1_[2]	RW	0	-
	6	Port2_LED1_[0]	RW	0	-
	7	Port2_LED1_[1]	RW	0	-

Register Base Address	Offset	Description	RW	Default	Pin
	8	Port2_LED1_[2]	RW	0	-
	9	Port3_LED1_[0]	RW	0	-
	10	Port3_LED1_[1]	RW	0	-
	11	Port3_LED1_[2]	RW	0	-
	12	Port4_LED1_[0]	RW	0	-
	13	Port4_LED1_[1]	RW	0	-
	14	Port4_LED1_[2]	RW	0	-
	15	**Reserved**	RW	0	-

Register Base Address	Offset	Description	RW	Default	Pin
0x0011	0	Port5_LED1_[0]	RW	0	-
	1	Port5_LED1_[1]	RW	0	-
	2	Port5_LED1_[2]	RW	0	-
	3	Port6_LED1_[0]	RW	0	-
	4	Port6_LED1_[1]	RW	0	-
	5	Port6_LED1_[2]	RW	0	-
	6	Port7_LED1_[0]	RW	0	-
	7	Port7_LED1_[1]	RW	0	-
	8	Port7_LED1_[2]	RW	0	-
	9	Port8_LED1_[0]	RW	0	-
	10	Port8_LED1_[1]	RW	0	-
	11	Port8_LED1_[2]	RW	0	-
	12	Port9_LED1_[0]	RW	0	-
	13	Port9_LED1_[1]	RW	0	-
	14	Port9_LED1_[2]	RW	0	-
	15	**Reserved**	RW	0	-

Register Base Address	Offset	Description	RW	Default	Pin
0x0012	0	Port10_LED1_[0]	RW	0	-
	1	Port10_LED1_[1]	RW	0	-
	2	Port10_LED1_[2]	RW	0	-
	3	Port11_LED1_[0]	RW	0	-
	4	Port11_LED1_[1]	RW	0	-
	5	Port11_LED1_[2]	RW	0	-
	6	Port12_LED1_[0]	RW	0	-
	7	Port12_LED1_[1]	RW	0	-
	8	Port12_LED1_[2]	RW	0	-
	9	Port13_LED1_[0]	RW	0	-
	10	Port13_LED1_[1]	RW	0	-
	11	Port13_LED1_[2]	RW	0	-
	12	Port14_LED1_[0]	RW	0	-
	13	Port14_LED1_[1]	RW	0	-
	14	Port14_LED1_[2]	RW	0	-
	15	**Reserved**	RW	0	-

Register Base Address	Offset	Description	RW	Default	Pin
0x0013	0	Port15_LED1_[0]	RW	0	-
	1	Port15_LED1_[1]	RW	0	-
	2	Port15_LED1_[2]	RW	0	-
	3	Port16_LED1_[0]	RW	0	-
	4	Port16_LED1_[1]	RW	0	-
	5	Port16_LED1_[2]	RW	0	-
	6	Port17_LED1_[0]	RW	0	-
	7	Port17_LED1_[1]	RW	0	-
	8	Port17_LED1_[2]	RW	0	-
	9	Port18_LED1_[0]	RW	0	-
	10	Port18_LED1_[1]	RW	0	-

Register Base Address	Offset	Description	RW	Default	Pin
	11	Port18_LED1_[2]	RW	0	-
	12	Port19_LED1_[0]	RW	0	-
	13	Port19_LED1_[1]	RW	0	-
	14	Port19_LED1_[2]	RW	0	-
	15	**Reserved**	RW	0	-

Register Base Address	Offset	Description	RW	Default	Pin
0x0014	0	Port20_LED1_[0]	RW	0	-
	1	Port20_LED1_[1]	RW	0	-
	2	Port20_LED1_[2]	RW	0	-
	3	Port21_LED1_[0]	RW	0	-
	4	Port21_LED1_[1]	RW	0	-
	5	Port21_LED1_[2]	RW	0	-
	6	Port22_LED1_[0]	RW	0	-
	7	Port22_LED1_[1]	RW	0	-
	8	Port22_LED1_[2]	RW	0	-
	9	Port23_LED1_[0]	RW	0	-
	10	Port23_LED1_[1]	RW	0	-
	11	Port23_LED1_[2]	RW	0	-
	12	Port24_LED1_[0]	RW	0	-
	13	Port24_LED1_[1]	RW	0	-
	14	Port24_LED1_[2]	RW	0	-
	15	**Reserved**	RW	0	-

Register Base Address	Offset	Description	RW	Default	Pin
0x0015	0	Port25_LED1_[0]	RW	0	-
	1	Port25_LED1_[1]	RW	0	-
	2	Port25_LED1_[2]	RW	0	-
	3	Port26_LED1_[0]	RW	0	-
	4	Port26_LED1_[1]	RW	0	-
	5	Port26_LED1_[2]	RW	0	-
	6	Port27_LED1_[0]	RW	0	-
	7	Port27_LED1_[1]	RW	0	-
	8	Port27_LED1_[2]	RW	0	-
	9	Port28_LED1_[0]	RW	0	-
	10	Port28_LED1_[1]	RW	0	-
	11	Port28_LED1_[2]	RW	0	-
	12	Port29_LED1_[0]	RW	0	-
	13	Port29_LED1_[1]	RW	0	-
	14	Port29_LED1_[2]	RW	0	-
	15	**Reserved**	RW	0	-

Register Base Address	Offset	Description	RW	Default	Pin
0x0016	0	Port30_LED1_[0]	RW	0	-
	1	Port30_LED1_[1]	RW	0	-
	2	Port30_LED1_[2]	RW	0	-
	3	Port31_LED1_[0]	RW	0	-
	4	Port31_LED1_[1]	RW	0	-
	5	Port31_LED1_[2]	RW	0	-
	6	**Reserved**	RW	0	-
	7	**Reserved**	RW	0	-
	8	**Reserved**	RW	0	-
	9	**Reserved**	RW	0	-
	10	**Reserved**	RW	0	-

Register Base Address	Offset	Description	RW	Default	Pin
	11	**Reserved**	RW	0	-
	12	**Reserved**	RW	0	-
	13	**Reserved**	RW	0	-
	14	**Reserved**	RW	0	-
	15	**Reserved**	RW	0	-

Register Base Address	Offset	Description	RW	Default	Pin
0x0017	0	Port0_LED2_[0]	RW	0	-
	1	Port0_LED2_[1]	RW	0	-
	2	Port0_LED2_[2]	RW	0	-
	3	Port1_LED2_[0]	RW	0	-
	4	Port1_LED2_[1]	RW	0	-
	5	Port1_LED2_[2]	RW	0	-
	6	Port2_LED2_[0]	RW	0	-
	7	Port2_LED2_[1]	RW	0	-
	8	Port2_LED2_[2]	RW	0	-
	9	Port3_LED2_[0]	RW	0	-
	10	Port3_LED2_[1]	RW	0	-
	11	Port3_LED2_[2]	RW	0	-
	12	Port4_LED2_[0]	RW	0	-
	13	Port4_LED2_[1]	RW	0	-
	14	Port4_LED2_[2]	RW	0	-
	15	**Reserved**	RW	0	-

Register Base Address	Offset	Description	RW	Default	Pin
0x0018	0	Port5_LED2_[0]	RW	0	-
	1	Port5_LED2_[1]	RW	0	-
	2	Port5_LED2_[2]	RW	0	-
	3	Port6_LED2_[0]	RW	0	-
	4	Port6_LED2_[1]	RW	0	-
	5	Port6_LED2_[2]	RW	0	-
	6	Port7_LED2_[0]	RW	0	-
	7	Port7_LED2_[1]	RW	0	-
	8	Port7_LED2_[2]	RW	0	-
	9	Port8_LED2_[0]	RW	0	-
	10	Port8_LED2_[1]	RW	0	-
	11	Port8_LED2_[2]	RW	0	-
	12	Port9_LED2_[0]	RW	0	-
	13	Port9_LED2_[1]	RW	0	-
	14	Port9_LED2_[2]	RW	0	-
	15	**Reserved**	RW	0	-

Register Base Address	Offset	Description	RW	Default	Pin
0x0019	0	Port10_LED2_[0]	RW	0	-
	1	Port10_LED2_[1]	RW	0	-
	2	Port10_LED2_[2]	RW	0	-
	3	Port11_LED2_[0]	RW	0	-
	4	Port11_LED2_[1]	RW	0	-
	5	Port11_LED2_[2]	RW	0	-
	6	Port12_LED2_[0]	RW	0	-
	7	Port12_LED2_[1]	RW	0	-
	8	Port12_LED2_[2]	RW	0	-
	9	Port13_LED2_[0]	RW	0	-
	10	Port13_LED2_[1]	RW	0	-

Register Base Address	Offset	Description	RW	Default	Pin
	11	Port13_LED2_[2]	RW	0	-
	12	Port14_LED2_[0]	RW	0	-
	13	Port14_LED2_[1]	RW	0	-
	14	Port14_LED2_[2]	RW	0	-
	15	**Reserved**	RW	0	-

Register Base Address	Offset	Description	RW	Default	Pin
0x001A	0	Port15_LED2_[0]	RW	0	-
	1	Port15_LED2_[1]	RW	0	-
	2	Port15_LED2_[2]	RW	0	-
	3	Port16_LED2_[0]	RW	0	-
	4	Port16_LED2_[1]	RW	0	-
	5	Port16_LED2_[2]	RW	0	-
	6	Port17_LED2_[0]	RW	0	-
	7	Port17_LED2_[1]	RW	0	-
	8	Port17_LED2_[2]	RW	0	-
	9	Port18_LED2_[0]	RW	0	-
	10	Port18_LED2_[1]	RW	0	-
	11	Port18_LED2_[2]	RW	0	-
	12	Port19_LED2_[0]	RW	0	-
	13	Port19_LED2_[1]	RW	0	-
	14	Port19_LED2_[2]	RW	0	-
	15	**Reserved**	RW	0	-

Register Base Address	Offset	Description	RW	Default	Pin
0x001B	0	Port20_LED2_[0]	RW	0	-
	1	Port20_LED2_[1]	RW	0	-
	2	Port20_LED2_[2]	RW	0	-
	3	Port21_LED2_[0]	RW	0	-
	4	Port21_LED2_[1]	RW	0	-
	5	Port21_LED2_[2]	RW	0	-
	6	Port22_LED2_[0]	RW	0	-
	7	Port22_LED2_[1]	RW	0	-
	8	Port22_LED2_[2]	RW	0	-
	9	Port23_LED2_[0]	RW	0	-
	10	Port23_LED2_[1]	RW	0	-
	11	Port23_LED2_[2]	RW	0	-
	12:14	**Reserved**	RW	0	-
	15	Sync_LED	RW/SC	0	-

Register Base Address	Offset	Description	RW	Default	Pin
0x001C	0	DATA_GPIO[0]	RW	0	-
	1	DATA_GPIO[1]	RW	0	-
	2	DATA_GPIO[2]	RW	0	-
	3	DATA_GPIO[3]	RW	0	-
	4	DATA_GPIO[4]	RW	0	-
	5	DATA_GPIO[5]	RW	0	-
	6	DATA_GPIO[6]	RW	0	-
	7	DATA_GPIO[7]	RW	0	-
	8	DATA_GPIO[8]	RW	0	-
	9	DATA_GPIO[9]	RW	0	-
	10	DATA_GPIO[10]	RW	0	-
	11	DATA_GPIO[11]	RW	0	-
	12	DATA_GPIO[12]	RW	0	-

Register Base Address	Offset	Description	RW	Default	Pin
	13	DATA_GPIO[13]	RW	0	-
	14	DATA_GPIO[14]	RW	0	-
	15	DATA_GPIO[15]	RW	0	-

Register Base Address	Offset	Description	RW	Default	Pin
0x001D	0	DATA_GPIO[16]	RW	0	-
	1	DATA_GPIO[17]	RW	0	-
	2	DATA_GPIO[18]	RW	0	-
	3	DATA_GPIO[19]	RW	0	-
	4	DATA_GPIO[20]	RW	0	-
	5	DATA_GPIO[21]	RW	0	-
	6	DATA_GPIO[22]	RW	0	-
	7	DATA_GPIO[23]	RW	0	-
	8	DATA_GPIO[24]	RW	0	-
	9	DATA_GPIO[25]	RW	0	-
	10	DATA_GPIO[26]	RW	0	-
	11	DATA_GPIO[27]	RW	0	-
	12	DATA_GPIO[28]	RW	0	-
	13	DATA_GPIO[29]	RW	0	-
	14	DATA_GPIO[30]	RW	0	-
	15	DATA_GPIO[31]	RW	0	-

Register Base Address	Offset	Description	RW	Default	Pin
0x001E	0	DATA_GPIO[32]	RW	0	-
	1	DATA_GPIO[33]	RW	0	-
	2	DATA_GPIO[34]	RW	0	-
	3	DATA_GPIO[35]	RW	0	-

Register Base Address	Offset	Description	RW	Default	Pin
	4	DATA_GPIO[36]	RW	0	-
	5	**Reserved**	RW	0	-
	6	**Reserved**	RW	0	-
	7	**Reserved**	RW	0	-
	8	**Reserved**	RW	0	-
	9	**Reserved**	RW	0	-
	10	**Reserved**	RW	0	-
	11	**Reserved**	RW	0	-
	12	**Reserved**	RW	0	-
	13	**Reserved**	RW	0	-
	14	**Reserved**	RW	0	-
	15	Sync_GPIO	RW/SC	0	-

10. Electrical Characteristics

10.1. Absolute Maximum Ratings

WARNING: Absolute maximum ratings are limits beyond which permanent damage may be caused to the device, or device reliability will be affected. All voltages are specified reference to GND unless otherwise specified.

Table 14. Absolute Maximum Ratings

Parameter	Min	Max	Units
Junction Temperature (Tj)	-	+125	°C
Storage Temperature	-45	+125	°C
VDD Supply Referenced to GND	GND-0.3	+3.63	V
Digital Input Voltage	GND-0.3	VDD+0.3	V

10.2. Recommended Operating Range

Table 15. Recommended Operating Range

Parameter	Min	Typical	Max	Units
Ambient Operating Temperature (Ta)	0	-	70	°C
VDD Supply Voltage Range	3.135	3.3	3.465	V

10.3. Thermal Characteristics

Assembly Description

Table 16. Assembly Description

Package	Type	LQFP-48
	Dimension (L x W)	7 x 7mm
	Thickness	0.27mm
PCB	PCB Dimension (L x W)	81mm^2
	PCB Thickness	1.6mm

	Number of Cu Layer-PCB	2 layers (2S): -Top layer: 20% coverage of Cu -Bottom layer: 75% coverage of Cu 4 layers (2S2P): -1st layer: 20% coverage of Cu -2nd layer: 80% coverage of Cu -3rd layer: 80% coverage of Cu -4th layer: 75% coverage of Cu

Material Properties

Table 17. Material Properties

Item		Material	Thermal Conductivity K (W/m-k)
Package	Die	Si	147
	Silver Paste	1033BF	1.5
	Lead Frame	CDA7025	168
	Mold Compound	7372	0.92
PCB		Cu	400
		FR4	0.2

10.3.1. Shift Register mode

Simulation Conditions

Table 18. Simulation Conditions

Input Power	435.6 mW
Test Board (PCB)	2L (2S) / 4L (2S2P)
Control Condition	Air Flow = 0, 1, 2, 3 m/s

Thermal Performance of E-Pad LQFP-216 on PCB Under Still Air Convention

Table 19. Thermal Performance of LQFP-48 on PCB Under Still Air Convention

	θ_{JA}	θ_{JB}	θ_{JC}	Ψ_{JT}	Ψ_{JB}
4L PCB	TBD	TBD	TBD	TBD	TBD
2L PCB	TBD	TBD	TBD	TBD	TBD

Thermal Performance of E-Pad LQFP-216 on PCB Under Forced Convection

Table 20. Thermal Performance of LQFP-48 on PCB Under Forced Convection

	Air Flow (m/s)	0	1	2	3
4L PCB	θ_{JA}	TBD	TBD	TBD	TBD
	Ψ_{JT}	TBD	TBD	TBD	TBD
	Ψ_{JB}	TBD	TBD	TBD	TBD
2L PCB	θ_{JA}	TBD	TBD	TBD	TBD
	Ψ_{JT}	TBD	TBD	TBD	TBD
	Ψ_{JB}	TBD	TBD	TBD	TBD

Note:

θ_{JA}: Junction to ambient thermal resistance

θ_{JB}: Junction to board thermal resistance

θ_{JC}: Junction to case thermal resistance

Ψ_{JT}: Junction to top center of package thermal characterization

Ψ_{JB}: Junction to bottom surface center of PCB thermal characterization

10.4. DC Characteristics

Table 21. DC Characteristics

Parameter	SYM	Min	Typical	Max	Units
RTL8231 idle (no loading)					
Power Supply Current for VDD	$I_{DVDDIO0}$	-	17	-	mA
Total Power Consumption			56.1		mW
Scan Single color LED					
Power Supply Current for VDD	$I_{DVDDIO0}$	-	109	-	mA
Total Power Consumption for 72 LED application	PS	-	359.7	-	mW
Scan Bi-color LED					
Power Supply Current for VDD 48 LED application	$I_{DVDDIO0}$	-	116	-	mA
Total Power Consumption	PS	-	382.8	-	mW
Shift Register Mode					
Power Supply Current for VDD 36 LED application	$I_{DVDDIO0}$	-	132	-	mA
Total Power Consumption	PS	-	435.6	-	mW
VDDIO=3.3V					
TTL Input High Voltage	V_{ih}	2.0	-	-	V
TTL Input Low Voltage	V_{il}	-	-	0.8	V
Output High Voltage	V_{oh}	2.7	-	-	V
Output Low Voltage	V_{ol}	-	-	0.6	V

10.5. AC Characteristics

10.5.1. SMI Slave Mode Timing Characteristics

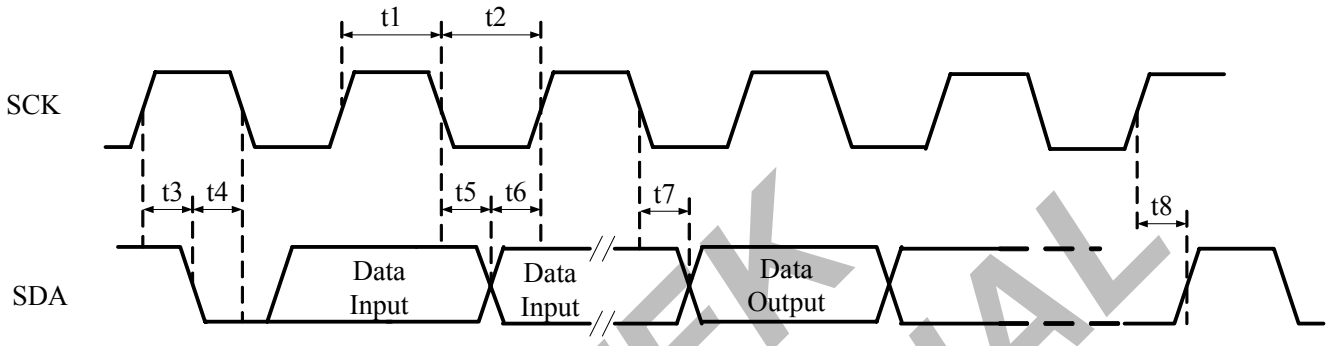

Figure 22. SMI Slave Mode Timing Characteristics

Table 22. SMI Slave Mode Timing Characteristics

Symbol	Description	I/O	Min	Typical	Max	Units
t1	SCK High Time **A1*	I	400	-	-	ns
t2	SCK Low Time **A1*	I	400	-	-	ns
t3	START Condition Setup Time	I	150	-	-	ns
t4	START Condition Hold Time	I	150	-	-	ns
t5	Data Hold Time	I	200	-	-	ns
t6	Data Setup Time	I	10	-	-	ns
t7	Clock to Data Output Delay	O	200		350	ns
t8	STOP Condition Setup Time	I	150	-	-	ns

**A1: Base on the RC clock is 10MHz*

10.6. MII Management (MIIM) Interface Timing

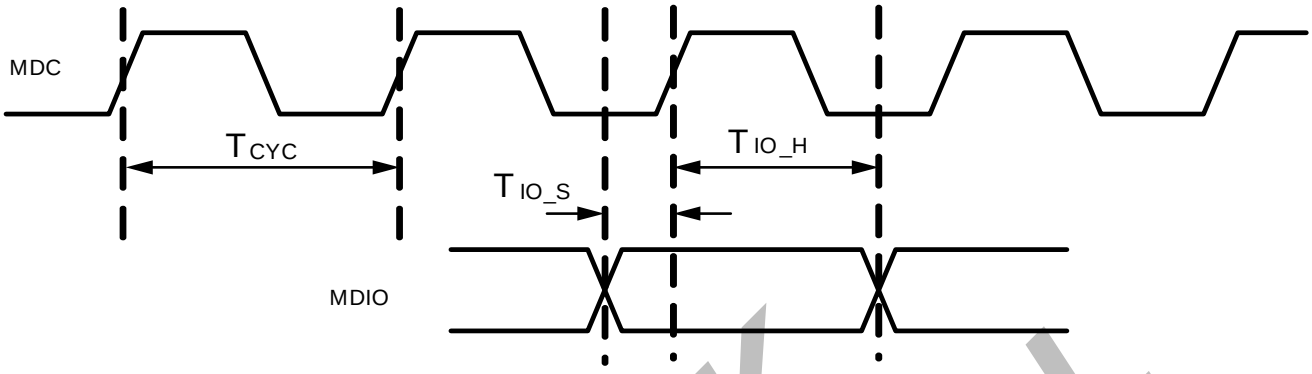

Figure 23. MII Management (MIIM) Interface Write Timing

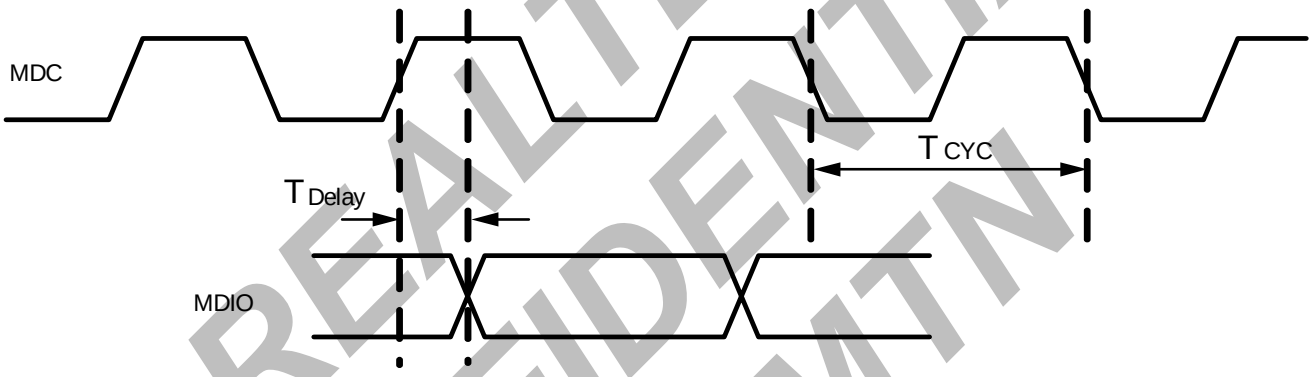

Figure 24. MII Management (MIIM) Interface Read Timing

Table 23. MII Management (MIIM) Interface Timing

Parameter	SYM	Condition	Min	Typical	Max	Units
MDC Clock Input Cycle	T_{CYC}	MDC Clock Input Cycle	50	-	-	ns
MDIO to MDC Rising Input Setup Time	T_{IO_S}	MDIO to MDC Rising Input Setup Time	10	-	-	ns

Parameter	SYM	Condition	Min	Typical	Max	Units
MDIO to MDC Rising Input Hold Time	T_{IO_H}	MDIO to MDC Rising Input Hold Time	10	-	-	ns
MDIO Output Delay	T_{Delay}	MDC to MDIO Rising Output Delay	-	-	10	ns

10.7. Reset Characteristics

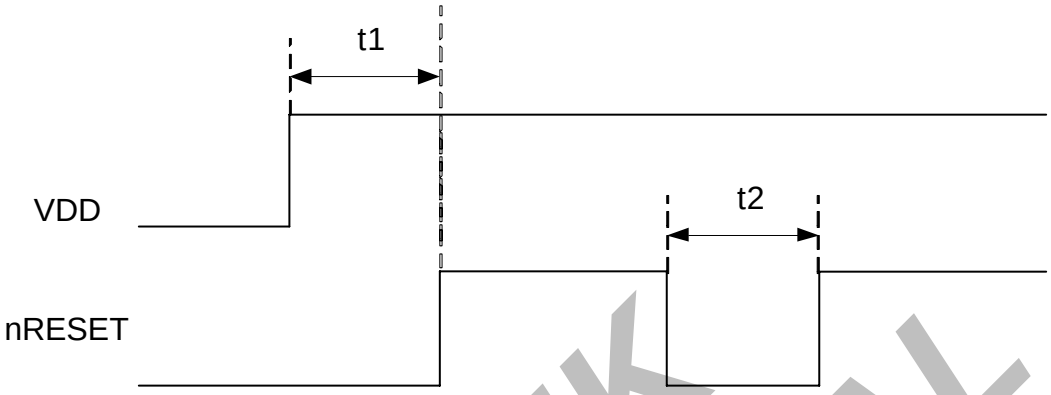

Figure 25. Reset Characteristics

Table 24. Reset Characteristics

Symbol	Description	I/O	Min	Typical	Max	Units
t1	Reset Delay	I	1	-	-	ms
t2	Reset Low	I	1	-	-	ms

11. Mechanical Dimensions

11.1. LQFP-48 Dimensions

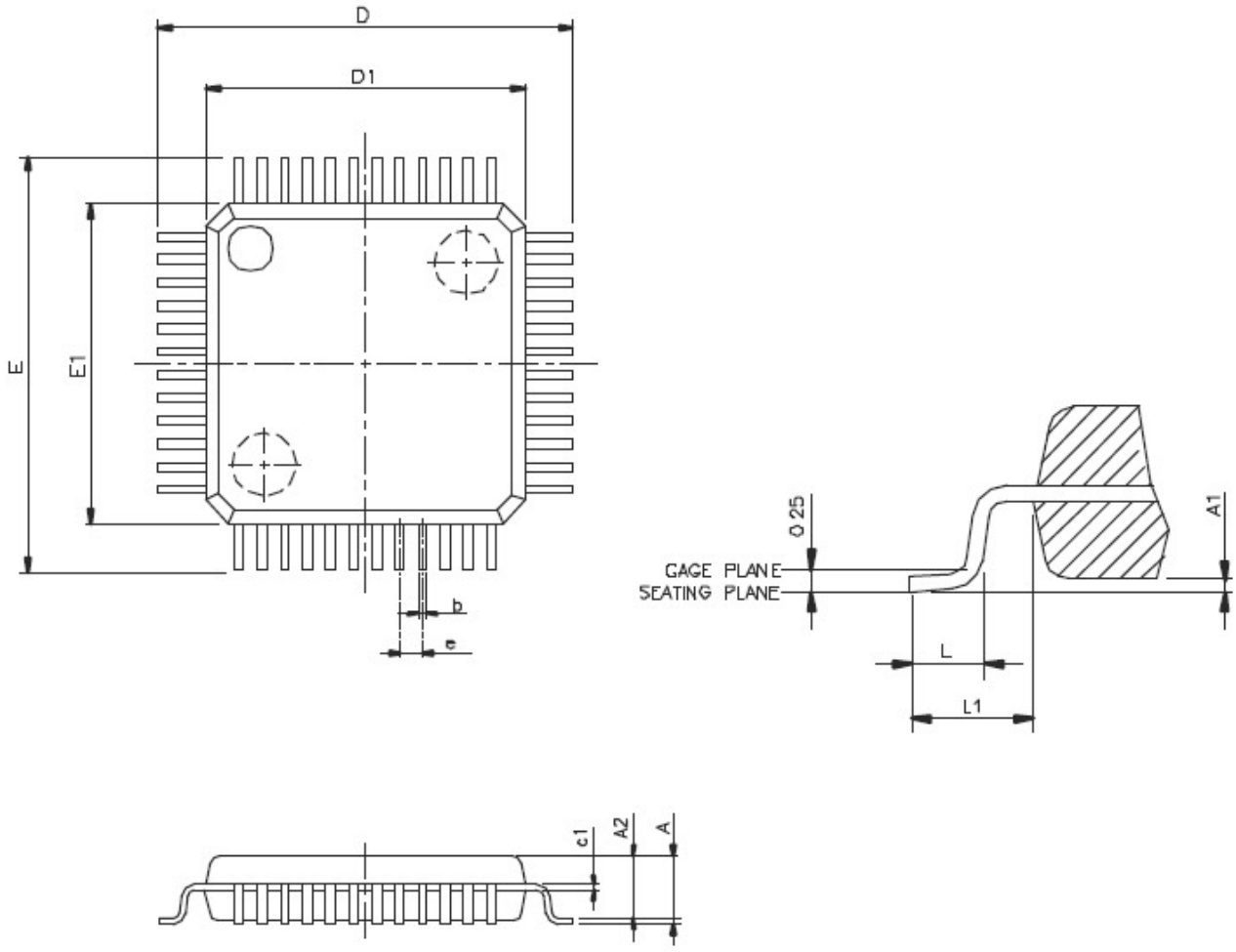

Table 25. Dimension Range for LQFP-48 Pin (7*7 mm)

Symbol	Dimension in mm		Dimension in inch	
	Min	Max	Min	Max
A	--	1.6	--	0.06299
A1	0.05	0.15	0.00196	0.00591
A2	1.35	1.45	0.05315	0.05708
c1	0.09	0.16	0.00354	0.00629
D	9.00 BSC		0.3543 BSC	
D1	7.00 BSC		0.2756 BSC	
E	9.00 BSC		0.3543 BSC	
E1	7.00 BSC		0.2756 BSC	
e	0.5 BSC		0.0197 BSC	
b	0.17	0.27	0.0067	0.0106
L	0.45	0.75	0.0177	0.0295
L1	1 REF		0.0393 REF	

NOTES:

1. JEDEC outline: MS-026 BBC
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm per side. D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. dimension b does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum b dimension by more than 0.08mm.

12. Ordering Information

Table 26. Ordering Information

Part Number	Package	Status
RTL8231-GR	LQFP 48-Pin ‘Green’ Package	-

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