2.25 GHz XpressView HDMI 1:2 Splitter with 4:1 Input Mux

Data Sheet **ADV7630**

FEATURES

- 2.25 GHz TMDS HDMI 1:2 splitter with 4:1 input mux
- High-Definition Multimedia Interface (HDMI) supported
  - All mandatory and additional 3D video formats supported
  - CEC 1.4-compatible
- 225 MHz maximum TMDS clock frequency
  - XpressView fast switching on all HDMI input ports
- 36-/30-bit per pixel Deep Color and 24-bit per pixel color support
  - High-bandwidth Digital Content Protection (HDCP) 1.4 support with internal HDCP keys
  - HDCP repeater support
    - Up to 127 KSVs supported
  - Integrated CEC controller
  - 5 V detect and hot plug assert for each HDMI port
  - EDID data extraction on HDMI outputs
  - Hot plug detection (HPD) input on HDMI outputs
- General
  - Interrupt controller with interrupt output
  - On-chip 5 V regulator for 5 V HDMI cable power support
  - Software libraries, driver, and application available
  - Internal EDID RAM
  - 128-lead 14 mm × 14 mm TQFP_EP package

APPLICATIONS

- Video conferencing
- HDTV
- AVR, HTiB
- Soundbar
- Video switch
- HDMI splitter

FUNCTIONAL BLOCK DIAGRAM

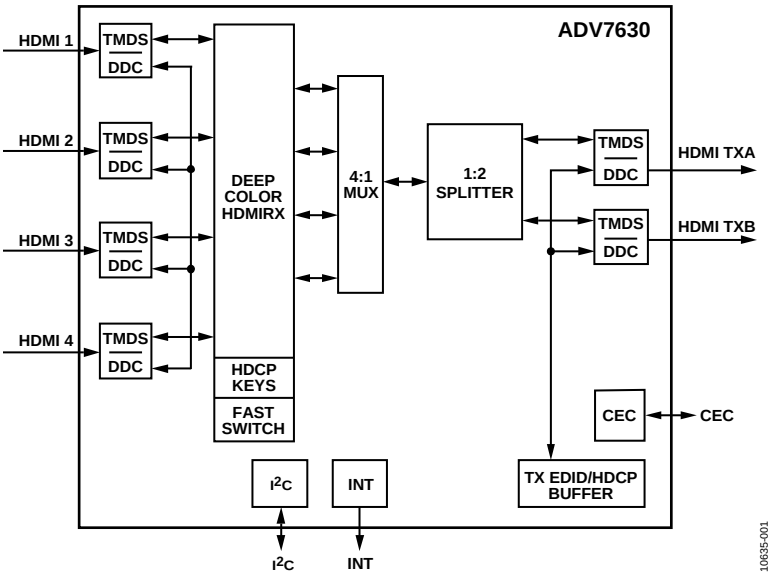


Figure 1.

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
Technical Support www.analog.com

TABLE OF CONTENTS

REVISION HISTORY

9/12—Revision 0: Initial Version

GENERAL DESCRIPTION

The ADV7630 is a high quality 1:2 HDMI® splitter with 4:1 input multiplexer. It incorporates a four-input HDMI receiver and dual transmitter functions onto a single chip. The ADV7630 supports all mandatory HDMI 3D TV formats, HDTV formats up to 1080p 36-bits per pixel Deep Color, and display resolutions up to 1080p60. The reception of HDCP encrypted video is also supported by the HDMI receiver with TMDS The HDMI video transmitted to the downstream device by the transmitter. HDMI output features dedicated DDC lines with an HDCP encryption engine.

The ADV7630 integrates an HDMI CEC controller that supports the capability discovery and control (CDC) feature.

The ADV7630 incorporates XpressView™ fast switching on all input HDMI ports. Using an Analog Devices, Inc., hardware-based HDCP engine that minimizes software overhead, XpressView technology allows fast switching between all HDMI input ports in less than 1 second.

Each HDMI input port has dedicated 5 V detect and hot plug assert pins. The HDMI receiver also includes an integrated equalizer that ensures robust operation of the interface even with long and low quality cables.

Each HDMI has a dedicated hot plug detect port and DDC lines along with an internal HDCP encryption engine.

The ADV7630 features an EDID replicator and internal EDID RAM. On the transmitter side, DDC control allows reading back EDID data from sink. As the part incorporates an internal regulator, the EDID functionality on the receiver's side can be powered from the HDMI cable when ac power is removed from the system.

Fabricated in an advanced CMOS process, the ADV7630 is provided in a 14 mm × 14 mm, 128-lead surface-mount TQFP_EP, RoHS-compliant package and is specified over the 0°C to 70°C temperature range.

DETAILED FUNCTIONAL BLOCK DIAGRAM

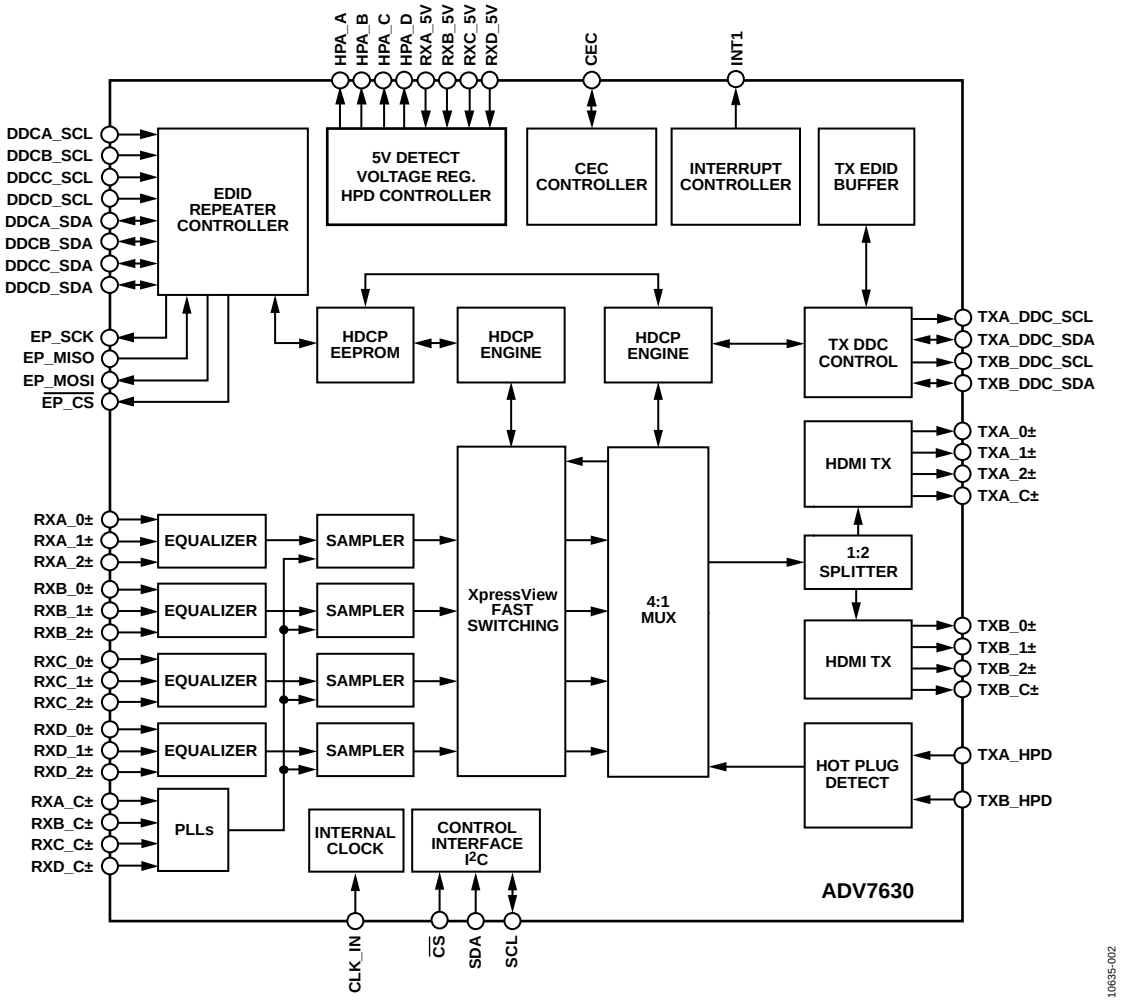


Figure 2.

SPECIFICATIONS

DVDD, TXA_PVDD, TXB_PVDD, CVDD, TX_AVDD at 1.71 V to 1.89 V; DVDDIO, TVDD, SYS_3P3V at 3.14 V to 3.46 V; T_{MIN} to T_{MAX} = 0ºC to 70ºC, unless otherwise noted.

ELECTRICAL CHARACTERISTICS

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
DIGITAL INPUTS						
Input High Voltage	V_{IH}	Digital inputs	2			V
Input Low Voltage	V_{IL}	Digital inputs			0.8	V
Input Current	I_{IN}	$\overline{RESET}$, $\overline{CS}$, EP_MISO		40		µA
		Other digital inputs		10		µA
Input Capacitance[1]	C_{IN}	Excluding differential HDMI inputs			20	pF
DIGITAL INPUTS (5 V TOLERANT)[2]						
Input High Voltage	V_{IH}		2.6			V
Input Low Voltage	V_{IL}				0.8	V
High Impedance Leakage Current	I_{LEAK}	DDCA_SCL, DDCB_SCL, DDCC_SCL, DDCD_SCL, DDCA_SDA, DDCB_SDA, DDCC_SDA, DDCD_SDA, TXA_DDC_SDA, TXB_DDC_SDA[3]		30		µA
		TXA_HPD, TXB_HPD		10		µA
DIGITAL OUTPUTS						
Output High Voltage	V_{OH}		2.4			V
Output Low Voltage	V_{OL}				0.4	V
High Impedance Leakage Current	I_{LEAK}	DDCA_SDA, DDCB_SDA, DDCC_SDA, DDCD_SDA, TXA_DDC_SDA, TXB_DDC_SDA, TXA_DDC_SCL, TXB_DDC_SCL[3]		30		µA
		All other digital pins		10		µA
Output Capacitance[1]	C_{OUT}	Excluding non-tristable outputs[4]			20	pF
POWER REQUIREMENTS[1]						
Digital Core Power Supply	DVDD		1.71	1.8	1.89	V
Digital I/O Power Supply	DVDDIO		3.14	3.3	3.46	V
PLL Power Supply TXA	TXA_PVDD		1.71	1.8	1.89	V
PLL Power Supply TXB	TXB_PVDD		1.71	1.8	1.89	V
Terminator Power Supply	TVDD		3.14	3.3	3.46	V
Comparator Power Supply	CVDD		1.71	1.8	1.89	V
System Power Supply	SYS_3P3V		3.14	3.3	3.46	V
TX Analog Power Supply	TX_AVDD		1.71	1.8	1.89	V
Power-Up Time	t_{PWRUP}			25		ms
Test Condition 1						
Digital Core Power Supply	I_{DVDD}	Test Condition 1		277	303	mA
Digital I/O Power Supply	I_{DVDDIO}	Test Condition 1		0.13	0.13	mA
PLL Power Supply	I_{TX_PVDD}[5]	Test Condition 1		85.9	97.6	mA
Terminator Power Supply	I_{TVDD}	Test Condition 1		226	227	mA
Comparator Power Supply	I_{CVDD}	Test Condition 1		307	328	mA
System Power Supply	I_{SYS_3P3V}	Test Condition 1		2.21	3.23	mA
TX Analog Power Supply	I_{TX_AVDD}	Test Condition 1		33.0	34.9	mA

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
Test Condition 2						
Power-Down Currents[1]	I_{DVDD_PD}	Test Condition 2		0.38	1.974	mA
	I_{DVDDIO_PD}	Test Condition 2		0	0.128	mA
	$I_{TX\_PVDD\_PD}$[6]	Test Condition 2		0.057	0.157	mA
	I_{TVDD_PD}	Test Condition 2		0.031	0.082	mA
	I_{CVDD_PD}	Test Condition 2		0.027	0.101	mA
	$I_{SYS\_3P3V\_PD}$	Test Condition 2		0.050	0.217	mA
	$I_{TX\_AVDD\_PD}$	Test Condition 2		3.160	3.450	mA

[1] Data recorded during lab characterization.
[2] The following pins are 5 V tolerant: TXA_DDC_SCL, TXA_DDC_SDA, TXB_DDC_SCL, TXB_DDC_SDA, DDCA_SCL, DDCA_SDA, DDCB_SCL, DDCB_SDA, DDCC_SCL, DDCC_SDA, DDCD_SCL, DDCD_SDA.
[3] SDA pins are bidirectional.
[4] Non-tristatable pins are all differential HDMI TX outputs.
[5] Sum of currents I_{TXA_PVDD} and I_{TXB_PVDD}.
[6] Sum of currents $I_{TXA\_PVDD\_PD}$ and $I_{TXB\_PVDD\_PD}$.

Table 2. Test Conditions for Power Requirements

Parameter	Value Used for Typical Case	Value Used For Maximum Case
TEST CONDITION 1		
Number of HDMI Inputs (XpressView Mode)	Four inputs	Four inputs
Video Format (Each HDMI Input)	1080p60, 12 bits	1080p60, 12 bits
HDCP Encryption	Transmitter only	Transmitter only
HDCP Decryption	Off	Off
Audio	192 kHz PCM	192 kHz PCM
Video Pattern (Each HDMI Input)	Pseudo random	Pseudo random
Number of HDMI Outputs Used	Two outputs	Two outputs
Temperature	25°C	70°C
Power Supply Voltages	Nominal	Maximum
TEST CONDITION 2 (POWER-DOWN)		
Number of HDMI Inputs (XpressView Mode)	Not applicable	Not applicable
Video Format (Each HDMI Input)	Not applicable	Not applicable
HDCP Decryption	Not applicable	Not applicable
Video Pattern (Each HDMI Input)	Not applicable	Not applicable
Number of HDMI Outputs Used	Not applicable	Not applicable
Audio	Not applicable	Not applicable
Temperature	25°C	70°C
Power Supply Voltages	Nominal	Maximum

TIMING CHARACTERISTICS

Data and I²C Timing Characteristics

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit
CLOCK					
Clock Frequency, CLK_IN			27.000		MHz
Frequency Stability				200	ppm
TMDS Frequency Range		25		225	MHz
I²C PORTS[1]					
SCL Frequency				400	kHz
SCL Minimum Pulse Width High	t_1	600			ns
SCL Minimum Pulse Width Low	t_2	1.3			µs
Start Condition Hold Time	t_3	600			ns
Start Condition Setup Time	t_4	600			ns
SDA Setup Time	t_5	100			ns
SCL and SDA Rise Time	t_6			300	ns
SCL and SDA Fall Time	t_7			300	ns
Stop Condition Setup Time	t_8	0.6			µs
RESET FEATURE					
$\overline{\text{RESET}}$ Pulse Width		5			ms
SPI PORT[1]					
$\overline{\text{EP\_CS}}$ Falling Edge Before First EP_SCK Edge	t_{CSL}		191.4	217.5	ns
$\overline{\text{EP\_CS}}$ Rising Edge After Last Rising EP_SCK Edge	t_{CSH}		191.4	217.5	ns
SCLK Low Pulse Width	t_{SL}		191.4	217.5	ns
SCLK High Pulse Width	t_{SH}		191.4	217.5	ns
Data Output Valid After EP_SCK Edge	t_{DAV}			27.2	ns
Data Output Setup Before EP_SCK Edge	t_{DOSU}			217.5	ns
Data Input Setup Time Before EP_SCK Edge	t_{DSU}	21.3			ns
Data Input Hold Time After EP_SCK Edge	t_{DHD}	21.3			ns

[1] Data guaranteed by design.

Timing Diagrams

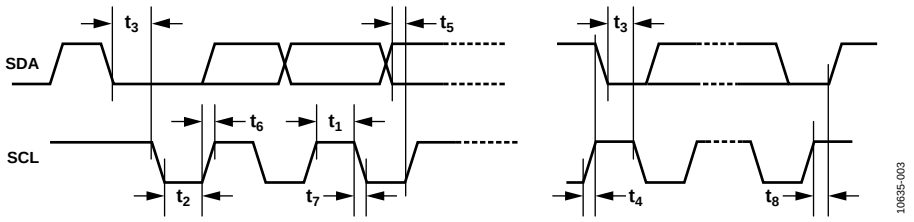


Figure 3. I²C Timing

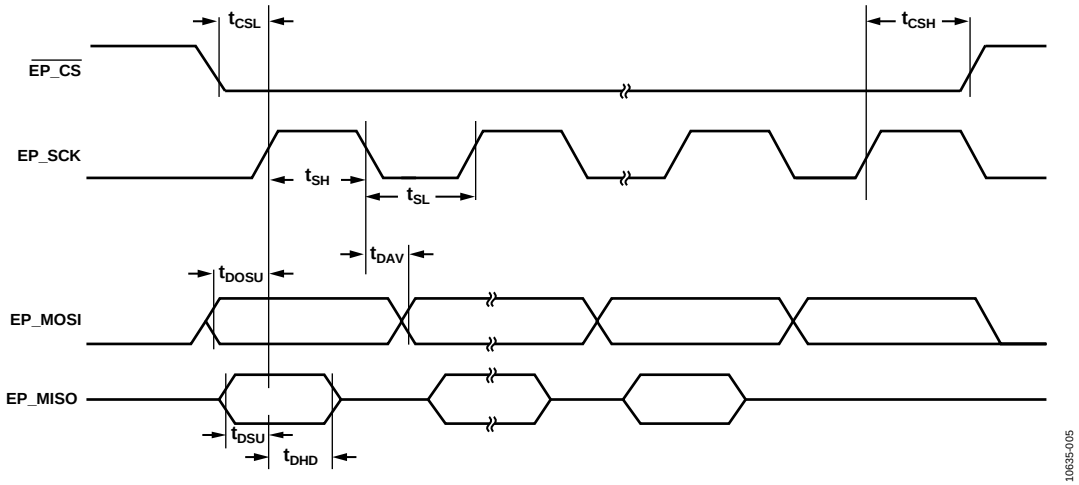


Figure 4. SPI Timing

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
CVDD to GND	2.2 V
DVDD to GND	2.2 V
TVDD to GND	3.9 V
TX_AVDD to GND	2.2 V
TXA_PVDD to GND	2.2 V
TXB_PVDD to GND	2.2 V
SYS_3P3V to GND	3.9 V
DVDDIO to GND	3.9 V
Digital Inputs Voltage to GND	GND – 0.3 V to DVDDIO + 0.3 V
Analog Inputs Voltage to GND	GND – 0.3 V to TXA_PVDD + 0.3 V
HDMI Digital Inputs Voltage to GND	GND – 0.3 V to TVDD + 0.3 V
5 V Tolerant Digital Inputs to GND[1, 3, 6]	GND – 0.3 V to 5.5 V
5 V Digital Inputs[2]	
5 V Tolerant Digital Outputs to GND[3, 6]	GND – 0.3 V to 5.5 V
Digital Outputs Voltage to GND[4, 5]	GND – 0.3 V to DVDDIO + 0.3 V
Analog Outputs Voltage to GND	GND – 0.3 V to CVDD + 0.3 V
HDMI Digital Outputs to GND	GND – 0.3 V to TVDD + 0.3 V
Maximum Junction Temperature ($T_{J\ MAX}$)	125°C
Storage Temperature Range	−60°C to +150°C
Infrared Reflow Soldering (20 sec)	260°C

[1] The following pins are 3.3 V inputs, 5 V tolerant: TXB_HPD, TXB_DDC_SDA, , TXA_HPD, TXA_DDC_SDA, DDCA_SCL, DDCB_SCL, DDCC_SCL, DDCD_SCL.
[2] The following pins are 5 V inputs: RXA_5V, RXB_5V, RXC_5V, RXD_5V.
[3] The following pins are 3.3 V outputs, 5 V tolerant: TXB_DDC_SCL, TXA_DDC_SCL, HPA_D, HPA_C, HPA_B, HPA_A.
[4] Except the DDCA_SDA, DDCB_SDA, DDCC_SDA, DDCD_SDA, EP_MOSI, EP_SCK, and $\overline{EP\_CS}$ pins, which are kept to GND – 0.3 V to REG_3P3V.
[5] Except the REG_3P3V output, which is kept to GND – 0.3 V to SYS_3P3 + 0.3 V and REG_1P8V output, which is kept to GND – 0.3 V to DVDD + 0.3 V.
[6] The following pins are 3.3 V bidirectional input/outputs, 5 V tolerant: TXA_DDC_SDA, TXB_DDC_SDA, DDCA_SDA, DDCB_SDA, DDCC_SDA, and DDCD_SDA.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL PERFORMANCE

To reduce power consumption when using the ADV7630, the user is advised to turn off the unused sections of the part.

Due to PCB metal variation and, therefore, variation in PCB heat conductivity, the value of θ_{JA} may differ for various PCBs.

The most efficient measurement solution is obtained using the package surface temperature to estimate the die temperature because this eliminates the variance associated with the θ_{JA} value.

The maximum junction temperature ($T_{J\ MAX}$) of 125°C must not be exceeded. The following equation calculates the junction temperature using the measured package surface temperature and applies only when no heat sink is used on the device under test (DUT):

$$T_J = T_S + (\Psi_{JT} \times W_{TOTAL})$$

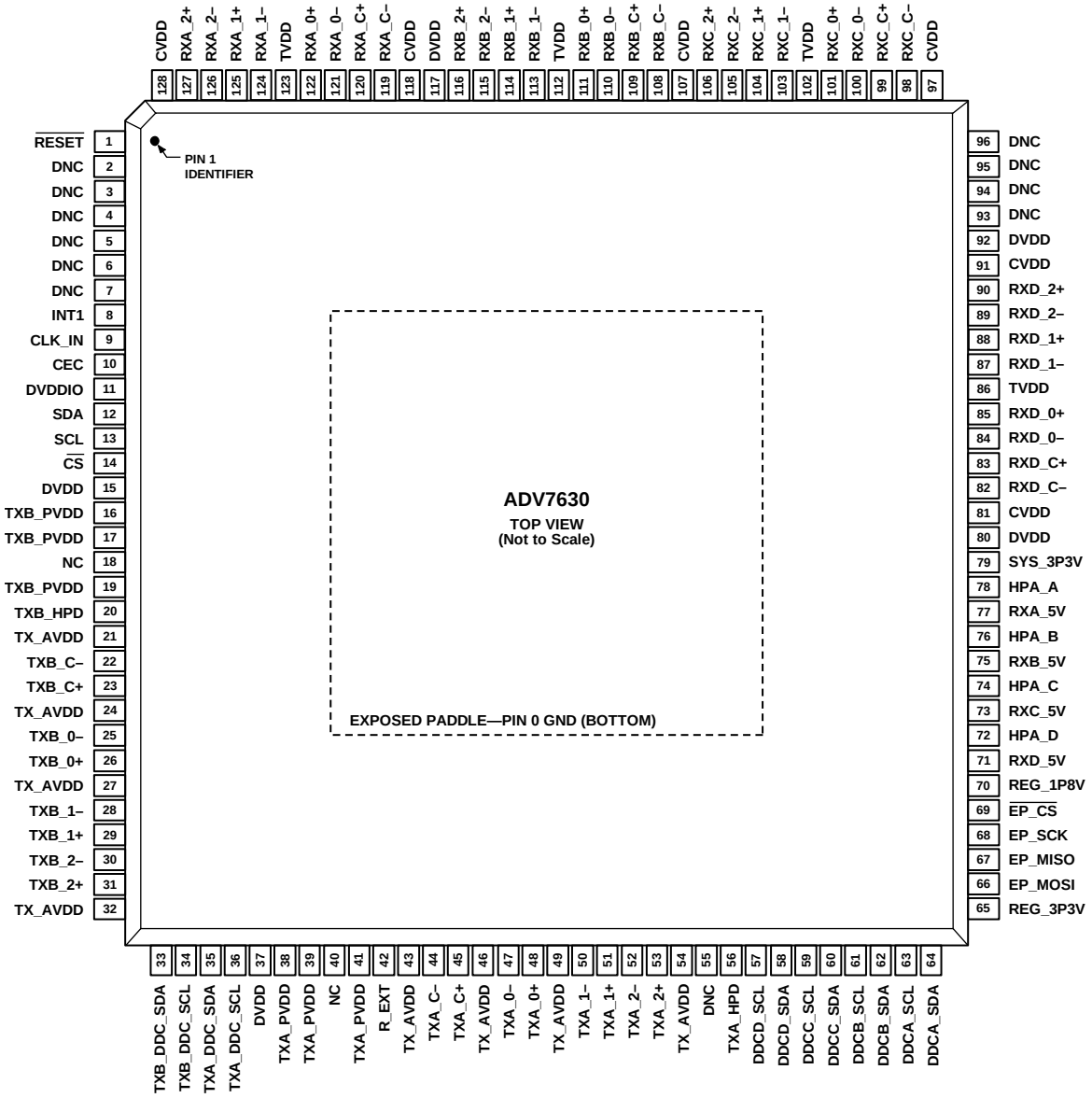
where:
T_S is the package surface temperature (°C).
Ψ_{JT} is 0.22°C/W for the 128-lead TQFP_EP.
$W_{TOTAL} = ((CVDD \times I_{CVDD}) + (0.2 \times TVDD \times I_{TVDD}) + (DVDD \times I_{DVDD}) + (TX\_AVDD \times I_{TX\_AVDD}) + (TXA\_PVDD \times I_{TXA\_PVDD}) + (TXB\_PVDD \times I_{TXA\_PVDD}) + (DVDDIO \times I_{DVDDIO})) + N_{TX} \times P_{TX}$

where:
0.2 is 20% of the TVDD power that is dissipated on the part itself.
N_{TX} is the number of connected and active TX ports.
P_{TX} = 28 mW minus average power dissipated on-chip of each HDMI transmitters.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. PINS LABELED NC CAN BE ALLOWED TO FLOAT, BUT IT IS BETTER TO CONNECT THESE PINS TO GROUND. AVOID ROUTING HIGH SPEED SIGNALS THROUGH THESE PINS BECAUSE NOISE COUPLING MAY RESULT.
2. EXPOSED PAD SHOULD BE CONNECTED TO GND.
3. DNC = DO NOT CONNECT TO THIS PIN.

10635-008

Figure 5. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
0	GND	Ground	The Exposed Pad Should be Connected to GND.
1	$\overline{\text{RESET}}$	Miscellaneous digital	System Reset Input. Active low. A minimum low reset pulse width of 5 ms is required to reset the ADV7630 circuitry.
2 to 7, 55, 93 to 96	DNC	Do not connect	Do not connect to this pin.
8	INT1	Miscellaneous digital	Interrupt Output Pin.
9	CLK_IN	Digital input	Input Pin for a 3.3 V 27.000 MHz Clock Oscillator. The following frequencies are also supported: 24 MHz, 24.576 MHz, and 28.63636 MHz.
10	CEC	Digital input/output	Consumer Electronic Control Channel.
11	DVDDIO	Power	Digital I/O Supply Voltage (3.3 V).
12	SDA	Digital input/output	I^2C Port Serial Data Input/Output Pin. SDA is the data line for the control port.
13	SCL	Digital input	I^2C Port Serial Clock Input. SCL is the clock line for the control port.
14	$\overline{\text{CS}}$	Digital input	Chip Select Pin. Pulling this pin up causes the I^2C state machine to ignore I^2C transmission. This pin has internal pull-down.
15	DVDD	Power	Digital Core Supply Voltage (1.8 V).
16	TXB_PVDD	Power	1.8 V Power Supply for PLL. This supply should be filtered and as quiet as possible. It should be kept separately from TXA_PVDD to avoid possible crosstalk. This power supply must be filtered with a ferrite bead and decoupled with 100 nF in parallel with 10 nF capacitors. The 100 nF and 10 nF capacitors must be placed close to the package.
17	TXB_PVDD	Power	1.8 V Power Supply for PLL. This supply should be filtered and as quiet as possible. It should be kept separately from TXA_PVDD to avoid possible crosstalk. This power supply must be filtered with a ferrite bead and decoupled with 100 nF in parallel with 10 nF capacitors. The 100 nF and 10 nF capacitors must be placed close to the package.
18, 40	NC	Not connected	This pin is not connected internally (see Figure 5).
19	TXB_PVDD	Power	1.8 V Power Supply for PLL. This supply should be filtered and as quiet as possible. It should be kept separately from TXA_PVDD to avoid possible crosstalk. This power supply must be filtered with a ferrite bead and decoupled with 100 nF in parallel with 10 nF capacitors. The 100 nF and 10 nF capacitors must be placed close to the package.
20	TXB_HPD	Digital input	Hot Plug Detect Signal of HDMI Output Port B. This pin indicates to the interface whether the receiver is connected. It supports 1.8 V to 5 V CMOS logic levels.
21	TX_AVDD	Power	1.8 V Power Supply for TMDS Outputs.
22	TXB_C−	HDMI output	TMDS Clock Output Complement of HDMI Output Port B.
23	TXB_C+	HDMI output	TMDS Clock Output True of HDMI Output Port B.
24	TX_AVDD	Power	1.8 V Power Supply for TMDS Outputs.
25	TXB_0−	HDMI output	TMDS Output Channel 0 Complement of HDMI Output Port B.
26	TXB_0+	HDMI output	TMDS Output Channel 0 True of HDMI Output Port B.
27	TX_AVDD	Power	1.8 V Power Supply for TMDS Outputs.
28	TXB_1−	HDMI output	TMDS Output Channel 1 Complement of HDMI Output Port B.
29	TXB_1+	HDMI output	TMDS Output Channel 1 True of HDMI Output Port B.
30	TXB_2−	HDMI output	TMDS Output Channel 2 Complement of HDMI Output Port B.
31	TXB_2+	HDMI output	TMDS Output Channel 2 True of HDMI Output Port B.
32	TX_AVDD	Power	1.8 V Power Supply for TMDS Outputs.
33	TXB_DDC_SDA	Digital input/output	HDCP Master Serial Data of HDMI Output Port B. TXB_DDC_SDA is a 3.3 V open-drain input/output that is 5 V tolerant.
34	TXB_DDC_SCL	Digital output	HDCP Master Serial Clock of HDMI Output Port B. TXB_DDC_SCL is a 3.3 V open-drain output that is 5 V tolerant.

Pin No.	Mnemonic	Type	Description
35	TXA_DDC_SDA	Digital input/output	HDCP Master Serial Data of HDMI Output Port A. TXA_DDC_SDA is a 3.3 V open-drain input/output that is 5 V tolerant.
36	TXA_DDC_SCL	Digital output	HDCP Master Serial Clock of HDMI Output Port A. TXA_DDC_SCL is a 3.3 V open-drain output that is 5 V tolerant.
37	DVDD	Power	Digital Core Supply Voltage (1.8 V).
38	TXA_PVDD	Power	1.8 V Power Supply for PLL. This supply should be filtered and as quiet as possible. It should be kept separately from TXB_PVDD to avoid possible crosstalk. This power supply must be filtered with a ferrite bead and decoupled with 100 nF in parallel with 10 nF capacitors. The 100 nF and 10 nF capacitors must be placed close to the package.
39	TXA_PVDD	Power	1.8 V Power Supply for PLL. This supply should be filtered and as quiet as possible. It should be kept separately from TXB_PVDD to avoid possible crosstalk. This power supply must be filtered with a ferrite bead and decoupled with 100 nF in parallel with 10 nF capacitors. The 100 nF and 10 nF capacitors must be placed close to the package.
41	TXA_PVDD	Power	1.8 V Power Supply for PLL. This supply should be filtered and as quiet as possible. It should be kept separately from TXB_PVDD to avoid possible crosstalk. This power supply must be filtered with a ferrite bead and decoupled with 100 nF in parallel with 10 nF capacitors. The 100 nF and 10 nF capacitors must be placed close to the package.
42	R_EXT	Input	Sets internal reference currents. Place a 470 Ω resistor (1% tolerance) between this pin and ground.
43	TX_AVDD	Power	1.8 V Power Supply for TMDS Outputs.
44	TXA_C−	HDMI output	TMDS Clock Output Complement of HDMI Output Port A.
45	TXA_C+	HDMI output	TMDS Clock Output True of HDMI Output Port A.
46	TX_AVDD	Power	1.8 V Power Supply for TMDS Outputs.
47	TXA_0−	HDMI output	TMDS Output Channel 0 Complement of HDMI Output Port A.
48	TXA_0+	HDMI output	TMDS Output Channel 0 True of HDMI Output Port A.
49	TX_AVDD	Power	1.8 V Power Supply for TMDS Outputs.
50	TXA_1−	HDMI output	TMDS Output Channel 1 Complement of HDMI Output Port A.
51	TXA_1+	HDMI output	TMDS Output Channel 1 True of HDMI Output Port A.
52	TXA_2−	HDMI output	TMDS Output Channel 2 Complement of HDMI Output Port A.
53	TXA_2+	HDMI output	TMDS Output Channel 2 True of HDMI Output Port A.
54	TX_AVDD	Power	1.8 V Power Supply for TMDS Outputs.
56	TXA_HPD	Digital input	Hot Plug Detect Signal of HDMI Output Port A. This pin indicates to the interface whether the receiver is connected. It supports 1.8 V to 5 V CMOS logic levels.
57	DDCD_SCL	Digital input	HDCP Slave Serial Clock Port D. DDCD_SCL is a 3.3 V input that is 5 V tolerant.
58	DDCD_SDA	Digital input/output	HDCP Slave Serial Data Port D. DDCD_SDA is a 5 V tolerant 3.3 V input and open-drain output.
59	DDCC_SCL	Digital input	HDCP Slave Serial Clock Port C. DDCC_SCL is a 3.3 V input that is 5 V tolerant.
60	DDCC_SDA	Digital input/output	HDCP Slave Serial Data Port C. DDCC_SDA is a 5 V tolerant 3.3 V input and open-drain output.
61	DDCB_SCL	Digital input	HDCP Slave Serial Clock Port B. DDCB_SCL is a 3.3 V input that is 5 V tolerant.
62	DDCB_SDA	Digital input/output	HDCP Slave Serial Data Port B. DDCB_SDA is a 5 V tolerant 3.3 V input and open-drain output.
63	DDCA_SCL	Digital input	HDCP Slave Serial Clock Port A. DDCA_SCL is a 3.3 V input that is 5 V tolerant.
64	DDCA_SDA	Digital input/output	HDCP Slave Serial Data Port A. DDCA_SDA is a 5 V tolerant 3.3 V input and open-drain output.
65	REG_3P3V	Power output	Output of Internal 3.3 V LDO. Must be connected to ground via decoupling capacitors (10 nF in parallel with 100 nF capacitor). This pin can be used to power up external EDID SPI EEPROM when part is in power-down mode and 5 V is connected to the part from an HDMI cable.
66	EP_MOSI	Digital output	SPI Master Output/Slave Input for External EDID Interface.
67	EP_MISO	Digital input	SPI Master Input/Slave Output for External EDID Interface.
68	EP_SCK	Digital output	SPI Clock for External EDID Interface.
69	$\overline{\text{EP\_CS}}$	Digital output	SPI Chip Select for External EDID Interface.

Pin No.	Mnemonic	Type	Description
70	REG_1P8V	Power output	Output of Internal 1.8 V LDO. This pin must be connected only to decoupling capacitors (100 nF in parallel with 10 nF).
71	RXD_5V	HDMI input	5 V Detect Pin for Port D in the HDMI Interface. This pin is used to power the EDID replicator.
72	HPA_D	HDMI output	Hot Plug Assert Signal Output for HDMI Port D.
73	RXC_5V	HDMI input	5 V Detect Pin for Port C in the HDMI Interface. This pin is used to power the EDID replicator.
74	HPA_C	HDMI output	Hot Plug Assert Signal Output for HDMI Port C.
75	RXB_5V	HDMI input	5 V Detect Pin for Port B in the HDMI Interface. This pin is used to power the EDID replicator.
76	HPA_B	HDMI output	Hot Plug Assert Signal Output for HDMI Port B.
77	RXA_5V	HDMI input	5 V Detect Pin for Port A in the HDMI Interface. This pin is used to power the EDID replicator.
78	HPA_A	HDMI output	Hot Plug Assert Signal Output for HDMI Port A.
79	SYS_3P3V	Miscellaneous power	3.3 V Power Supply.
80	DVDD	Power	Digital Core Supply Voltage (1.8 V).
81	CVDD	Power	HDMI Analog Block Supply Voltage (1.8 V).
82	RXD_C−	HDMI input	Digital Input Clock Complement of Port D in the HDMI Interface.
83	RXD_C+	HDMI input	Digital Input Clock True of Port D in the HDMI Interface.
84	RXD_0−	HDMI input	Digital Input Channel 0 Complement of Port D in the HDMI Interface.
85	RXD_0+	HDMI input	Digital Input Channel 0 True of Port D in the HDMI Interface.
86	TVDD	Power	Terminator Supply Voltage (3.3 V).
87	RXD_1−	HDMI input	Digital Input Channel 1 Complement of Port D in the HDMI Interface.
88	RXD_1+	HDMI input	Digital Input Channel 1 True of Port D in the HDMI Interface.
89	RXD_2−	HDMI input	Digital Input Channel 2 Complement of Port D in the HDMI Interface.
90	RXD_2+	HDMI input	Digital Input Channel 2 True of Port D in the HDMI Interface.
91	CVDD	Power	HDMI Analog Block Supply Voltage (1.8 V).
92	DVDD	Power	Digital Core Supply Voltage (1.8 V).
97	CVDD	Power	HDMI Analog Block Supply Voltage (1.8 V).
98	RXC_C−	HDMI input	Digital Input Clock Complement of Port C in the HDMI Interface.
99	RXC_C+	HDMI input	Digital Input Clock True of Port C in the HDMI Interface.
100	RXC_0−	HDMI input	Digital Input Channel 0 Complement of Port C in the HDMI Interface.
101	RXC_0+	HDMI input	Digital Input Channel 0 True of Port C in the HDMI Interface.
102	TVDD	Power	Terminator Supply Voltage (3.3 V).
103	RXC_1−	HDMI input	Digital Input Channel 1 Complement of Port C in the HDMI Interface.
104	RXC_1+	HDMI input	Digital Input Channel 1 True of Port C in the HDMI Interface.
105	RXC_2−	HDMI input	Digital Input Channel 2 Complement of Port C in the HDMI Interface.
106	RXC_2+	HDMI input	Digital Input Channel 2 True of Port C in the HDMI Interface.
107	CVDD	Power	HDMI Analog Block Supply Voltage (1.8 V).
108	RXB_C−	HDMI input	Digital Input Clock Complement of Port B in the HDMI Interface.
109	RXB_C+	HDMI input	Digital Input Clock True of Port B in the HDMI Interface.
110	RXB_0−	HDMI input	Digital Input Channel 0 Complement of Port B in the HDMI Interface.
111	RXB_0+	HDMI input	Digital Input Channel 0 True of Port B in the HDMI Interface.
112	TVDD	Power	Terminator Supply Voltage (3.3 V).
113	RXB_1−	HDMI input	Digital Input Channel 1 Complement of Port B in the HDMI Interface.
114	RXB_1+	HDMI input	Digital Input Channel 1 True of Port B in the HDMI Interface.
115	RXB_2−	HDMI input	Digital Input Channel 2 Complement of Port B in the HDMI Interface.
116	RXB_2+	HDMI input	Digital Input Channel 2 True of Port B in the HDMI Interface.
117	DVDD	Power	Digital Core Supply Voltage (1.8 V).
118	CVDD	Power	HDMI Analog Block Supply Voltage (1.8 V).
119	RXA_C−	HDMI input	Digital Input Clock Complement of Port A in the HDMI Interface.
120	RXA_C+	HDMI input	Digital Input Clock True of Port A in the HDMI Interface.

Pin No.	Mnemonic	Type	Description
121	RXA_0−	HDMI input	Digital Input Channel 0 Complement of Port A in the HDMI Interface.
122	RXA_0+	HDMI input	Digital Input Channel 0 True of Port A in the HDMI Interface.
123	TVDD	Power	Terminator Supply Voltage (3.3 V).
124	RXA_1−	HDMI input	Digital Input Channel 1 Complement of Port A in the HDMI Interface.
125	RXA_1+	HDMI input	Digital Input Channel 1 True of Port A in the HDMI Interface.
126	RXA_2−	HDMI input	Digital Input Channel 2 Complement of Port A in the HDMI Interface.
127	RXA_2+	HDMI input	Digital Input Channel 2 True of Port A in the HDMI Interface.
128	CVDD	Power	HDMI Analog Block Supply Voltage (1.8 V).

POWER SUPPLY RECOMMENDATION

POWER-UP SEQUENCE

The power-up sequence of the ADV7630 is as follows:

1. Hold $\overline{\text{RESET}}$ low.
2. Bring up the 3.3 V supplies (DVDDIO, TVDD, SYS_3P3V).
3. A minimum delay of 20 ms is required from the point at which the 3.3 V supplies reaches the minimum recommended value (3.14 V) before powering up the 1.8 V supplies.
4. Bring up the 1.8 V supplies (DVDD, TXA_PVDD, TXB_PVDD, CVDD, TX_AVDD). These should be powered up together, that is, there should be a difference of less than 0.3 V between them.
5. $\overline{\text{RESET}}$ can be pulled high after supplies have been powered up.
6. A complete reset is recommended after power-up. This can be performed by the system microcontroller.

POWER-DOWN SEQUENCE

The ADV7630 supplies can be de-asserted simultaneously as long as a higher rated supply does not go below a lower rated supply.

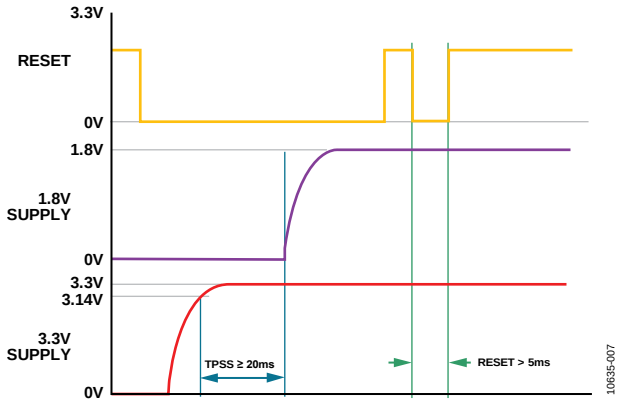


Figure 6. Supply Power-Up Sequence

FUNCTIONAL OVERVIEW

HDMI RECEIVER

The ADV7630 incorporates a 1:2 HDMI splitter with 4:1 multiplexed input receiver that supports all mandatory and many optional 3D formats, HDTV formats up to 1080p, and all display resolutions up to UXGA (1600 × 1200 at 60 Hz).

The inclusion of HDCP allows the ADV7630 to receive encrypted video content. The HDMI interface of the ADV7630 allows for the reception of two parallel and independent video streams including authentication of a video receiver, decryption of encoded data at the receiver, and the maintenance of that authentication during transmission, as specified by the HDCP 1.4 protocol.

The HDMI-compatible receiver on the ADV7630 incorporates an equalizer that compensates for the high frequency losses inherent in HDMI and DVI cabling, especially at longer lengths and higher frequencies. It is capable of equalizing for cable lengths up to 30 meters to achieve robust receiver performance.

XpressView fast switching can be implemented with full HDCP authentication available on the background port.

HDMI receiver features include:

- 1:2 HDMI splitter
- 4:1 HDMI input mux
- 3D format support
- 225 MHz HDMI receiver
- Integrated equalizer for cable lengths up to 30 meters
- HDCP 1.4 also on background ports
- Internal HDCP keys
- 36-/30-bit Deep Color support
- Repeater support
- Internal EDID RAM
- Hot plug assert output pin for each HDMI port
- CEC controller

HDMI TRANSMITTER

The ADV7630 features two HDMI transmitters: TXA and TXB. Both transmitters support 3D TV formats as well as all HDTV formats up to 1080p 36-bit Deep Color. The TXA and TXB transmitters have separate DDC lines to allow reading EDID data and performing HDCP operations authentication with two independent HDMI sinks.

Both transmitters feature an on-chip microprocessor unit (MPU) with an I^2C master to perform HDCP operations and EDID reading operations.

I^2C INTERFACE

The ADV7630 supports a 2-wire serial (I^2C-compatible) microprocessor bus driving multiple peripherals. The ADV7630 is controlled by an external I^2C master device, such as a microcontroller.

OTHER FEATURES

Other features include the following:

- Fully qualified software libraries, driver, and application
- Programmable interrupt request output pin (INT1)
- Chip select
- Temperature range: 0°C to 70°C
- 14 mm × 14 mm, Pb-free 128-lead TQFP with exposed pad

OUTLINE DIMENSIONS

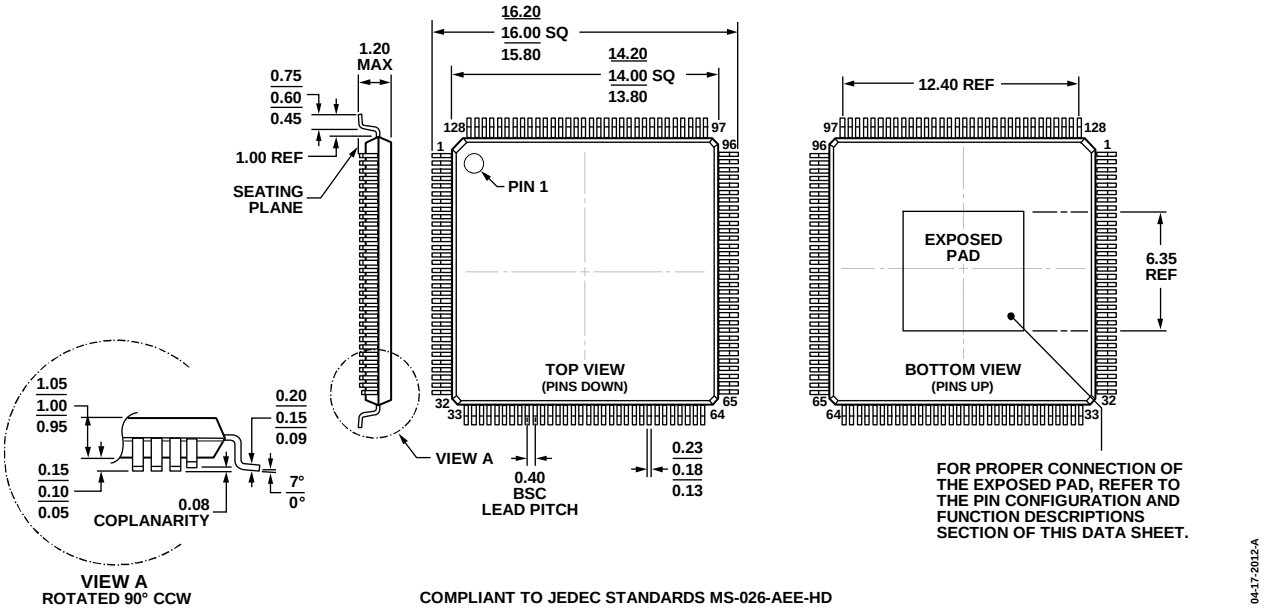


Figure 7. 128-Lead Thin Quad Flat Package, Exposed Pad [TQFP_EP]
(SV-128-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADV7630KSVZ	0°C to 70°C	128-Lead TQFP_EP	SV-128-1

[1] Z = ROHS Compliant.

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).
HDMI, the HDMI Logo, and High-Definition Multimedia Interface are trademarks or registered trademarks of HDMI Licensing LLC in the United States and other countries.