CS5518 Datasheet
MIPI DSI to LVDS Convertor

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1 Introduction

The Capstone CS5518 is a MIPI DSI input, LVDS output convert chip. The MIPI DSI supports up to 4lanes and each lane operates at 1Gbps maximum. The LVDS support 18 or 24-bits pixel with 25MHz to 154MHz, by VESA or JEIDA format. It can use only single 1.8V power supply for saves cost and optimizes board space.

The CS5518 is suitable for multiple market segments and display applications, such as handheld device, motherboard, dual panel display and car display etc.

Figure 1-1 CS5518 Block Diagram

2 Features

General

Embedded oscillator and there's no need for external crystal
Optional external clock input for 20-154MHz
Support SSC Generation +/-3% 100~300KHz for reduce EMI
Support Dithering and 6 bits + FRC.
Integrate PWM Generator with GPIO output PWM to control backlight
Internal power-on-reset (POR)

MIPI Input

Supports MIPI® D-PHY Version 1.00.00 and MIPI® DSI Version 1.02.00
Support 1-to-4 Data lanes, 1 Clock Lane
Bi-directional Lane 0 (Reverse only LP)
Support ULPS (Ultra Low Power State)
Support Packed Pixel Format RGB at 18/24/30/36 bits
Support Loosely Packed Pixel Format RGB at 18 bits
Support RGB565 16-bits input
DSI host can access local register in ESCAPE mode
Support Sync Event/Sync Pulse mode
Support Low Power Mode entry in all lines during V-blanking
Support Lane/Polarity swap
Support continuous clock and/or non-continuous clock

LVDS Output

Support 18-bit Single Port, 18-bit Dual Port, 24-bit Single Port and 24-bit Dual Port LVDS output interface.
Support speed up to 1.08Gbps/lane (154M pixel clock at single)
Support VESA and JEIDA mode
Flexible LVDS output pins swapping.
Programmable swing/common mode voltage.
Support Lane/Polarity/Bit swap

Misc.

Single 1.8V power supply mode.
Optional 3.3V power for IO power
Internal 1.2V LDO power supply
QFN48 7x7 package

3 Pin Definition

3.1 Pin Assignments

Figure 3-1 CS5518 Pin Layout

3.2 Pin Description

Table 3-1 CS5518 Pin Definitions

Pin #	Description	Type	Direction	Note
Power/Ground				
10	VDD18_33	P		1.8 or 3.3V Power for IO
11	VDD12_LDO	P		1.2V LDO output, must connect a 0.1uF and a 4.7uF for de-coupling

Pin #	Description	Type	Direction	Note
13	VDD18_RX	P		Analog 1.8V Power
35,38	VDD18_LVDS	P		Analog 1.8V Power
36	VDD18_PLL	P		Analog 1.8V Power
37	VSS_PLL	G		Analog Ground
5	GND	G		Digital Ground
e-PAD	GND	G		e-PAD must connect to GND
High-speed Rx Interface				
14,15	RX_0P/N	Analog	I	MIPI input data lane0
16,17	RX_1P/N	Analog	I	MIPI input data lane1
18,19	RX_CKP/N	Analog	I	MIPI input clock lane
20,21	RX_2P/N	Analog	I	MIPI input data lane2
22,23	RX_3P/N	Analog	I	MIPI input data lane3
High-speed Tx Interface				
34,33	A_Y0P/N	Analog	O	LVDS output port A data lane0
32,31	A_Y1P/N	Analog	O	LVDS output port A data lane1
30,29	A_Y2P/N	Analog	O	LVDS output port A data lane2
28,27	A_CKP/N	Analog	O	LVDS output port A clock lane
26,25	A_Y3P/N	Analog	O	LVDS output port A data lane3
48,47	B_Y0P/N	Analog	O	LVDS output port B data lane0
46,45	B_Y1P/N	Analog	O	LVDS output port B data lane1
44,43	B_Y2P/N	Analog	O	LVDS output port B data lane2
42,41	B_CKP/N	Analog	O	LVDS output port B clock lane
40,39	B_Y3P/N	Analog	O	LVDS output port B data lane3
Configuration				
1,2	SCL/SDA	LVTTL	I/O	I2C master or slave
3,4	GPIO_0/1	LVTTL	I/O	GPIO
6	IRQ	LVTTL	I/O	Interrupt out, also GPIO
7	I2C_ADDR	LVTTL	I	I2C address selection. High: chip address is 0x72/0x73 Low: chip address is 0x70/0x71(default)
8	I2C_TYPE	LVTTL	I	0: SCL/SDA are slave(default) 1: SCL/SDA are master
9	TEST_EN	LVTTL	I	Chip test mode enable, when work, must connect to GND.
12	CHIP_EN	LVTTL	I	Shut down chip if low
24	REFCLK	LVTTL	I	Optional reference clock for chip

4 Electrical Specifications

4.1 Absolute Maximum Conditions

Permanent damage may occur if absolute maximum conditions are violated. Refer to Section 4.2 for functional operating limits.

Table 4-1 Absolute Maximum Conditions

Symbol	Parameter	Min	Typ	Max	Unit
VDD18	1.8V power input	-0.3	—	2.16	V
VDD18_33	IO power input	-0.3	—	3.96	V
T_J	Junction temperature	-40	—	125	°C
T_{STG}	Storage temperature	-65	—	150	°C
ESD_{HBM}	ESD protection (Human body model)	—	—	±6	KV
ESD_{CDM}	ESD protection (Charge Device model)	—	—	700	V

1. Max 260°C can be guaranteed with max 8 sec soldering time.

4.2 Operating Conditions

Table 4-2 Normal Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
VDD12_OUT	1.2V LDO output	1.08	1.2	1.32	V
VDD18	1.8V power input	1.62	1.8	1.98	V
VDD18_33	IO power input	1.62	3.3	3.6	V
T_A	Ambient temperature	-10		70	°C
θ_{JA}	Package thermal resistance, no air flow	—	39.3	—	°C/W

4.3 Electrical Specification

Table 4-3 IO DC Electrical Specification

Symbol	Parameter	Min	Typ	Max
V_{il} (V)	Input low voltage	—	—	VIO *0.3
V_{ih} (V)	Input high Voltage	VIO *0.7	—	—
V_{ol} (V)	Output low voltage	0	—	VIO *0.3
V_{oh} (V)	Output high voltage	VIO *0.7	—	—
I_{in} (uA)	Input leakage current	-10	—	+10
I_{hiz} (uA)	Output tri-state leakage current	-10	—	+10

Table 4-4 MIPI RX HS DC Specification

Symbol	Description	Min	Typ	Max	Unit
$V_{CMRX(DC)}$	Common-mode voltage HS receive mode	70		330	mV
V_{IDTH}	Differential input high threshold			70	mV
V_{IDTL}	Differential input low threshold	-70			mV
V_{IHHS}	Single-ended input high voltage			460	mV
V_{ILHS}	Single-ended input low voltage	-40			mV
$V_{TERM-EN}$	Single-ended threshold for HS termination enable			450	mV
Z_{ID}	Differential input impedance	80	100	125	Ω

Table 4-5 MIPI RX HS AC Specification

Symbol	Description	Min	Typ	Max	Unit
$\Delta V_{CMRX(HF)}$	Common-mode interference beyond 450 MHz			100	mV
$\Delta V_{CMRX(LF)}$	Common-mode interference 50MHz – 450MHz	-50		50	mV
C_{CM}	Common-mode termination			60	pF

Table 4-6 MIPI RX LP DC Specification

Symbol	Description	Min	Typ	Max	Unit
V_{IH}	Logic 1 input voltage	880			mV
V_{IL}	Logic 0 input voltage, not in ULP State			550	mV
$V_{IL-ULPS}$	Logic 0 input voltage, ULP State			300	mV
V_{HYST}	Input hysteresis	25			mV

Table 4-7 MIPI RX LP AC Specification

Symbol	Description	Min	Typ	Max	Unit
e_{SPIKE}	Input pulse rejection			300	V·ps
T_{MIN-RX}	Minimum pulse width response	20			ns
V_{INT}	Peak interference amplitude			200	mV
f_{INT}	Interference frequency	450			MHz

4.4 Power Consumption

Different applications would result in different power consumptions of CS5518. For example, whether to adopt the embedded oscillator, and how fast of the video clock frequency are all definitely the key factors of the power consumption of CS5518. The following tables show the reference power consumption of CS5518 in several different application conditions.

Table 4-8 CS5518 Typical Power Consumption

Active Resolution (Pixel clock)	Min	Typ	Max	Unit
MIPI 1 lanes, LVDS 1 Port, 640x480x60 (25-MHz)	-	TBD	-	mA
MIPI 2 lanes, LVDS 1 Port, 1366x768x60 (85-MHz)	-	TBD	-	mA
MIPI 4 lanes, LVDS 2 Port, 1920x1080x60 (148-MHz)	-	TBD	-	mA

Note:

1. These power values tested on single 1.8V power supply mode.
2. In practice, the measured power consumption might be slightly different from the tables above due to the different video content and the different measurement equipment.

5 Package Specification

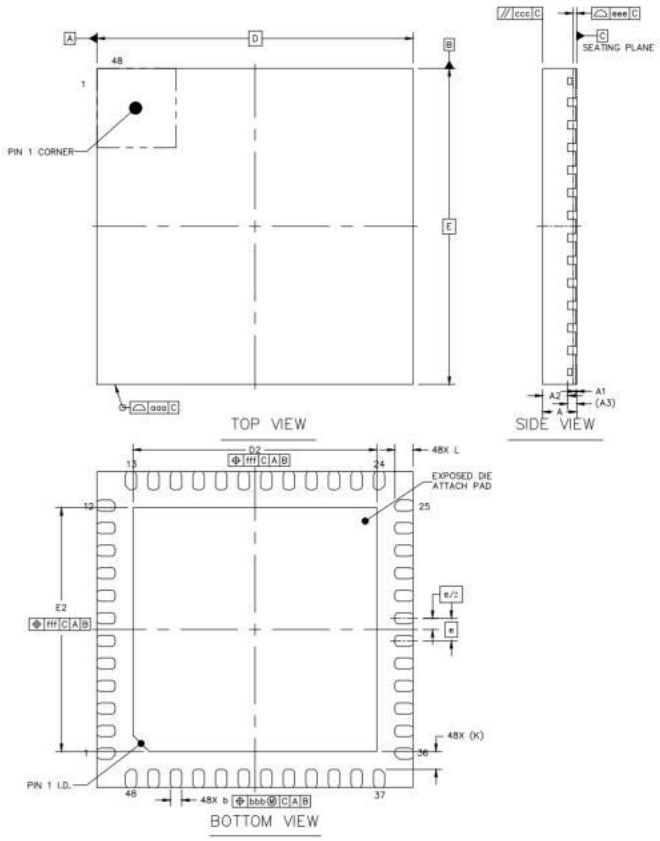

Figure 5-1 CS5518 Package Outline (QFN48 Leads 7x7mm)

Table 5-1 Package Dimension

Symbol	Dimension in mm			Dimension in inch		
	Min	Normal	Max	Min	Normal	Max
A	0.70	0.75	0.80	0.028	0.0295	0.031
A1	0.00	0.02	0.05	0.000	0.001	0.002
A2	—	0.55	—	—	0.022	—
A3		0.20 REF			0.008 REF	
b	0.2	0.25	0.3	0. 080	0.098	0.012
D/E		7.00 BSC			0.276 BSC	
D2/E2	5.3	5.4	5.5	0.209	0.213	0.217
e		0.50 BSC			0.020 BSC	
L	0.30	0.40	0.50	0.012	0.016	0.020
K		0.4 REF			0.016 REF	0.

6 Ordering Information

The CS5518 can be ordered using the part numbers in Table 6-1. Please consult sales for further details.

Table 6-1 CS5518 Ordering Information

Part No.	Description	Temperature Range	MSL	Environment Compliance	Packing Type
CS5518AN	48 Pin (QFN) Lead-free package	Commercial: 0 to 70 degree C	Level 3	Green	5K / T &R

Table 6-2 CS5518 Marking Information

Line No.	Description	Temperature Range
Line1	CS5518	Product Name
Line2	XXXXXX	Lot #
Line3	YYWW	YYWW: Date code
Line4	PIN1 indicator	

Figure 6-1 CS5518 Marking

7 Revision History

Table 7-1 Document Revision History

Revision	Date	Changes
V0.1	Mar. 2022	draft version
V1.0	Sep. 2022	Update chip marking