扩展 RISC-V 的芯边界- Andes 最新的處理器核介绍

晶心科技 市场部
资深技术经理 胡鸿光

Andes Technology Corporation 晶心科技

Who We Are

CPU Pure-play CPU IP Vendor

Founded in 2005, IPO 2017 (6533 TW). 18 years old company

Active Open-Source Contributor/Maintainer

Activities in RISC-V International (RVI)

Founding & Premier Member

- Board of Directors
- Technical Steering Committee
- Ambassador

P-Extension TG

TEE/IOPMP TG

Fast Intr. TG

Quick Facts

>300 people
80% are engineers

US$127M
GDR offering in Sep. 2021

12B+ SoC
Total customer shipment

80K+ users
for AndeSight™ IDE

Andes Core Is Everywhere

D25F, D45, AX25MP, AX45MP

N25F, N45, AX45MP

N25F, N45

From the Edge, To the Cloud, Into the Space

NX27V, AX25, AX27, AX45MP, AX45MPV

N25F

N25F, A25, A45MP, AX45MP

AndesCore™ Lineup

AX60 Series 13-stage OOO MP	AX6x-SE		AX65		A72~A76; X1/V1
Categories	***FUSA***	*Power-efficient*	*Mid-range*	*Extended*	
45 Series 8-stage superscalar	D45-SE	N45, NX45	D45 NX45V*	A45(MP), AX45(MP) AX45MPV	A53/55, R52/82, M7
27 Series 5-stage MemBoost			NX27V	A27(L2) AX27(L2)	A5/7/35
25 Series 5-stage fast & compact	N25F-SE D25F-SE*	N25F, NX25F	D25F	A25(MP) AX25(MP)	A5/7/35, R4/5, M4/33
Entry Series	D23-SE	N22	D23		M0/0+/3/33/4
Categories	*FUSA*	*Embedded*	*DSP/Vector*	*Linux AP*	*References*

*Note *: AX45MPV configured as single core. *D25F-SE is a variation of N25F-SE, N25F-SE is available now*

- **Upcoming new cores:** AX45MPV, AX65, D25F-SE, D23
- **Automotive Safety Enhanced Series:** at least one per year

Note: roadmap subject to change without notice

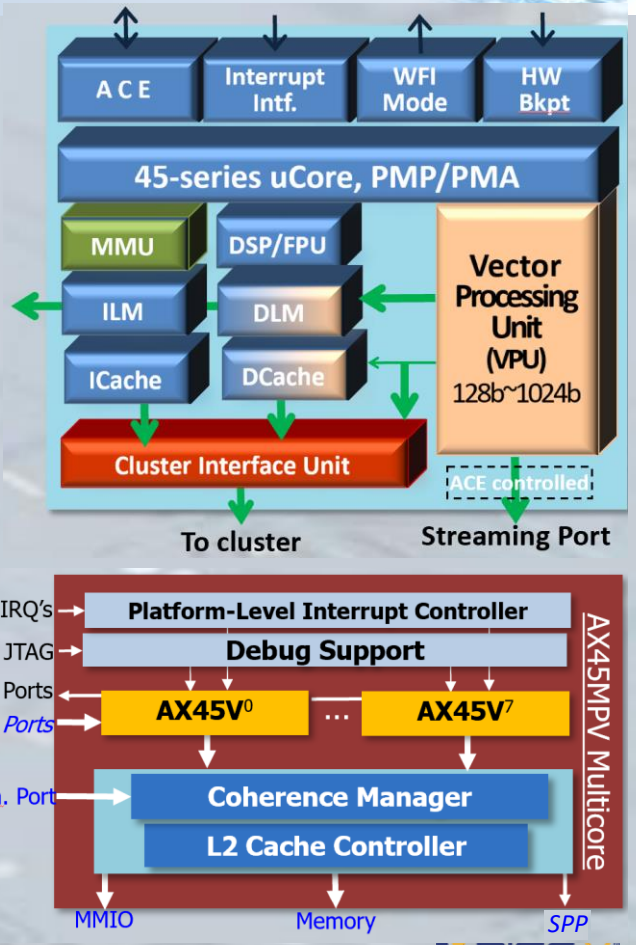
AndesCore™ AX45MPV

Multicore 1024-bit Vector Processor

多核心 1024位向量处理器

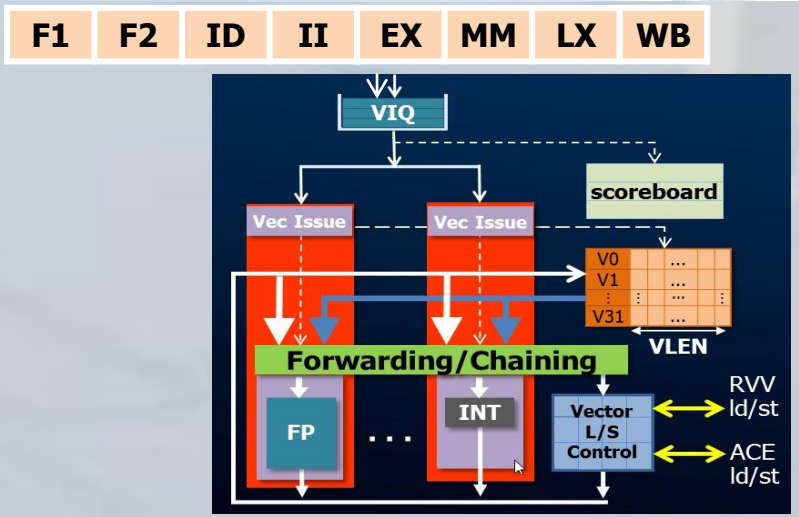
AX45MPV Core and Multicore Cluster

- **ISA: RV64GCBP* + V**
- **8-stage In-order dual-issue**
- **Scalar Unit: configurable**
  - MMU/SV48, M/S/U modes
  - FPU, DSP
  - I/D LM: 0~16MB, dynamic wait-cycle, and ECC
  - I/D caches: 8K~64KB; Parity (I$) or ECC (both)
  - Andes Custom Extension™ (ACE)
- **CM/L2$ subsystem**
  - 128KB to 8MB, 64B line, 16-way
  - Multi-cycle support for high-density SRAMs
  - Instruction/data prefetch, up to 64 outstanding request
- **AXI Bus Interfaces:**
  - Bus clock: N-to-1 or asynchronous
  - Width: 128/256/**512** bits except 64-bit SPP

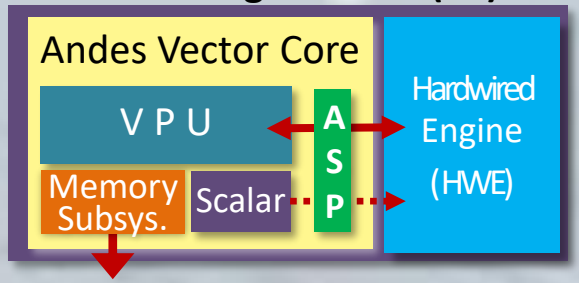


AX45MPV: 1024-bit VPU

- **RISC-V Vector Extension (RVV v1.0)**
  - data format: int8~64, fp16~64; int4, **bf16**
  - VLEN/DLEN: 128~**1024** bits, 1:1 or 2:1 ratio
  - Up to 5 DLEN results per cycle (6 with FMAC2)
- **Vector pipeline:**
  - Up to 2 RVV instructions/cycle can enter VIQ in EX
  - Instructions start execution after *committable*
  - Most functional Units are pipelined and chainable
    - INT: ALU, MUL/DIV, Permute
    - FP: FMAC1, FMAC2, FMISC
    - Others: LDST, ACE-RVV
- **ACE** enables flexible compute and comm. to HWE
  - Andes Streaming Port™ (ASP)
    - Data bus: data transfer btw VR and HWE
    - Command bus: control info to perform custom operations
  - ACE-RVV: custom RVV instructions performed inside VPU



Processing Element (PE)



NX45V (AX45MPV Single Core) vs. NX27V

- **Advantages:**
  - Dual-issue: help non-MAC dominated loops on the same VPU config
  - 1024-bit VLEN/DLEN: boost performance greatly for MAC dominated loops
  - 2x outstanding memory transactions: speed up memory-bound loops
- **Performance Comparison** (when VLEN/DLEN are the same):
  - Compute-bound loop: 20%~40% faster
  - Memory-bound loop: 30~50% faster

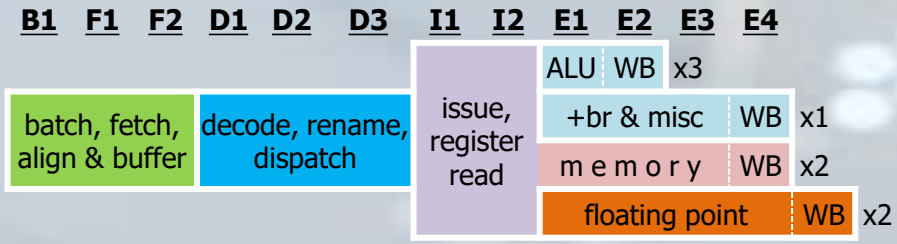
AndesCore™ AX65

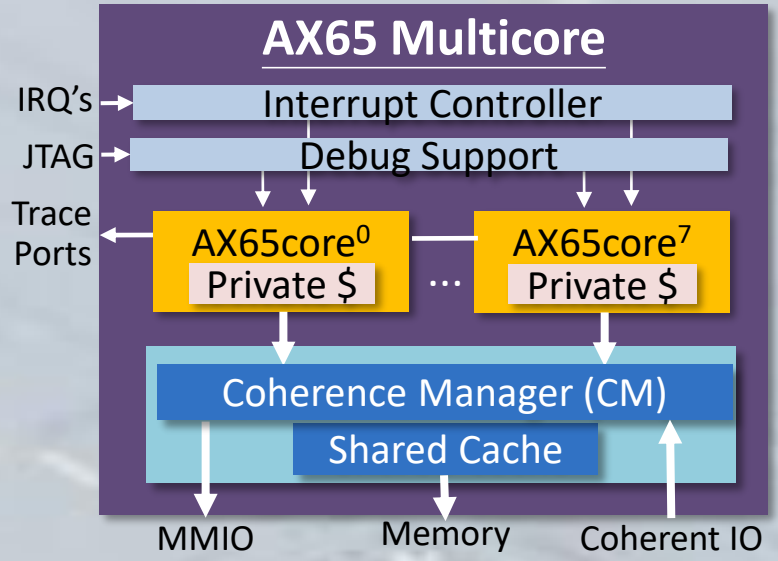
Multicore Out-of-Order Processor

多核心超纯量乱序处理器

AndesCore AX65: 1st Member of AX60-Series

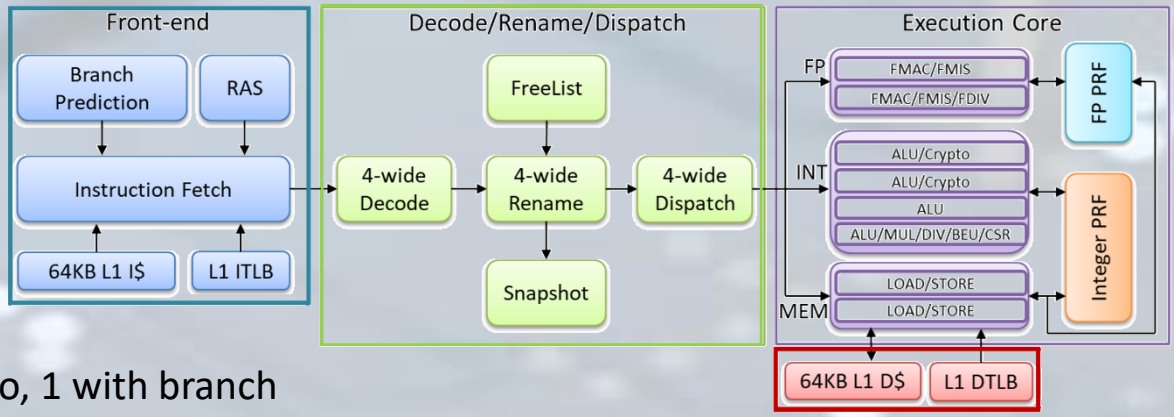
- RV64GCBK, SV48+VM extensions, ePMP
- 4-way 13-stage OOO superscalar
- Multicore cluster: 1~8 cores
- Private caches (I/D):
  - 64KB, 64B lines, 4-way, banked
  - VIPT with HW handling of VA aliasing
- Shared cache: up to 8MB
- CPU and CM: sync or async clocks
- 256-bit bus ports:
  - Types: Memory, MMIO, Coherent IO
  - Requests for uncached loads/stores are shared/merged for best efficiency





AX65 Microarchitecture: Overview

- **Two 8-byte fetches/cycle**
- **Branch prediction:**
  - TAGE and 2-level BTB
  - 9-cycle misprediction penalty
- **ROB/Freelist:** 128/128
- **Execution pipes:**
  - 4 integer ALUs: 2 with scalar crypto, 1 with branch
  - 2 full load/store units
  - 2 FPUs: one full, one without divide/sqrt
- **Split 2-level TLB:** L1 up to 32 entries, L2 up to 1024 entries
  - Combining 2 consecutive L1 entries
  - Aggressive concurrent HW page table walkers: 2 x instruction, 4 x data
- **Load/store units:** up to 64 outstanding instructions
- **Total requests/core:** >20 outstanding requests



Preliminary Performance Results

AndesCore	AX27L2	AX45MP (over AX27L2)	AX65 (over AX45MP)
Micro-architecture	5 stage scalar in-order	8 stage dual-issue in-order	13 stage quad-issue OOO
Freq. (7nm)	~2 GHz	>2 GHz	>2.5 GHz
Coremark/MHz	3.55	5.64 (+59%)	9.17 (+63%)
EEMBC FPMark/MHz	27.0	35.2 (+30%)	66.6 (+89%)
Linpack MFLOPS/MHz	0.130	0.220 (+69%)	0.613 (2.8x)
Mem Bandwidth[1]/MHz	1.0x	1.47x	1.90x
Specint2k6/GHz	2.82	3.46 (+23%)	> 7 (>2x, target)

1. Based on standard library memcpy

AndesCore® D25F-SE

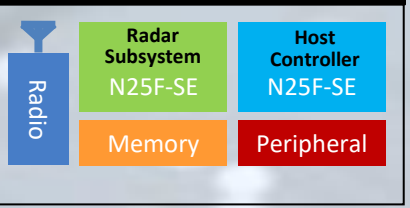
Automotive Functional Safety(FUSA)

车用强化安全处理器

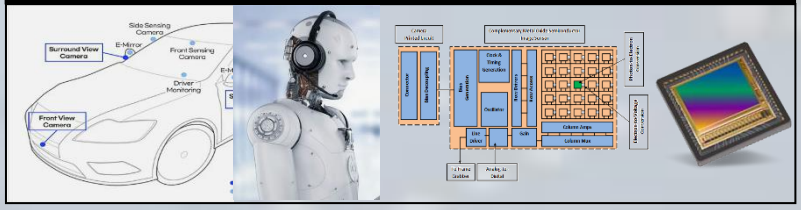
New Frontier – FUSA and Automotive

with Industry's 1st RISC-V ISO 26262 Fully Compliant Core, N25F-SE

In-Cabin Radar



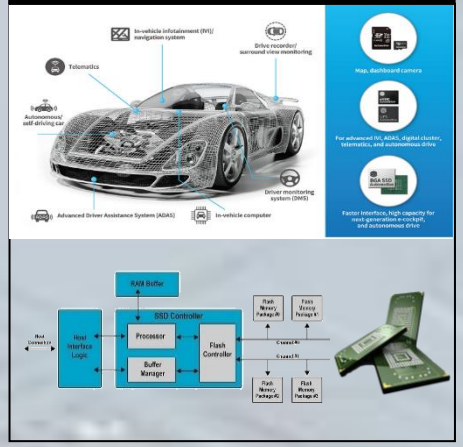
CMOS Sensor



Auto TDDI

Auto MCU

Auto Storage



Prerequisites for Developing FUSA Products

- **ISO 9001 Quality Management System**
  - In **April 2010**, Andes certified by DQS Inc.
  - Continue to maintain it since then
- **ISO 26262 Certification for Development Process: ASIL-D**
  - In **Dec. 2020**, Andes certified by SGS-TÜV Saar GmbH

CERTIFICATE

This is to certify that

Andes Technology Corporation
10F, No. 1, Sec. 3, Gongdao 5th Rd., East Dist.
Hsinchu City, 300042
Taiwan R.O.C.

has implemented and maintains a Quality Management System.

Scope:
The design and development of CPU cores, and companion IPs.
The provision of CPU architectures, hardware development platforms, software integrated development environment, and associated target software infrastructure.

Through an audit, documented in a report, it was verified that the management system fulfills the requirements of the following standard:

ISO 9001 : 2015

Certificate registration no.	20004946 QM15
Date of original certification	2010-04-11
Date of revision	2021-05-01
Date of certification	2021-05-18
Valid until	2024-05-17

DQS Inc.

Brad McGuire
Managing Director

Accredited Body: DQS Inc., 1500 McConnor Parkway, Suite 400, Schaumburg, IL 60173 USA
Administrative Office: DQS Taiwan Inc., 9F, 23, Yuan Huan West Road, Feng Yuan Dist., Taichung City, Taiwan 420

SGS TÜV SAAR

CERTIFICATE NO.: FS/71/220/20/0639 PAGE 1/1

LICENCE HOLDER

ANDES TECHNOLOGY CORPORATION
10F., NO. 1, SEC. 3, GONGDAO 5TH RD., EAST DIST.,
HSINCHU CITY
TAIWAN R.O.C 30069

Project-No/-ID	LICENSED TEST MARK	Report No.
P30L	SGS TÜV SAAR FUNCTIONAL SAFETY APPROVED	P30L0001

Tested according to	ISO 26262:2018
Certified Process	Development process for Functional Safety related components up to ASIL D Version V1.0/202011
Technical Data/Parameter	The audited development process complies with the ISO 26262 standard part requirements ISO 26262-2:2018, ISO 26262-6:2018 ISO 26262-4:2018, ISO 26262-8:2018 ISO 26262-5:2018, ISO 26262-9:2018
Specific Requirements	The certificate is created for the purpose of providing conformity of the development and support process in accordance with ISO 26262. Changes which are not covered in the Audit Report have to be reconsidered.

Certification Body
for Functional Safety
SGS-TÜV Saar GmbH

Munich, December 22nd, 2020

Marcus Rau

The test mark regulation is an integral part of this certificate.

CERTIFICATE

N25F-SE ISO 26262 Certificate

SGS TÜV SAAR

CERTIFICATE NO.: FS/71/220/22/0970 PAGE 1/1

LICENCE HOLDER

ANDES TECHNOLOGY CORPORATION
10F., NO. 1, SEC. 3, GONGDAO 5TH RD., EAST DIST.,
HSINCHU CITY 300042,
TAIWAN, R.O.C.

Project-No/-ID	LICENSED TEST MARK	Report No.
S280	SGS TÜV SAAR ASIL B COMPLIANT Functional Safety ISO 26262	S2800001

Tested according to ISO 26262:2018 (Parts 2, 4 partly, 5, 8, 9)

Certified Product(s) **CPU IP "N25F-SE"**
Version: R320

Technical Data/Parameter The above-mentioned product has been approved in a standard configuration (see certification report for details). The identified technical and process parameters are in compliance with **ASIL B** requirements.

Specific Requirements The certificate is for type approval and based on a detailed functional safety assessment. Any changes to the design or processes may require repetition of some of the assessment steps in order to retain type approval.
The certificate report is an integral part of this certificate. All requirements and specifications of the current valid revision of this report shall be met.

Certification Body for Functional Safety SGS-TÜV Saar GmbH

The validation status is documented via SGS Certification Database.

The test mark regulation is an integral part of this certificate.

Munich, October 28th, 2022

Marcus Rau

SGS-TÜV Saar GmbH, Hofmannstr. 50, D-81379 München, Deutschland / Germany.
Website: www.sgs-tuv-saar.com/fs
E-Mail: fs@sgs.com

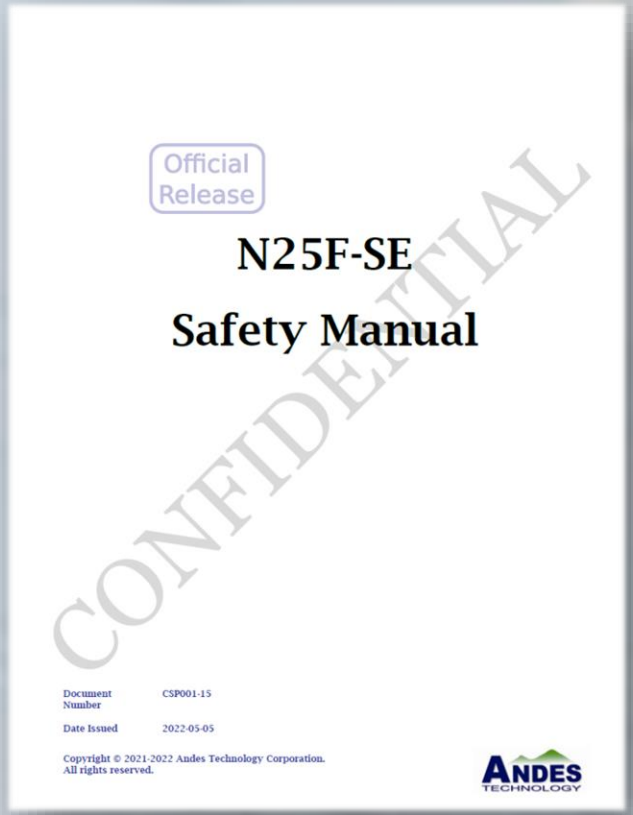
CERTIFICATE

- **ISO 26262 Edition 2018**
- **ASIL B Compliant**
- **Parts:**
  - ISO 26262-2,4,5,8,9
  - Covers all the sections applicable to CPU core
- **Certification Body**
  - SGS-TÜV Saar GmbH

✓ SGS technical report with German accreditation body DAkkS logo

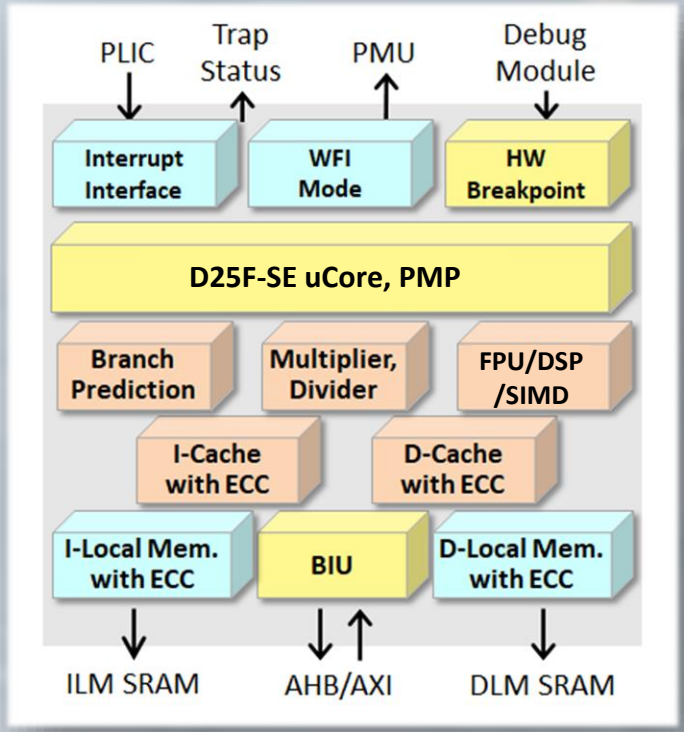
The N25F-SE Safety Manual

- **Safety Manual**
  - Provide information for designers to develop safety products integrating the supported core
- **The Contents**
  1. Overview
  2. Safety Lifecycle
     - Safety managements, confirmation measures
  3. Assumption of Safety Requirements
     - Safety goals, safety requirements, D-FMEA
  4. N25F-SE IP Safety Architecture Overview
     - Safety features
  5. Configuration Options
  6. Fault Detection and Control Mechanisms
     - Internal and external safety mechanisms
  7. Assumption of Use
  8. Safety Analysis Results
     - FMEDA, DFA



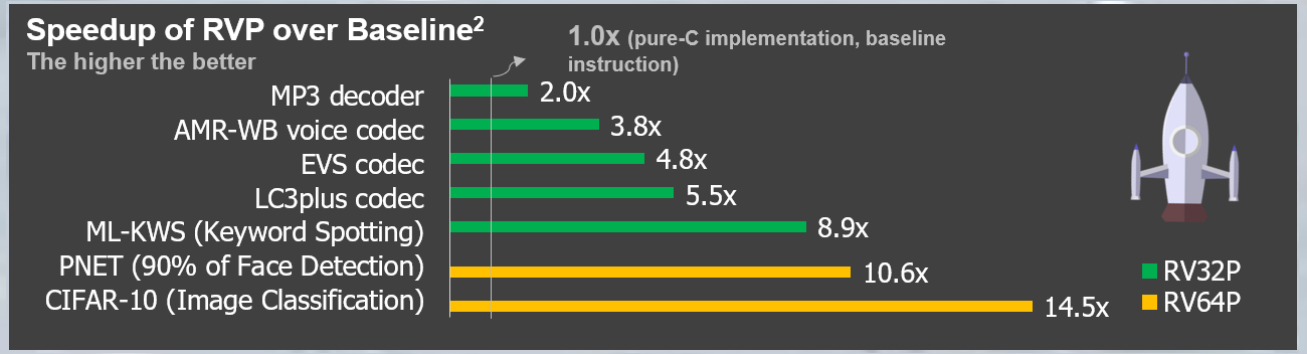
D25F-SE Key Features

- **CPU Core**
  - AndeStar™ V5 Instruction Set Architecture (ISA)
    - RISC-V 32-bit, RV32IMACFD + Andes Extensions
    - RISC-V P(draft) and B extensions.
    - 16 Physical Memory Protection (PMP) regions
    - Machine+User (M+U) privilege levels
  - 5-stage pipeline architecture
  - Dynamic branch prediction with BTB, BHT, RAS
  - CoDense™ code size reduction, StackSafe™ stack protection
- **Memory Subsystem**
  - Support I/D cache up to 32KB each,
  - Support I/D local memory up to 16MB each, with slave port interface for bus masters direct accesses
- **Bus Interfaces**
  - AXI or AHB bus master port
  - N:1 CPU clock vs. bus clock ratio
- **Others**
  - Platform-Level Interrupt Controller (PLIC), WFI power management, Debug interface



D25F-SE with DSP and Bit-manipulation

- **RVP: Powerful SIMD/DSP instructions for audio/voice codec and endpoint AI/ML**
- **SIMD instructions such as a quad 8 x 8 accumulated into 32-bit data**
- **DSP library support of over 200 functions**



- **RVB: Efficient bit-manipulation operations for codes such as cryptographic & checksums**
  - Latest RVB ISA-extension Ver 1.0.0, including:
    - address generation, basic bit-manipulation, carry-less multiplication and single-bit instructions
    - Accelerate Crypto calculations: **27%** improvement on SHA256, **19%** for AES, **16%** for MD5

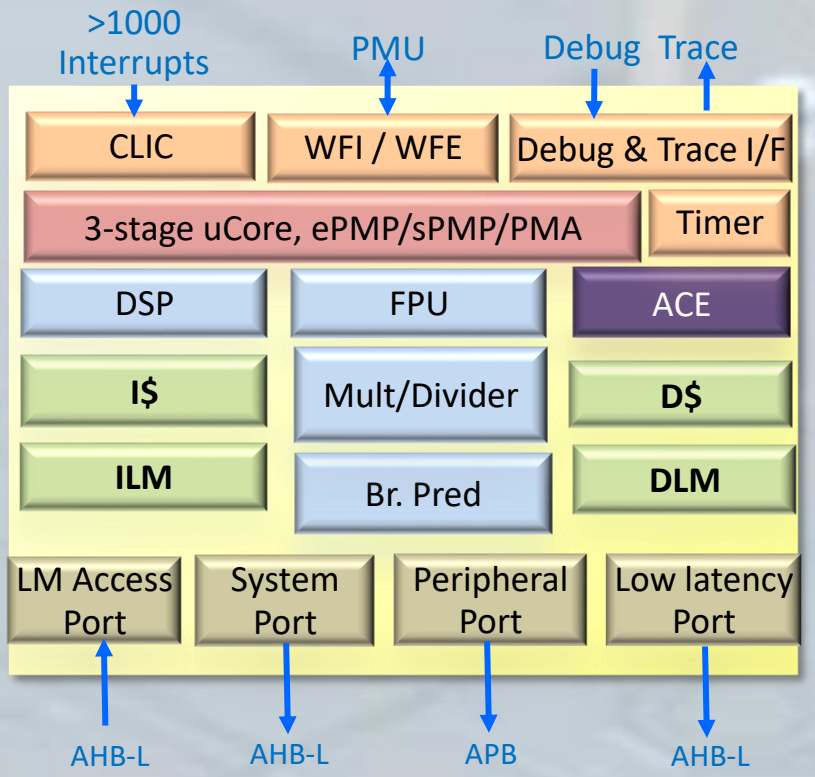
AndesCore® D23

Compact and Secure Controller

功能丰富且高度安全的入门级处理器

D23: Compact Controller

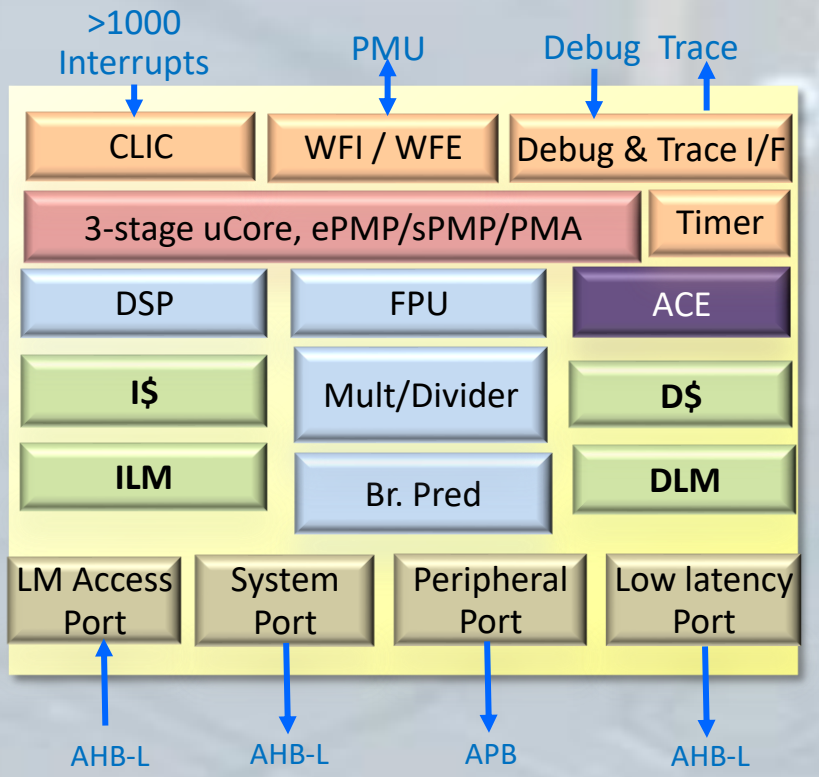
- **3-stage, limited dual-issue (optional)**
- **ISA extensions:**
  - Base: RV32 I[E]MAC + B+ Zce (compressed Inst)
  - Advanced: FD + *P+ K(crypto) + CMO(cache)
- **Privilege modes: M, S, U**
- **Configurable features**
  - Branch prediction: none, static, dynamic
  - Multiplier options:
    - Sequential: 1/2/4/8-bit per cycle
    - Fast: pipelined
  - *Andes Custom Extension ™ (ACE)*
  - Power management: WFI/WFE, PowerBrake
  - Core-Local Interrupt Controller (CLIC)
    - >1000 sources, 255 priority levels
    - Selective vectoring with priority preemption



*P: draft

D23: Compact Controller

- **Memory subsystem:**
  - Caches:
    - Config: Icache only, Icache with RO data; I/D caches
    - Cache sizes: 1KB~32KB
    - Error protection: Parity for I$; ECC for I$ and D$
  - I/D Local Memory (LM):
    - 0~512MB with ECC
    - Interface: SRAM or AHB-L
  - Enhanced/supervisor PMPs: up to 32 entries
  - PMA: up to 8 entries
- **Benchmarks and PPA at 28nm**
  - >4.1 Coremark/MHz and >2.0 DMIPS/MHz
  - Max. freq. (worst case): up to 800MHz
  - Gate count: <30K (for min. useful configuration)



Andes Tools and Software Solutions

AndeSight™ IDE
with AndeSoft™ BSP inside

- User-friendly IDE with **rich GUI features**
- Highly-optimized **GCC/LLVM** for speed & size
- Abundant **demos** to jumpstart development
- Rich **RTOSes** and LTP-verified **Linux**
- Optimized RVP/RVV **compute libraries**
- **Drivers** for AndeShape™ platform IP's
- Arduino support for Andes EVB

AndeSoft™ NN Library

Optimized for RISC-V DSP/SIMD and Vector ext'

COPILOT for ACE

Auto-generation of toolchains, ISS and RTL for user-defined instructions

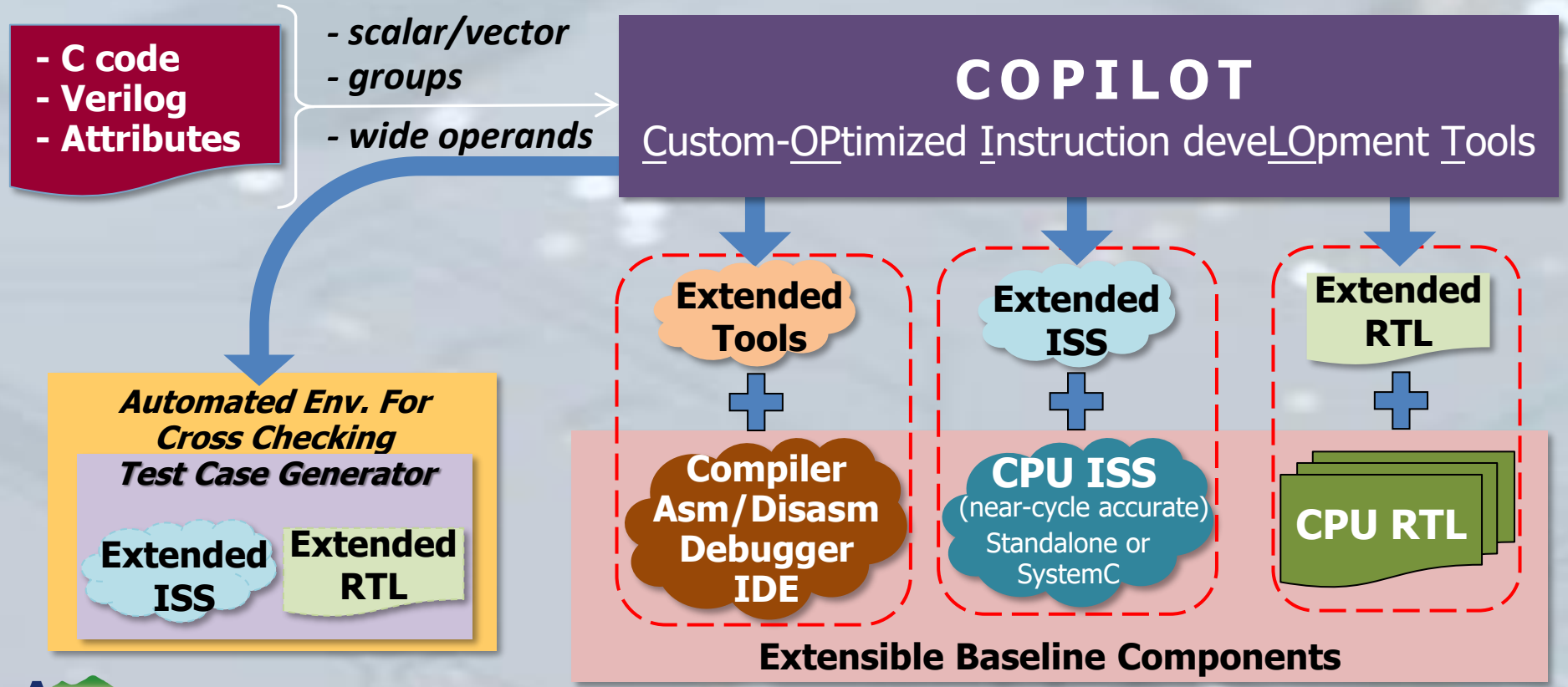
AndesClarity™

Processor **Pipeline Analyzer/Visualizer**, esp. powerful for vector processors

AndeSysC™

Near-cycle accurate SystemC processor models

COPILOT for ACE



Expanding RISC-V Beyond the Horizon

- RISC-V is a leading choice of processors for SoC and Computing Platforms
- Andes continues to develop high quality RISC-V solutions

AX65	AX45MPV
Multicore Out-Of-Order Application Processor	Multicore 1024-bit Vector Processor
D23	**D25F-SE**
Tiny and Secured Processor	ISO 26262 Fully-Compliant Processor

- Andes CPU cores, Tools and SW and partners are best to help customers succeed

Andes Embedded™

~18 years, 300+ customers, 80K+ IDE users, 12B+ customer SoC

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sales@andestech.com

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