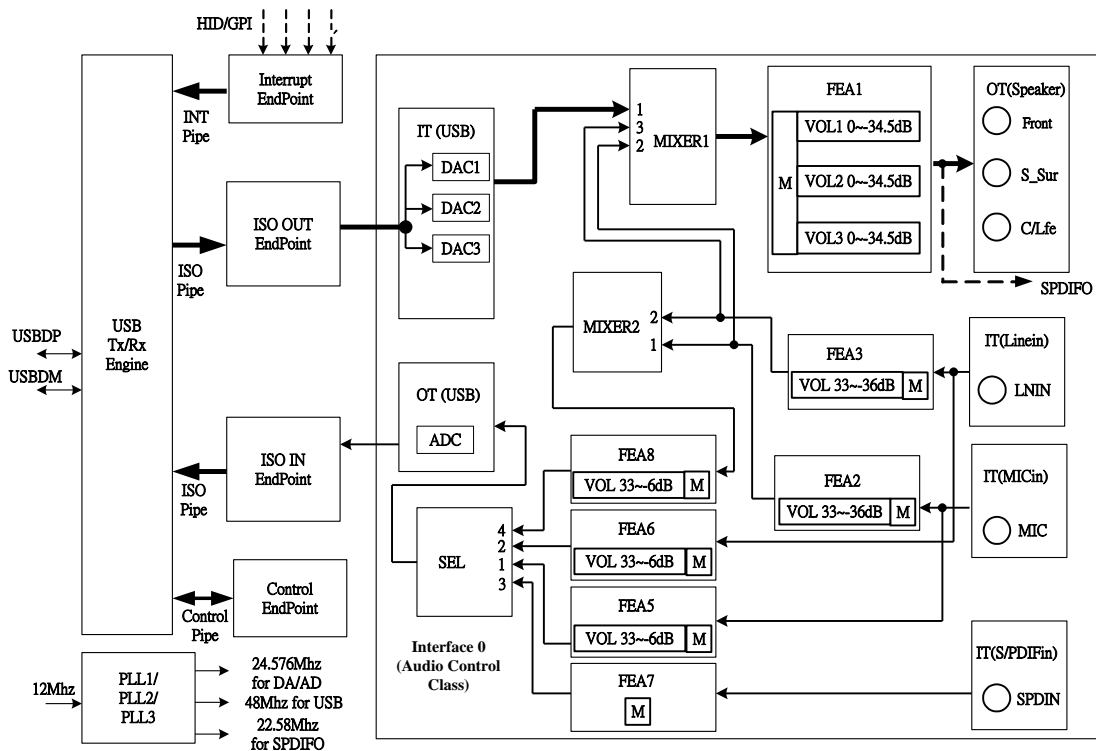


### DESCRIPTION

CM6206LX is a highly integrated single chip USB audio solution. All essential analog modules are embedded in CM6206LX, including 6CH DAC and earphone buffer, 2CH ADC, microphone gain, PLL, regulator, and USB transceiver. It is very suitable for high end USB external audio box, USB multi-channel headphone or USB audio interface multi-channel speaker set application.

Many features are programmable with external EEPROM and MCU interface. In addition, MCU/EEPROM/GPIO control can easily via HID software interface. Better yet, CM6206LX support stereo MIC, phone jack sense, S/PDIF I/O 48 KHz sampling rate. Moreover, unique patent driver can support world's first SPEAKER SHIFTER, Karaoke and Dolby AC-3 real-time encoder functions.

### BLOCK DIAGRAM



### FEATURES

- USB spec. 2.0 full speed compliant
- USB audio device class spec. 1.0 and USB HID class spec. 1.1 compliant
- IEC60958 spec. compliant (consumer format S/PDIF input and output with loop-back support)
- SCMS (Serial Copy Management System) compliant
- Dolby® digital audio streaming via S/PDIF output interface
- USB remote wake-up support
- 6 channel DAC output with 16 bit resolution
- 3.1 Vpp (1.1 Vrms) biased at 2.25V output swing
- Volume control and mute function
- Earphone buffer
- Self power / Bus power selectable (by EEPROM)
- 2X interpolator for digital playback data to improve quality
- 2 channel ADC input with 16 bit resolution



### Release Note

| Revision | Date       | Description                                                  |
|----------|------------|--------------------------------------------------------------|
| 1.6      | 2012/05/02 | -remove Cmedia old logo<br>-remove MCU<br>-remove codec mode |
| 1.7      | 2012/10/19 | -Change Pin 13 to reserve.                                   |
| 1.9      | 2013/10/30 | -Change pin 16, 17 description                               |
|          |            |                                                              |
|          |            |                                                              |
|          |            |                                                              |
|          |            |                                                              |

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## 1 Description and Overview

CM6206LX is a highly integrated single chip USB audio solution. All essential analog modules are embedded

in CM6206LX, including 6CH DAC and earphone buffer, 2CH ADC, microphone gain, PLL, regulator, and USB transceiver. It is very suitable for high end USB external audio box, USB multi-channel headphone or USB audio interface multi-channel speaker set application.

Many features are programmable with external EEPROM and MCU interface. In addition, MCU/EEPROM/GPIO control can easily via HID software interface. Better yet, CM6206LX support stereo MIC, phone jack sense, S/PDIF I/O 48 KHz sampling rate. Moreover, unique patent driver can support world's first SPEAKER SHIFTER, Karaoke and Dolby AC-3 real-time encoder functions.

## 2 Features

- USB spec. 2.0 full speed compliant
- USB audio device class spec. 1.0 and USB HID class spec. 1.1 compliant
- IEC60958 spec. compliant (consumer format S/PDIF input and output with loop-back support)
- SCMS (Serial Copy Management System) compliant
- Dolby® digital audio streaming via S/PDIF out S/PDIF output interface
- USB remote wake-up support
- 6 channel DAC output with 16 bit resolution
- 3.1 Vpp (1.1 Vrms) biased at 2.25V output swing
- Volume control and mute function
- Earphone buffer
- 2X interpolator for digital playback data to improve quality
- 2 channel ADC input with 16 bit resolution
- 3.2 Vpp (or 4.0 Vpp programmed by vendor driver) biased at 2.25V input swing
- Volume control and mute function
- Isochronous transfer using adaptive synchronization with internal PLL
- Stereo MIC support with 33dB maximum capability
- Recording source select from S/PDIF, MIC, Line-in and summation of MIC, Line-in and front channel
- MIC, Line-in monitor from front channel (all channels optional) with volume control and mute function
- Master volume control by default; per-channel volume control by C-Media driver
- Playback with soft-mute function
- Support 48 / 44.1 KHz sampling rate for both playback and recording
- MCU support with two-wire serial interface
- Serial EEPROM support for customized VID/PID
- MCU / EEPROM / GPIO control via HID software interface
- Volume up / volume down / playback mute HID button
- LED indicator pins: operation / recording mute / SCMS protection
- C-Media value added software (multi-channel positional 3D sound, AC-3 encoder, etc.)
- Embedded USB transceiver and power on reset circuit

# CM6206LX

High Integrated USB Audio I/O Controller

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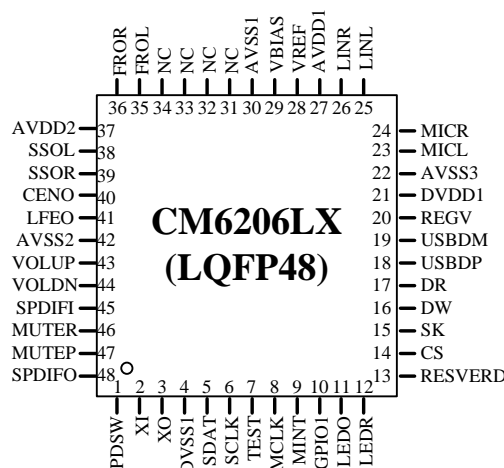
- Microsoft Vista Premium Level Compliant
- Single 12MHz crystal input with embedded PLL
- Single 5V power supply with embedded 5V to 3.3V regulator
- Industry standard LQFP-48 package
- C-Media value added patent software driver:
  - Xear 3D sound
  - Earphone Plus
  - SPEAKER SHIFTER
  - Environment sound effects
  - Room Size Mode
  - Graphic Equalizer
  - Karaoke Function
  - Dolby Digital Real-Time Content Encoder (Optional)

### 3 Pin Descriptions

#### 3.1 CM6206LX LQFP 48Pin Table

| PIN # | Signal Name | PIN # | Signal Name | PIN # | Signal Name |
|-------|-------------|-------|-------------|-------|-------------|
| 1     | PDSW        | 17    | DR          | 33    | N.C         |
| 2     | XI          | 18    | USBDP       | 34    | N.C         |
| 3     | XO          | 19    | USBDM       | 35    | FROL        |
| 4     | DVSS1       | 20    | REGV        | 36    | FROR        |
| 5     | SDAT        | 21    | DVDD1       | 37    | AVDD2       |
| 6     | SCLK        | 22    | AVSS3       | 38    | SSOL        |
| 7     | TEST        | 23    | MICL        | 39    | SSOR        |
| 8     | MCLK        | 24    | MICR        | 40    | CENO        |
| 9     | MINT        | 25    | LINL        | 41    | LFEO        |
| 10    | GPIO1       | 26    | LINR        | 42    | AVSS2       |
| 11    | LEDO        | 27    | AVDD1       | 43    | VOLUP       |
| 12    | LEDR        | 28    | VREF        | 44    | VOLDN       |
| 13    | RESERVED    | 29    | VBIAS       | 45    | SPDIFI      |
| 14    | CS          | 30    | AVSS1       | 46    | MUTER       |
| 15    | SK          | 31    | N.C         | 47    | MUTEP       |
| 16    | DW          | 32    | N.C         | 48    | SPDIFO      |

Figure 1. CM6206LX LQFP 48 Pin Assignments (Top View)



### 3.2 CM6206LX LQFP 48 PIN

| Pin # | Symbol   | Type | Description                                                                                                                                                                 |
|-------|----------|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1     | PDSW     | DO   | Power down switch control (for PMOS polarity)<br>0: normal mode<br>1: power down mode                                                                                       |
| 2     | XI       | DI   | 12MHz crystal, or oscillator input                                                                                                                                          |
| 3     | XO       | DO   | 12MHz crystal output                                                                                                                                                        |
| 4     | DVSS1    | P    | Digital ground                                                                                                                                                              |
| 5     | SDAT     | DIO  | External MCU serial bus data pin                                                                                                                                            |
| 6     | SCLK     | DI   | External MCU serial bus clock pin                                                                                                                                           |
| 7     | TEST     | DI   | Test mode select pin; pull low in normal operation                                                                                                                          |
| 8     | MCLK     | DO   | External MCU clock pin; clock frequency is programmable<br>(12MHz, 6MHz, 3MHz, 1.5MHz)<br>Default is 1.5 MHz                                                                |
| 9     | MINT     | DO   | External MCU interrupt pin (active L)<br>When internal register address 0 ~ 3 or external serial EEPROM is accessed,<br>MINT is set low; after MCU read, MINT is reset to H |
| 10    | GPIO1    | DIO  | GPIO pin #1                                                                                                                                                                 |
| 11    | LEDO     | DO   | LED for operation; output H for power on; toggling for data transmit                                                                                                        |
| 12    | LEDR     | DO   | LED for mute recording indication; output H when recording is muted                                                                                                         |
| 13    | RESERVED | DI   | Request connect a resistor 10K ohm to Digital ground                                                                                                                        |
| 14    | CS       | DO   | Chip Select for EEPROM                                                                                                                                                      |
| 15    | SK       | DO   | Serial Data Clock to EEPROM                                                                                                                                                 |
| 16    | DW       | DO   | Serial Data Output to EEPROM                                                                                                                                                |
| 17    | DR       | DI   | Serial Data Input from EEPROM                                                                                                                                               |
| 18    | USBDP    | AIO  | USB data D+                                                                                                                                                                 |
| 19    | USBDM    | AIO  | USB data D-                                                                                                                                                                 |
| 20    | REGV     | AO   | 3.3V reference output for internal 5 → 3.3V regulator                                                                                                                       |
| 21    | DVDD1    | P    | 5V power supply to internal regulator                                                                                                                                       |
| 22    | AVSS3    | P    | Analog ground                                                                                                                                                               |
| 23    | MICL     | AI   | Microphone input left channel                                                                                                                                               |
| 24    | MICR     | AI   | Microphone input right channel                                                                                                                                              |
| 25    | LINL     | AI   | Line-In input left channel                                                                                                                                                  |
|       |          |      |                                                                                                                                                                             |

| Pin # | Symbol | Type | Description |
|-------|--------|------|-------------|
|-------|--------|------|-------------|

|    |        |    |                                                                                         |
|----|--------|----|-----------------------------------------------------------------------------------------|
| 26 | XLINER | AI | Line in right channel                                                                   |
| 27 | AVDD1  | P  | 5V analog power for analog circuit                                                      |
| 28 | VREF   | AO | Connecting to external decoupling capacitor for embedded band-gap circuit; 2.25V output |
| 29 | VBIAS  | AO | Microphone bias voltage supply (4.5V/2.25V)                                             |
| 30 | AVSS1  | P  | Analog ground                                                                           |
| 31 | N.C    |    |                                                                                         |
| 32 | N.C    |    |                                                                                         |
| 33 | N.C    |    |                                                                                         |
| 34 | N.C    |    |                                                                                         |
| 35 | FROL   | AO | Line out front left channel                                                             |
| 36 | FROR   | AO | Line out front right channel                                                            |
| 37 | AVDD2  | P  | 5V analog power for analog circuit                                                      |
| 38 | SSOL   | AO | Line out side surround left channel (For Vista definition @ 5.1CH )                     |
| 39 | SSOR   | AO | Line out side surround right channel (For Vista definition @ 5.1CH CH)                  |
| 40 | CENO   | AO | Line out center channel                                                                 |
| 41 | LFEO   | AO | Line out LFE (subwoofer) channel                                                        |
| 42 | AVSS2  | P  | Analog ground                                                                           |
| 43 | VOLUP  | DI | Volume up (edge trigger with de-bouncing)                                               |
| 44 | VOLDN  | DI | Volume down (edge trigger with de-bouncing)                                             |
| 45 | SPDIFI | DI | S/PDIF input                                                                            |
| 46 | MUTER  | DI | Mute recording (edge trigger with de-bouncing)                                          |
| 47 | MUTEPL | DI | Mute playback (edge trigger with de-bouncing)                                           |
| 48 | SPDIFO | DO | S/PDIF output                                                                           |

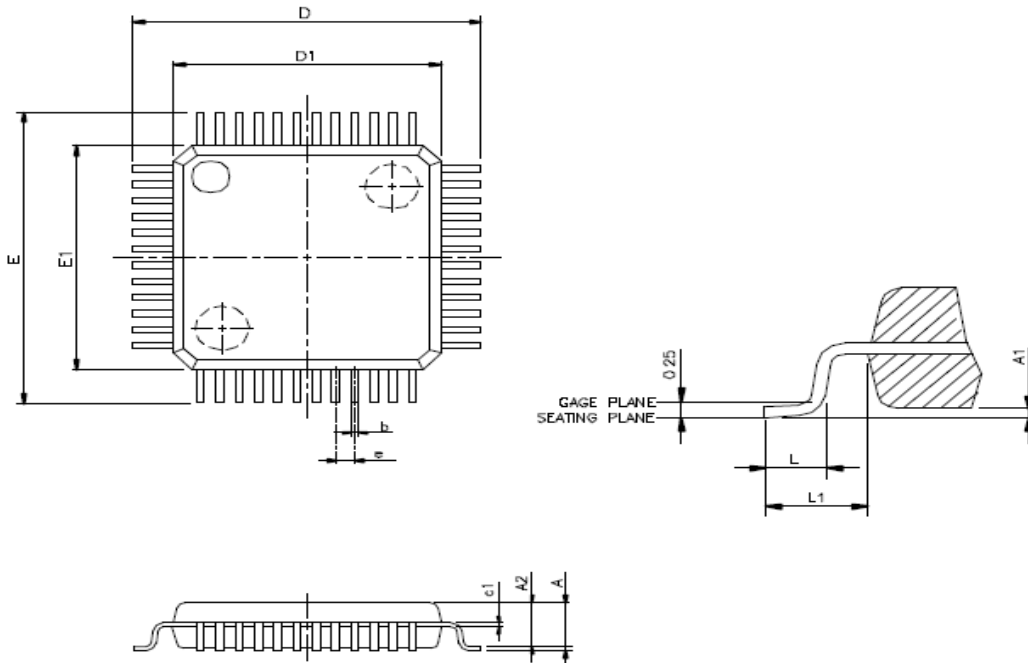
\*Note 1: DI - digital input pad  
 DO - digital output pad  
 DIO - digital bi-directional pad  
 AI/AO/AIO - analog pad  
 P - power pad

\*Note 2: For LQFP 48 package, PWRSEL, PWRSEL1, MSEL1 and MSEL2 are internal bonding options; all of those 4 pins are not bounded in default state.



### 4 Ordering Information

#### 4.1 CM6206LX (LQFP48)



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

| SYMBOLS | MIN.     | MAX. |
|---------|----------|------|
| A       | --       | 1.6  |
| A1      | 0.05     | 0.15 |
| A2      | 1.35     | 1.45 |
| c1      | 0.09     | 0.16 |
| D       | 9.00 BSC |      |
| D1      | 7.00 BSC |      |
| E       | 9.00 BSC |      |
| E1      | 7.00 BSC |      |
| e       | 0.5 BSC  |      |
| b       | 0.17     | 0.27 |
| L       | 0.45     | 0.75 |
| L1      | 1 REF    |      |

NOTES:

1. JEDEC OUTLINE: MS-026 BBC
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm.

### 5 Block Diagram

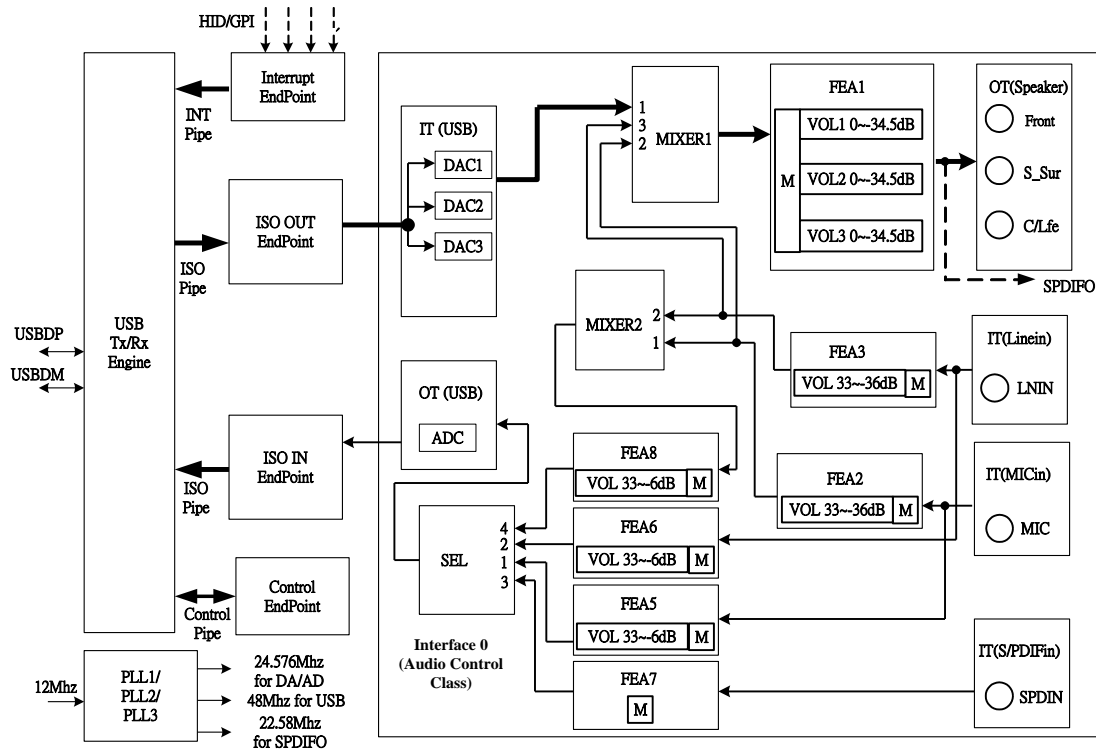


Figure 2 : Function Block Diagram of CM6206LX

## 6 Function Descriptions Block Diagram of CM6206LX

### 6.1 Internal Register

The internal registers of CM6206LX can be divided to two parts. Some of them (REG0, REG1, REG2, REG3, REG4 and REG5) are 16-bit width and can be accessed via HID interface SET\_RPT request. The others (REG8- REG14) are 8-bit width and can be accessed by vendor requests.

To access registers via HID interface, users should issue a “Set Output Report” HID request. The four bytes of output report data is organized as below:

|          |                                       |
|----------|---------------------------------------|
| Byte [0] | Bit5 = 1 => Access internal register  |
|          | Bit4 = 1 => read    Bit4 = 0 => write |
| Byte [1] | DATAL                                 |
| Byte [2] | DATAH                                 |
| Byte [3] | Register address (0, 1, 2, 3, 4, 5)   |



|         |           |          |            |         |           |            |           |
|---------|-----------|----------|------------|---------|-----------|------------|-----------|
| 15      | 14        | 13       | 12         | 11      | 10        | 9          | 8         |
| Rsvd    | SEL_CLK   | PLLBINen | SOFTMUTEen | GPIO4_o | GPIO4_OEN | GPIO3_o    | GPIO3_OEN |
| 7       | 6         | 5        | 4          | 3       | 2         | 1          | 0         |
| GPIO2_o | GPIO2_OEN | GPIO1_o  | GPIO1_OEN  | Valid   | SPDIFLOOP | DIS_SPDIFO | SPDIFMIX  |

| Bit Number | Bit Mnemonic | Read/Write | Function                                                               |
|------------|--------------|------------|------------------------------------------------------------------------|
| 15         | Rsvd         | R/W        | Reserved                                                               |
| 14         | SEL_CLK      | R/W        | For test. Select 44.1k source for DACs 1=from 22.58M<br>0=from 24.576M |
| 13         | PLLBINen     | R/W        | PLL binary search enable                                               |
| 12         | SOFTMUTEen   | R/W        | Soft mute enable                                                       |
| 11         | GPIO4_o      | R/W        | Gpio4 signal                                                           |
| 10         | GPIO4_OEN    | R/W        | Gpio4 output enable                                                    |
| 9          | GPIO3_o      | R/W        | Gpio3 signal                                                           |
| 8          | GPIO3_OEN    | R/W        | Gpio3 output enable                                                    |
| 7          | GPIO2_o      | R/W        | Gpio2 signal                                                           |
| 6          | GPIO2_OEN    | R/W        | Gpio2 output enable                                                    |
| 5          | GPIO1_o      | R/W        | Gpio1 signal                                                           |
| 4          | GPIO1_OEN    | R/W        | Gpio1 output enable                                                    |
| 3          | VALID        | R/W        | SPDIFOUT Valid Signal 1=un-valid                                       |
| 2          | SPDIFLOOP    | R/W        | SPDIF loop-back enable                                                 |
| 1          | DIS_SPDIFO   | R/W        | SPDIF out disable                                                      |
| 0          | SPDIFMIX     | R/W        | SPDIF in mix enable                                                    |

REG2

Address: 0x02  
Reset State: 0x6004

|          |    |    |    |    |        |           |   |
|----------|----|----|----|----|--------|-----------|---|
| 15       | 14 | 13 | 12 | 11 | 10     | 9         | 8 |
| PLAYMUTE |    |    |    |    |        |           |   |
| 7        | 6  | 5  | 4  | 3  | 2      | 1         | 0 |
| PLAYMUTE |    |    |    |    | EN_BTL | MCUCLKSEL |   |

| Bit Number | Bit Mnemonic | Read/Write | Function                                                                                                                                                                                                                                                                                                                            |
|------------|--------------|------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15         |              |            |                                                                                                                                                                                                                                                                                                                                     |
| 14-13      |              |            |                                                                                                                                                                                                                                                                                                                                     |
| 12-3       | PLAYMUTE     | R/W        | Channel mute control (high active)<br>PLAYMUTE[0]: mute Left Front<br>PLAYMUTE[1]: mute Right Front<br>PLAYMUTE[2]: mute Center<br>PLAYMUTE[3]: mute Subwoofer<br>PLAYMUTE[4]: mute Side Surround Left<br>PLAYMUTE[5]: mute Side Surround Right<br>PLAYMUTE[6]:<br>PLAYMUTE[7]:<br><b>PLAYMUTE[8]: 0:</b><br><b>PLAYMUTE[9]: 0:</b> |
| 2          | EN_BTL       | R/W        | <b>1 = BTL mode enable. This bit only useful for 2ch mode.</b>                                                                                                                                                                                                                                                                      |
| 1-0        | MCUCLKSEL    | R/W        | MCU clock frequency<br>00: 1.5Mhz<br>01: 3Mhz<br>10: 6Mhz<br>11: 12Mhz                                                                                                                                                                                                                                                              |

REG3

Address: 0x03

Reset State: 0x143f / 0x147f

|    |    |    |          |    |          |       |                   |
|----|----|----|----------|----|----------|-------|-------------------|
| 15 | 14 | 13 | 12       | 11 | 10       | 9     | 8                 |
|    |    |    | FLYSPEED |    | VRAP25EN | MSEL1 | SPDIF_F<br>REQ[1] |

|                   |        |     |     |      |      |      |        |
|-------------------|--------|-----|-----|------|------|------|--------|
| 7                 | 6      | 5   | 4   | 3    | 2    | 1    | 0      |
| SPDIF_F<br>REQ[0] | PINSEL | FOE | ROE | CBOE | LOSE | HPOE | CANREC |

| Bit Number | Bit Mnemonic | Read/Write | Function                                                                                    |
|------------|--------------|------------|---------------------------------------------------------------------------------------------|
| 15-14      | Rsvd         | R          | Reserved                                                                                    |
| 13-11      | FLYSPEED     | R/W        | Sensitivity to FLY tuner volume control VP/VD signal                                        |
| 10         | VRAP25EN     | R/W        | Microphone bias voltage supply select<br>0: 4.5V<br>1: 2.25V                                |
| 9          | MSEL1        | R          | 0: MICINL/R and LIL/R mix to LOFL and LOFR<br>1: MICINL/R and LIL/R mix to 8 channels       |
| 8-7        | SPDIF_FREQ   | R          | SPDIF in sample rate<br>00: 44.1K<br>01: reserved<br>10: 48K<br>11: 32K                     |
| 6          | PINSEL       | R          | 0: 100 pin package<br>1: 48 pin package                                                     |
| 5          | FOE          | R/W        | 1: LOFL/LOFR enable<br>0: LOFL/LOFR disable (Hi Z)                                          |
| 4          | ROE          | R/W        | 1: LOLS/LORS enable<br>0: LOLS/LORS disable (Hi Z)                                          |
| 3          | CBOE         | R/W        | 1: LOCF/LOLFE enable<br>0: LOCF/LOLFE disable (Hi Z)                                        |
| 2          |              |            |                                                                                             |
| 1          |              |            |                                                                                             |
| 0          | CANREC       | R          | SPDIF in recording status<br>0: SPDIF in can not be recorded<br>1: SPDIF in can be recorded |

REG4

Address: 0x04

Reset State: 0x0000

|          |                |          |                |          |                |         |               |
|----------|----------------|----------|----------------|----------|----------------|---------|---------------|
| 15       | 14             | 13       | 12             | 11       | 10             | 9       | 8             |
| GPIO12_o | GPIO12_<br>OEN | GPIO11_o | GPIO11_<br>OEN | GPIO10_o | GPIO10_<br>OEN | GPIO9_o | GPIO9_<br>OEN |

|         |               |         |               |         |               |         |               |
|---------|---------------|---------|---------------|---------|---------------|---------|---------------|
| 7       | 6             | 5       | 4             | 3       | 2             | 1       | 0             |
| GPIO8_o | GPIO8_<br>OEN | GPIO7_o | GPIO7_<br>OEN | GPIO6_o | GPIO6_<br>OEN | GPIO5_o | GPIO5_<br>OEN |

| Bit Number | Bit Mnemonic | Read/Write | Function             |
|------------|--------------|------------|----------------------|
| 15         | GPIO12_o     | R/W        | Gpio12 signal        |
| 14         | GPIO12_OEN   | R/W        | Gpio12 output enable |
| 13         | GPIO11_o     | R/W        | Gpio11 signal        |
| 12         | GPIO11_OEN   | R/W        | Gpio11 output enable |
| 11         | GPIO10_o     | R/W        | Gpio10 signal        |
| 10         | GPIO10_OEN   | R/W        | Gpio10 output enable |
| 9          | GPIO9_o      | R/W        | Gpio9 signal         |
| 8          | GPIO9_OEN    | R/W        | Gpio9 output enable  |
| 7          | GPIO8_o      | R/W        | Gpio8 signal         |
| 6          | GPIO8_OEN    | R/W        | Gpio8 output enable  |
| 5          | GPIO7_o      | R/W        | Gpio7 signal         |
| 4          | GPIO7_OEN    | R/W        | Gpio7 output enable  |
| 3          | GPIO6_o      | R/W        | Gpio6 signal         |
| 2          | GPIO6_OEN    | R/W        | Gpio6 output enable  |
| 1          | GPIO5_o      | R/W        | Gpio5 signal         |
| 0          | GPIO5_OEN    | R/W        | Gpio5 output enable  |

REG5

Address: 0x05

Reset State: 0x3000

|      |    |        |        |        |          |   |       |
|------|----|--------|--------|--------|----------|---|-------|
| 15   | 14 | 13     | 12     | 11     | 10       | 9 | 8     |
| Rsvd |    | DA_RST | AD_RST | AD2SPD | SPDO_SEL |   | CODEM |
|      |    | N      | N      | 0      |          |   |       |

|        |        |        |        |        |            |   |   |
|--------|--------|--------|--------|--------|------------|---|---|
| 7      | 6      | 5      | 4      | 3      | 2          | 1 | 0 |
| EN_HPF | T_SEL_ | T_SEL_ | T_SEL_ | T_SEL_ | T_SEL_DSAD |   |   |
|        | DSDA4  | DSDA3  | DSDA2  | DSDA1  |            |   |   |

| Bit Number | Bit Mnemonic | Read/Write | Function                                                                                                                                |
|------------|--------------|------------|-----------------------------------------------------------------------------------------------------------------------------------------|
| 15-14      | Rsvd         | R          | Reserved                                                                                                                                |
| 13         | DA_RSTN      | R/W        | DAC delta-sigma reset signal                                                                                                            |
| 12         | AD_RSTN      | R/W        | ADC delta-sigma reset signal                                                                                                            |
| 11         | AD2SPDO      | R/W        | 1: enable ADC data to SPDIFOUT                                                                                                          |
| 10-9       | SPDO_SEL     | R/W        | SPDIFOUT channel selector<br>00: Front; 01: Side_Sur; 10: CEN/LFE; 11: Rear_Sur                                                         |
| 8          | CODECM       | R/W        | 0: USB mode; 1: CODEC mode                                                                                                              |
| 7          | EN_HPF       | R/W        | 1: Enable DAC high pass filter                                                                                                          |
| 6          | T_SEL_DSDA4  | R/W        | 1: Loopback ADC 1-bit delta-sigma data to RearSurround DAC                                                                              |
| 5          | T_SEL_DSDA3  | R/W        | 1: Loopback ADC 1-bit delta-sigma data to CEN/LFE DAC                                                                                   |
| 4          | T_SEL_DSDA2  | R/W        | 1: Loopback ADC 1-bit delta-sigma data to SideSurround DAC                                                                              |
| 3          | T_SEL_DSDA1  | R/W        | 1: Loopback ADC 1-bit delta-sigma data to Front DAC                                                                                     |
| 2-0        | T_SEL_DSAD   | R/W        | Select delta-sigma 1-bit input source to AD digital filter.<br>000: normal; 100: Front; 101: SSurround; 110: Cen/LFE;<br>111: RSurround |





REG9

Address:

0x09

Reset State:

|       |       |       |        |       |       |       |       |
|-------|-------|-------|--------|-------|-------|-------|-------|
| 7     | 6     | 5     | 4      | 3     | 2     | 1     | 0     |
| MSEL1 | SEL 3 | SEL 2 | PINSEL | MSEL2 | HIDEN | SEL 1 | SEL 0 |

| Bit Number | Bit Mnemonic | Read/Write | Function                                   |
|------------|--------------|------------|--------------------------------------------|
| 7          | MSEL1        | R          | MSEL1 bonding option value                 |
| 6          | SEL3         | R          | SEL3 bonding option value                  |
| 5          | SEL2         | R          | SEL2 bonding option value                  |
| 4          | PINSEL       | R          | PINSEL bonding option value                |
| 3          | MSEL2        | --         |                                            |
| 2          | HIDEN        | R          | 0: No HID Function<br>1: With HID Function |
| 1          | SEL1         | R          | SEL1 bonding option value                  |
| 0          | SEL0         | R          | SEL0 bonding option value                  |

REG10

Address:

0x0a

Reset State:

0x05

|         |   |   |   |   |   |   |   |
|---------|---|---|---|---|---|---|---|
| 7       | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CHIP-ID |   |   |   |   |   |   |   |

| Bit Number | Bit Mnemonic | Read/Write | Function            |
|------------|--------------|------------|---------------------|
| 7-0        | CHIP-ID      | R          | Low byte of CHIP ID |

REG11 Address: 0x0b  
Reset State: 0x50

|         |   |   |   |   |   |   |   |
|---------|---|---|---|---|---|---|---|
| 7       | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CHIP-ID |   |   |   |   |   |   |   |

| Bit Number | Bit Mnemonic | Read/Write | Function             |
|------------|--------------|------------|----------------------|
| 7-0        | CHIP-ID      | R          | High byte of CHIP ID |

REG12 Address: 0x0c  
Reset State: 0x00

|       |   |   |   |   |   |   |   |
|-------|---|---|---|---|---|---|---|
| 7     | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| FDBK1 |   |   |   |   |   |   |   |

| Bit Number | Bit Mnemonic | Read/Write | Function                                        |
|------------|--------------|------------|-------------------------------------------------|
| 7-0        | FDBK1        | R/W        | Lowest byte of Feedback information for ISO OUT |

REG13 Address: 0x0d  
Reset State: 0x00

|       |   |   |   |   |   |   |   |
|-------|---|---|---|---|---|---|---|
| 7     | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| FDBK2 |   |   |   |   |   |   |   |

| Bit Number | Bit Mnemonic | Read/Write | Function                                        |
|------------|--------------|------------|-------------------------------------------------|
| 7-0        | FDBK2        | R/W        | Middle byte of Feedback information for ISO OUT |

REG14 Address: 0x0e  
Reset State: 0x00

|       |   |   |   |   |   |   |   |
|-------|---|---|---|---|---|---|---|
| 7     | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| FDBK3 |   |   |   |   |   |   |   |

| Bit Number | Bit Mnemonic | Read/Write | Function                                         |
|------------|--------------|------------|--------------------------------------------------|
| 7-0        | FDBK3        | R/W        | Highest byte of Feedback information for ISO OUT |

### 6.2 Serial EEPROM Content

CM6206LX supports four-wire serial EEPROM interface. When an external serial EEPROM is detected,

Vendor ID and Product ID reported within Device Descriptor will be derived from the content of serial EEPROM. The organization of serial EEPROM is shown below:

|              |                     |
|--------------|---------------------|
| Address = 0  | 16'h434dX           |
| Address = 1  | Vendor ID           |
| Address = 2  | Product ID          |
| Address = 3  | String 1,String 0   |
| Address = 4  | String 3,String 2   |
| Address = 5  | String 5,String 4   |
| Address = 6  | String 7,String 6   |
| Address = 7  | String 9,String 8   |
| Address = 8  | String 11,String 10 |
| Address = 9  | String 13,String 12 |
| Address = 10 | String 15,String 14 |
| Address = 11 | String 17,String 16 |
| Address = 12 | String 19,String 18 |
| Address = 13 | String 21,String 20 |
| Address = 14 | String 23,String 22 |
| Address = 15 |                     |
| Address = 16 |                     |
| Address = 17 |                     |
| Address = 18 |                     |
| Address = 19 |                     |
| Address = 20 | {8'dx,MString 0}    |
| Address = 21 | {8'dx,MString 1}    |
| Address = 22 | {8'dx,MString 2}    |
| Address = 23 | {8'dx,MString 3}    |
| Address = 24 | {8'dx,MString 4}    |
| Address = 25 | {8'dx,MString 5}    |
| Address = 26 | {8'dx,MString 6}    |
| Address = 27 | {8'dx,MString 7}    |
| Address = 28 | {8'dx,MString 8}    |
| Address = 29 | {8'dx,MString 9}    |
| Address = 30 | {8'dx,MString 10}   |
| Address = 31 | {8'dx,MString 11}   |
| Address = 63 | 16'hXXXX            |

Users can program serial EEPROM via HID interface, as described in the former section. The first word is a magic code. Only when it matches, CM6206LX will regard the serial EEPROM valid.

### 6.3 Power Management

To meet suspend current specification of USB; CM6206LX turns off most blocks when entering suspend. The only two exceptions are power-on-reset and regulator.

To meet un-configured current specification of USB, CM6206LX provides a control signal PDSW to turn off external components. PDSW would be active when USB host does not configure CM6206LX. PDSW would also be active when CM6206LX is suspended. If serial EEPROM is exist, notice that it should not be powered off anyway because it contains Vendor ID and Product ID which should be returned to USB host before CM6206LX is configured.

## 7 Volume Control

### 7.1 DAC Volume Control

| VOL_*_<br><5:0> | Scale<br>(linear) | VOL_*_<br><5:0> | Scale<br>(linear) | VOL_*_<br><5:0> | Scale<br>(linear) | VOL_*_<br><5:0> | Scale<br>(linear) |
|-----------------|-------------------|-----------------|-------------------|-----------------|-------------------|-----------------|-------------------|
| 00              | 1.000             | 10              | 0.724             | 20              | 0.448             | 30              | 0.171             |
| 01              | 0.973             | 11              | 0.696             | 21              | 0.420             | 31              | 0.144             |
| 02              | 0.944             | 12              | 0.669             | 22              | 0.392             | 32              | 0.116             |
| 03              | 0.917             | 13              | 0.641             | 23              | 0.365             | 33              | 0.088             |
| 04              | 0.890             | 14              | 0.613             | 24              | 0.337             | 34              | 0.061             |
| 05              | 0.862             | 15              | 0.586             | 25              | 0.309             | 35              | 0.033             |
| 06              | 0.834             | 16              | 0.558             | 26              | 0.282             | 36              | 0.006             |
| 07              | 0.807             | 17              | 0.530             | 27              | 0.254             | 37              | mute              |
| 08              | 0.779             | 18              | 0.503             | 28              | 0.227             |                 |                   |
| 09              | 0.751             | 19              | 0.475             | 29              | 0.199             |                 |                   |

Note: VOL\_\*\_ stands for VOL\_FL\_, VOL\_FR\_, VOL\_CF\_, VOL\_LFE\_, VOL\_LS\_, VOL\_RS\_, VOL\_SL\_, VOL\_SR\_. The volume control is in

linear scale.

### 7.2 ADC Volume Control

Note: VOL\_\*\_ stands for VOL\_REC\_L\_ and VOL\_REC\_R\_. The volume control is in log scale.

| USB Request Data<br>(Hex) | VOL_*_<br><4:0> | Scale (log) | USB Request Data<br>(Hex) | VOL_*_<br><4:0> | Scale (log) |
|---------------------------|-----------------|-------------|---------------------------|-----------------|-------------|
| 0B7F-0B00                 | 11111           | +33dB       | 047F-0400                 | 10001           | +12dB       |
| 0AFF-0A80                 | 11110           | +31.5dB     | 03FF-0380                 | 10000           | +10.5dB     |
| 0A7F-0A00                 | 11101           | +30dB       | 037F-0300                 | 01111           | +9dB        |
| 09FF-0980                 | 11100           | +28.5dB     | 02FF-0280                 | 01110           | +7.5dB      |
| 097F-0900                 | 11011           | +27dB       | 027F-0200                 | 01101           | +6dB        |
| 08FF-0880                 | 11010           | +25.5dB     | 01FF-0180                 | 01100           | +4.5dB      |
| 087F-0800                 | 11001           | +24dB       | 017F-0100                 | 01011           | +3dB        |
| 07FF-0780                 | 11000           | +22.5dB     | 00FF-0080                 | 01010           | +1.5dB      |
| 077F-0700                 | 10111           | +21dB       | 007F-0000                 | 01001           | 0dB         |
| 06FF-0680                 | 10110           | +19.5dB     | FFFF-FC00                 | 01000           | -1.5dB      |

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|           |       |         |                  |       |        |
|-----------|-------|---------|------------------|-------|--------|
| 067F-0600 | 10101 | +18dB   | FBFF-F800        | 00111 | -3dB   |
| 05FF-0580 | 10100 | +16.5dB | F7FF-F400        | 00110 | -4.5dB |
| 057F-0500 | 10011 | +15dB   | F3FF-F000 / 8000 | 00101 | -6dB   |
| 04FF-0480 | 10010 | +13.5dB | FFFF-EC00        | 00100 | -6dB   |

Note: VOL\*\_ stands for VOL\_REC\_L\_ and VOL\_REC\_R\_. The volume control is in log scale.

### 7.3 MIC / Line-in Monitor Volume Control

| VOL*_*<4:0> | Scale (log) | VOL*_*<4:0> | Scale (log) | VOL*_*<4:0> | Scale (log) | VOL*_*<4:0> | Scale (log) |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| 00          | +12.0dB     | 08          | 0.0dB       | 16          | -12.0dB     | 24          | -24.0dB     |
| 01          | +10.5dB     | 09          | -1.5dB      | 17          | -13.5dB     | 25          | -25.5dB     |
| 02          | +9.0dB      | 10          | -3.0dB      | 18          | -15.0dB     | 26          | -27.0dB     |
| 03          | +7.5dB      | 11          | -4.5dB      | 19          | -16.5dB     | 27          | -28.5dB     |
| 04          | +6.0dB      | 12          | -6.0dB      | 20          | -18.0dB     | 28          | -30.0dB     |
| 05          | +4.5dB      | 13          | -7.5dB      | 21          | -19.5dB     | 29          | -31.5dB     |
| 06          | +3.0dB      | 14          | -9.0dB      | 22          | -21.0dB     | 30          | -33.0dB     |
| 07          | +1.5dB      | 15          | -10.5dB     | 23          | -22.5dB     | 31          | mute        |

Note: VOL\*\_\* stands for VOL\_MICM\_L\_, VOL\_MICM\_R\_, VOL\_LINEM\_L\_, VOL\_LINEM\_R\_. The volume control is in log scale.

## 8 Electrical Characteristics

### 8.1 Maximum Ratings

| Parameter                   | Symbol | Min. | Max. | Unit |
|-----------------------------|--------|------|------|------|
| Digital power voltage       | DVDD   | 4.75 | 5.25 | V    |
| Analog power voltage        | AVDD   | 4.75 | 5.25 | V    |
| Digital Input Voltage       | VIND   | -0.5 | 3.6  | V    |
| Analog Input Voltage        | VINA   | -0.5 | 5.5  | V    |
| Operating temperature range | TO     | 0    | 70   | °C   |
| Storage temperature range   | TST    | -40  | 125  | °C   |
| Power dissipation           | PDMAX  |      | 900  | mW   |

### 8.2 Recommended Operating Conditions

| Parameter                     | Symbol | Min. | Typ. | Max. | Unit |
|-------------------------------|--------|------|------|------|------|
| Digital Operating Voltage     | DVDD   | 4.75 | 5    | 5.25 | V    |
| Analog Operating voltage      | AVDD   | 4.75 | 5    | 5.25 | V    |
| Operating Ambient Temperature | TO     | 0    | 25   | 70   | °C   |

### 8.3 Power Consumption

| Parameter                     | Min. | Typ. | Max. | Unit |
|-------------------------------|------|------|------|------|
| Power Supply Current (Normal) |      |      |      |      |
| AVDD (5.0V)                   | -    | 85   | -    | mA   |
| DVDD (5.0V)                   | -    | 35   | -    | mA   |

### 8.4 DC Characteristics (Digital)

| PARAMETER             | Symbol | Condition              | Min. | Typ. | Max.    | Unit |
|-----------------------|--------|------------------------|------|------|---------|------|
| Input high voltage    | VIH    |                        | 2.0  | -    | VDD+0.3 | V    |
| Input low voltage     | VIL    |                        | -0.5 | -    | 0.8     | V    |
| Output high voltage   | VOH    | I <sub>OH</sub> = 4mA  | 2.4  | -    | VDD     | V    |
| Output low voltage    | VOL    | I <sub>OL</sub> = -4mA | 0.0  | 0.2  | 0.4     | V    |
| Input Leakage Current | IIL    | 0<Vin<VDD              | -70  | -    | 70      | μA   |
| Input Pin Capacitance | Cin    |                        | -    | -    | 10      | pF   |
| Pin Inductance        | Lpin   |                        | -    | -    | 20      | nH   |

### 8.5 AC Characteristics (Digital)

| Parameter | Symbol | Condition | Min. | Max. | Units |
|-----------|--------|-----------|------|------|-------|
|-----------|--------|-----------|------|------|-------|



|                              |       |                    |   |   |      |
|------------------------------|-------|--------------------|---|---|------|
| <b>Output Rise Slew Rate</b> | SLEWr | 0.2Vdd-0.6Vdd load | 1 | 4 | V/ns |
| <b>Output Fall Slew Rate</b> | SLEWf | 0.6Vdd-0.2Vdd load | 1 | 4 | V/ns |

### 8.6 Analog Performance

The measurements are performed under the circumstance as:

Tambient = 25°C, AVdd = 5.0V ± 5%, DVdd = 3.3V ± 5%, 10kΩ/50pF external load. Input is 1 kHz sine wave; Sampling frequency = 48 kHz; Bandwidth = 20 to 20 kHz; 0dB attenuation; All sound effects such as 3D effects are disabled.

| Parameter                     | Minimum | Typical | Maximum | Units |
|-------------------------------|---------|---------|---------|-------|
| Full Scale Input Voltage:     |         |         |         |       |
| Line Inputs (Mixer)           | -       | 1.1     | 1.25    | Vrms  |
| Line Inputs (A/D)             | -       | 1.1     | 1.25    | Vrms  |
| Mic Inputs (33dB Maximum)     | -       | 0.1     | 1.25    | Vrms  |
| Full Scale Output Voltage:    |         |         |         |       |
| Front_Out                     | -       | 1.1     | -       | Vrms  |
| Side_Surround_Out             | -       | 1.1     | -       | Vrms  |
| Center / LFE_out              | -       | 1.1     | -       | Vrms  |
| Back_Surround_Out             | -       | 1.1     | -       | Vrms  |
| SNR (Idle)                    |         |         |         | -     |
| D/A                           | 96      | 97      | -       | dBFS  |
| A/D                           | 80      | 85      | -       | dBFS  |
| Dynamic Range (-60dB)         |         |         |         |       |
| D/A                           | -       | 96      | -       | dBFS  |
| A/D                           | -       | 91      | -       | dBFS  |
| THD+N                         |         |         |         |       |
| D/A                           | -       | -88     | -       | dBFS  |
| A/D                           | -       | -88     | -       | dBFS  |
| Frequency Response            |         |         |         |       |
| D/A                           | 16      | -       | 19,200  | Hz    |
| A/D                           | 16      | -       | 19,200  | Hz    |
| Transition Band               | 19,200  |         | 28,800  | Hz    |
| Stop Band                     | 28,800  |         | ∞       | Hz    |
| Stop Band Rejection           | -       | -75     | -       | dB    |
| Out-Of-Band Rejection         | -       | -65     | -       | dB    |
| Power Supply Rejection Ratio  | -       | -40     | -       | dB    |
| Master Volume Gain (38 steps) |         |         |         |       |
| Step Size                     |         | Linear  |         |       |
| Control Range                 | -34.5   |         | 0       | dB    |
| Analog Input Gain (48 steps)  |         |         |         |       |
| Step Size                     |         | 1.5     |         | dB    |
| Control Range                 | -36     | -       | +22.5   | dB    |
| Recording Gain (26 steps)     |         |         |         |       |
| Step Size                     |         | 1.5     |         | dB    |
| Control Range                 | -6      | -       | +33     | dB    |
| Input Impedance               |         |         |         |       |
| Line-In, CD, MIC, PCSPK       | -       | 20      | -       | KΩ    |
| Vrefout                       | -       | 2.25    | -       | V     |

## 9 Audio Performance Curves

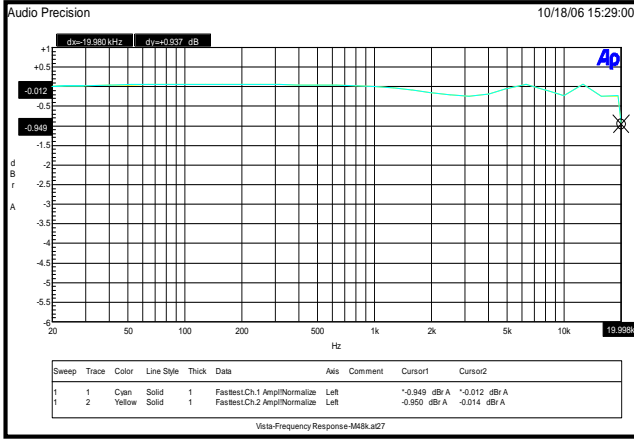
### 9.1 10K loading (Line Out / Surround / Center LFE) Frequency Response

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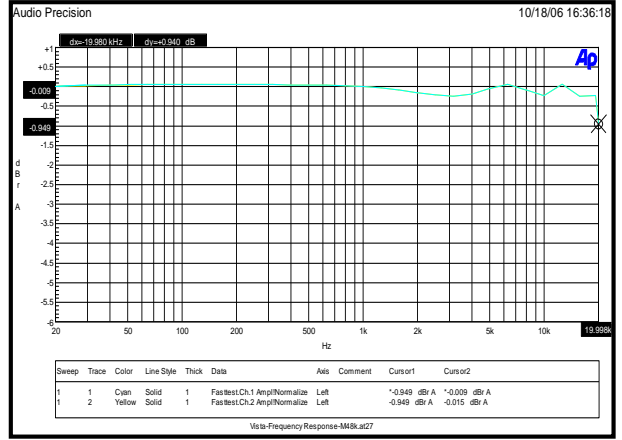
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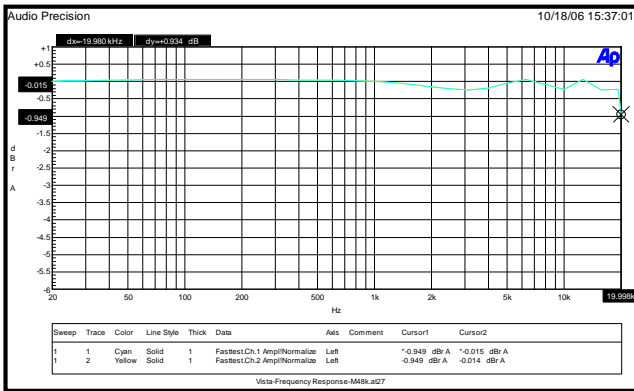
Front out



Center LFE out

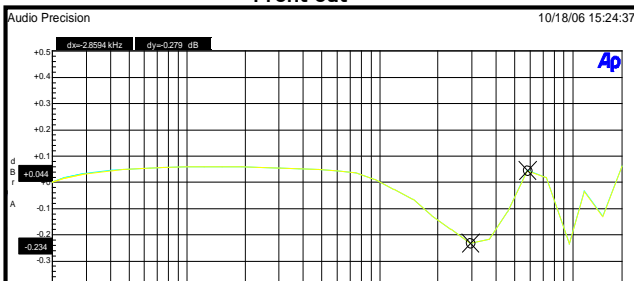


Surround out



## 9.2 10K loading (Line Out / Surround / Center LFE) Passband Ripple

Front out



Center LFE Out

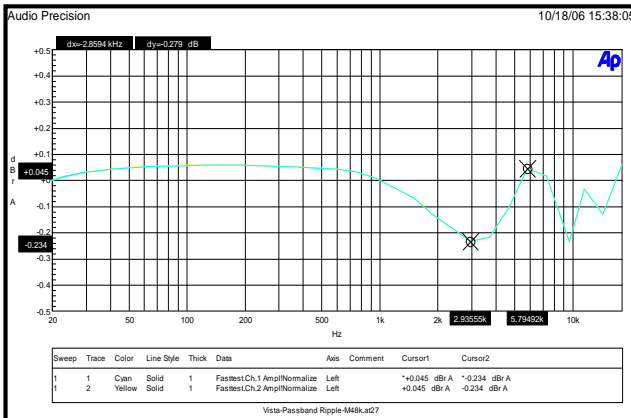


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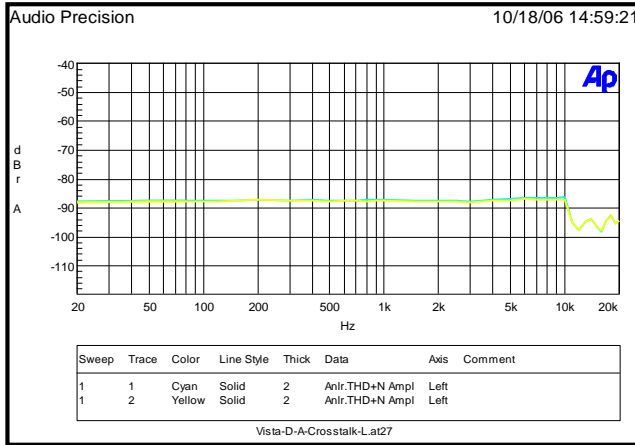


## Surround out

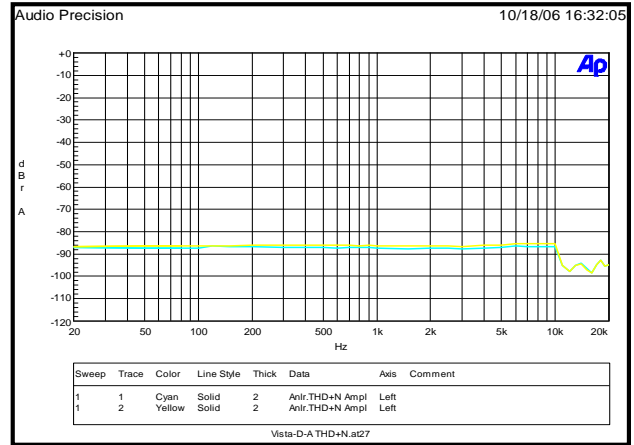


### 9.3 10K loading (Line Out / Surround / Center LFE /) THD+N Curve

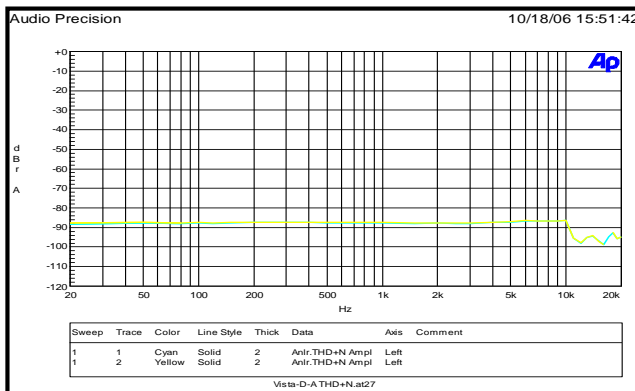
Front out



Center LFE Out

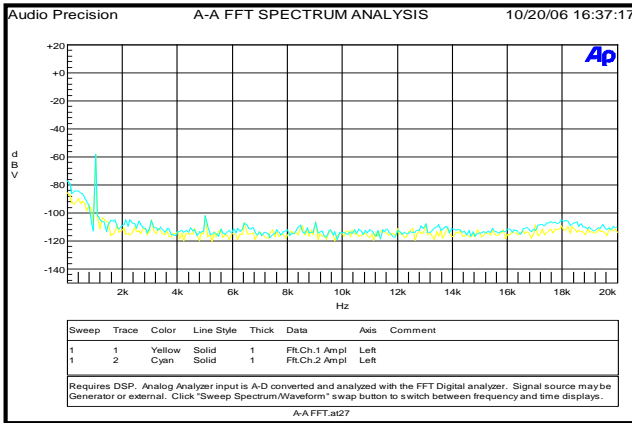


Surround out

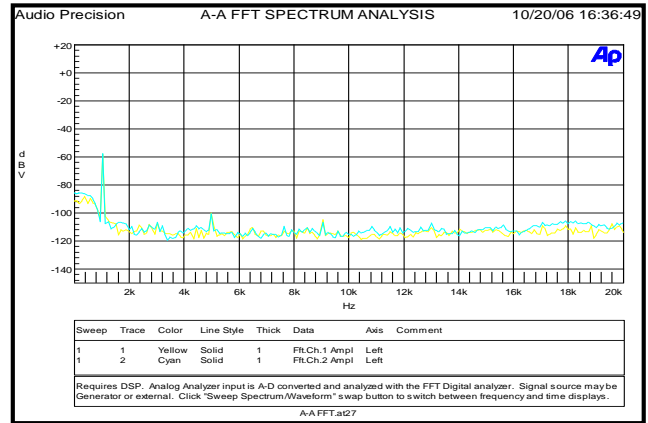


### 9.4 10K loading (Line Out / Surround / Center LFE /) Dynamic Range

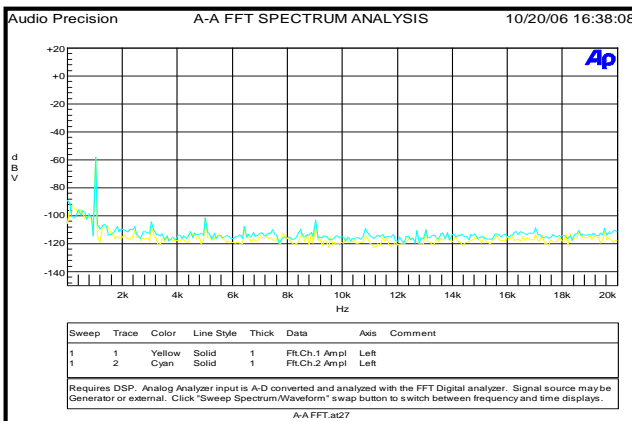
Front out



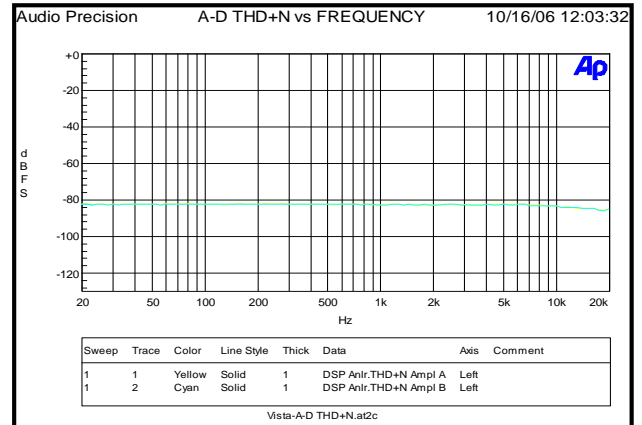
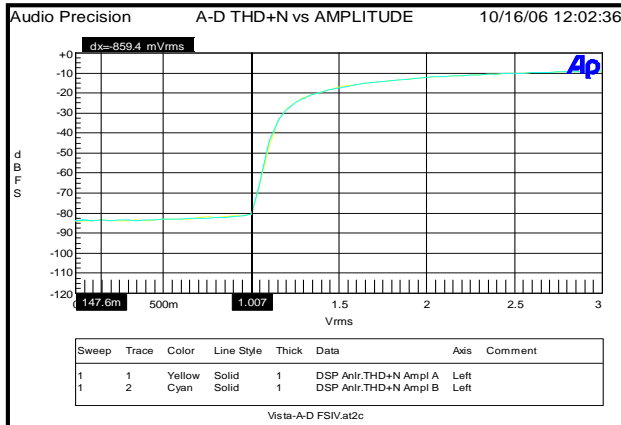
Center LFE Out



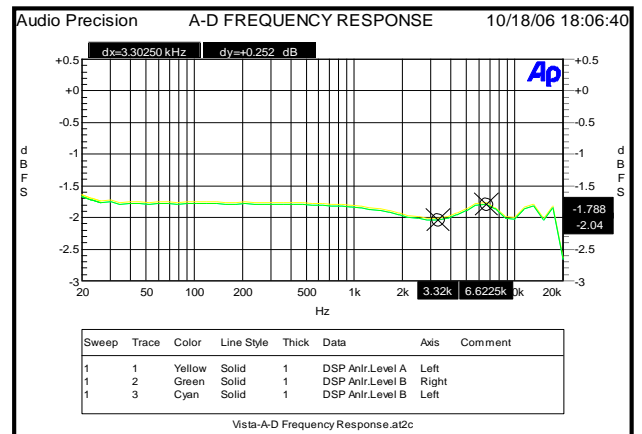
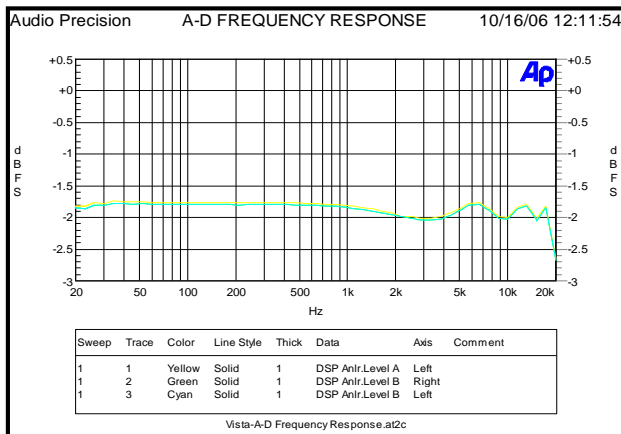
Surround out



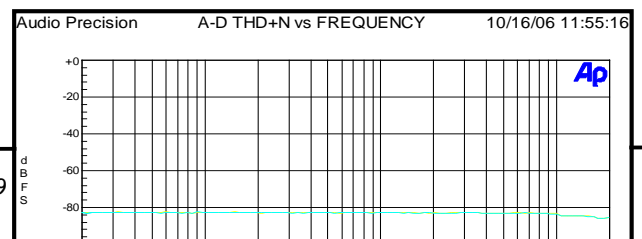
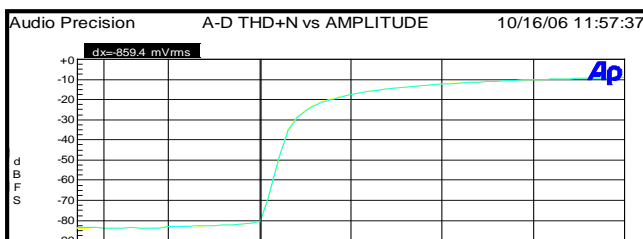
### 9.5 A-D Line in FSIV / THD+N Curve



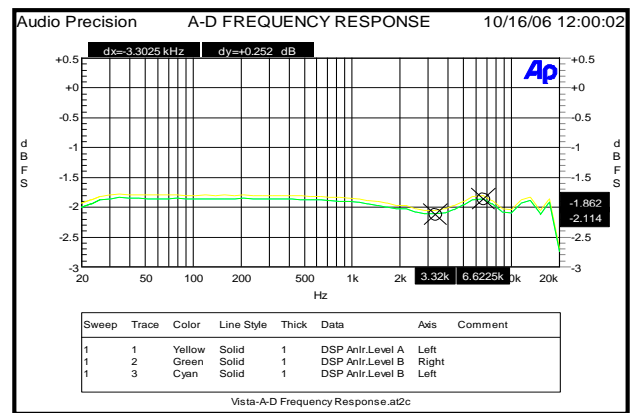
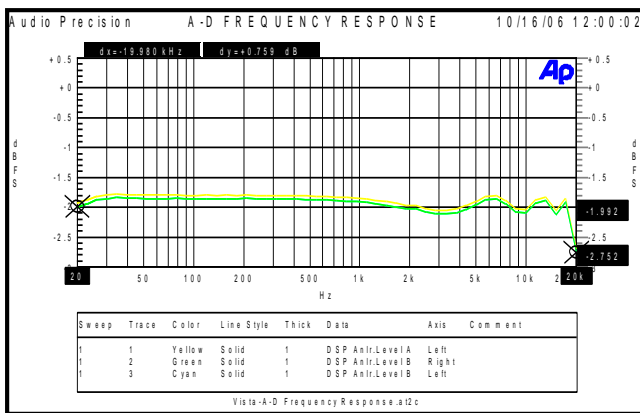
### 9.6 A-D Line in Frequency Response / Passband Ripple



### 9.7 A-D Mic in FSIV / THD+N Curve



### 9.8 A-D Mic in Frequency Response / Passband Ripple



### Reference

USB-IF, USB Specification, Revision 1.1 and 2.0, and USB Audio Device Class Specification, Revision 1.0.

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— End of Specifications —

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