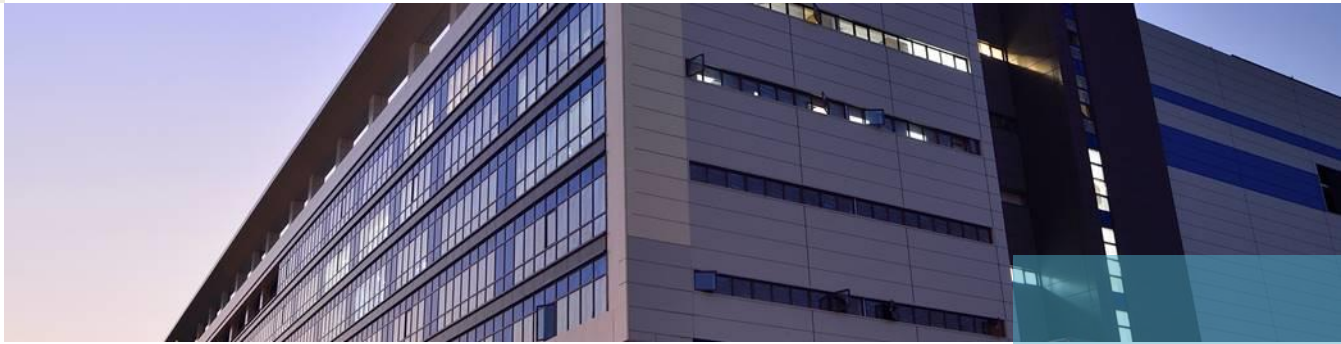
Nexchip

Confidential



Nexchip 110LP Process Introduction

2021.12

110LP Process Outline

- **1P5M CMOS Silicide Process**
  - ✓ Photo layers :
    - Standard (1P5M, with Hi-R, OTP)
    - Standard: 25 masks
    - Optional layer: 2 layers
- **High density SRAM**
  - ✓ Single port 1.32um^2 (6T SRAM)
- **device**
  - ✓ IO device: 5V
  - ✓ Core device: 1.5V

110LP Process Key Process Features

- Single poly, up to five metal layers
- Gate Oxide (25A/150A)
- Offer SRAM with bit cell area 1.32um^2
- Retrograde Twin-well for core device(1.5V) and IO devices 5V
- Aluminum metallization with tungsten plug
- OTP and MTP Cell

110LP Process Device

- **I/O device: 5V**
- **Core device: 1.5V**
- **SRAM :** Bit cell 1.32um^2 at 1.5V w/i compiler
- **OTP :** eMemory
- **MTP :** ACTT
- **MIM :** 1.0, 1.25, 1.5, 2.0 fF/um^2
- **High-R poly :** 2 K ohm without additional mask

110LP Process Key Design Rules

Process	110nm
AA(OD)	0.16/0.16
Poly	0.11/0.20
CT	0.12/0.16
M1	0.144/0.144
Via n	0.16/0.2
nM	0.18/0.20
TM_10K	0.39/0.40
SRAM	1.32um^2

110LP Process 5V/1.5V EDR

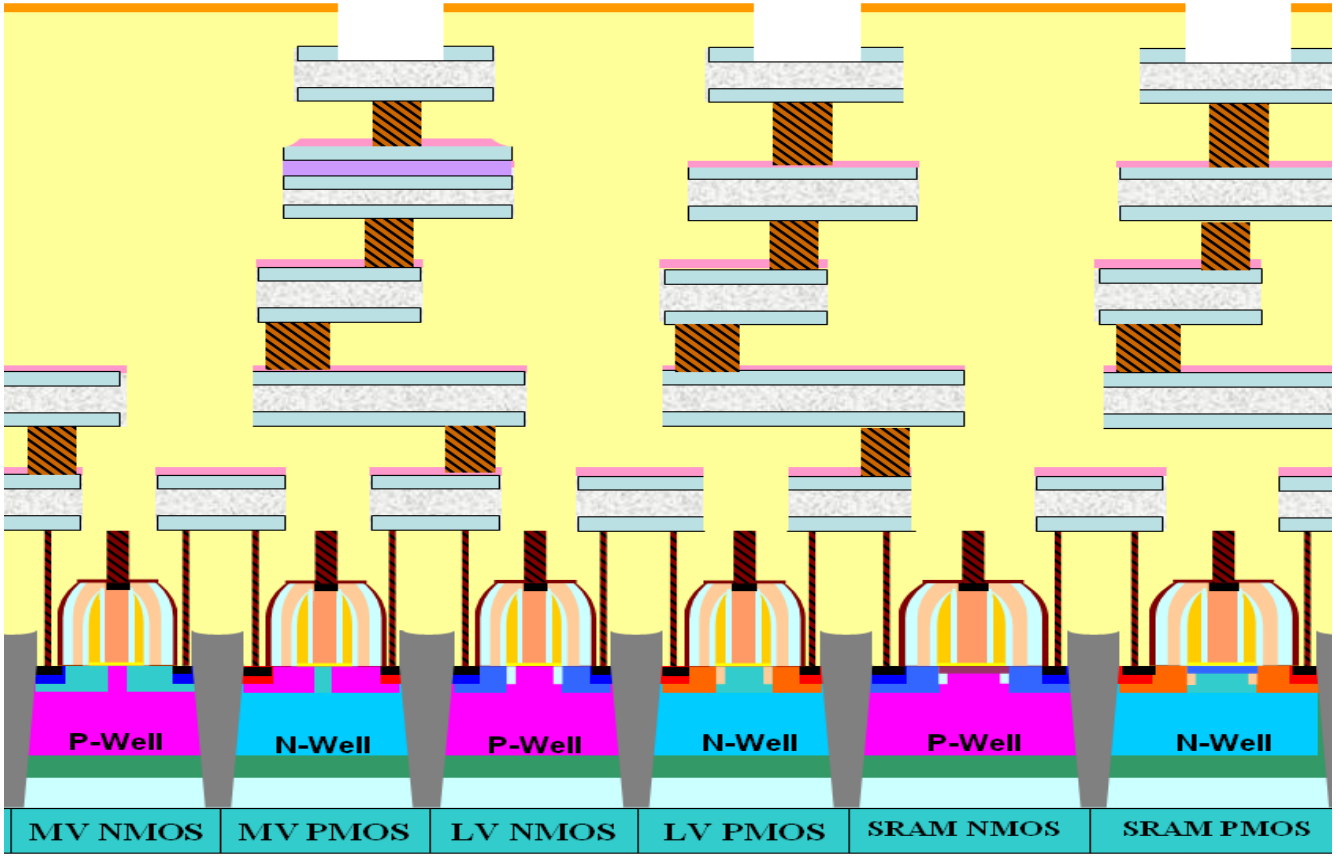
Device	I/O (5V)		Core (1.5V)	
N/PMOS	NMOS	PMOS	RVT	
			NMOS	PMOS
W/L (um)	10/0.6	10/0.5	10/0.11	10/0.11
Gox (A)	150		25	
Vt (V)	0.711	-0.79	0.61	-0.61
Idsat (uA/um)	468	-291	425	-170
Ioff (pA/um)	10	-10	2	-2
BV N/PMOS (V)	> 7	<-7	> 3.5	< -3.5

110LP Process 5V/1.5V EDR

Item Name	(W / L) um	Unit	Lower	Target	Upper
Rs_N+AA_NC	W=5um	ohm/sqr	47	82	117
Rs_P+AA_NC	W=5um	ohm/sqr	83	131	179
Rs_N+POLY_NC	W=5um	ohm/sqr	241	445	649
Rs_P+POLY_NC	W=5um	ohm/sqr	298	418	538
Rs_N+AA_CO	W=5um	ohm/sqr	5.3	8.3	11.3
Rs_P+AA_CO	W=5um	ohm/sqr	5.1	8.1	11.1
Rs_N+POLY_CO	W=5um	ohm/sqr	6	9	12
Rs_P+POLY_CO	W=5um	ohm/sqr	5.9	8.9	11.9
Rs_Metal 1	W=0.144um	ohm/sqr	0.180	0.350	0.510
Rs_Metal n	W=0.18um	ohm/sqr	0.065	0.11	0.146
Rs_Top Metal(10K)	W=0.39um	ohm/sqr	0.008	0.029	0.052
Rs_Top Metal(12K)	W=0.6um	ohm/sqr	0.006	0.027	0.050
Rs_Top Metal(30K)	W=2.0um	ohm/sqr	0.001	0.0107	0.02
Rs_UHR(Hi-R Poly)	W=1.0um	ohm/sqr	1580	2100	2620

Item Name	(W / L) um	Unit	Lower	Target	Upper
Rc_N+AA	0.12um	ohm/cont	8.5	14	21.5
Rc_P+AA	0.12um	ohm/cont	8.5	14	21.5
Rc_N+POLY	0.12um	ohm/cont	7.5	12	20.5
Rc_P+POLY	0.12um	ohm/cont	7.5	11.5	18.5
Rc_Via n	0.16um	ohm/via	2	10	22
Rc_Top Via TM(10K/12K)	0.16um	ohm/via	2	10	22
Rc_Top Via TM(30K)	0.36um	ohm/via	0.4	1.85	4

110LP Process Physical Structure



110LP Process Flow and Photo Count

NO.	Layer	Description
1	1F	AA
2	3D	MV&LV NWell
3	4D	MV&LV PWell
4	5D	LVRVT Vtp
5	6D	LVRVT Vtn
6	1D	SRAM Vtp
7	2D	SRAM Vtn
8	2E	LV define
9	1G	Poly
10	5N	MV NLDD
11	5P	MV PLDD
12	1N	LV NLDD
13	1P	LV PLDD
14	2P	P+ S/D
15	2N	N+ S/D
16	3E	SAB

NO.	Layer	Description
17	1C	CONTACT(1)
18	1M	METAL(1)
19	1T	THROUGH HOLE(1)
20	2M	METAL(2)
21	2T	THROUGH HOLE(2)
22	3M	METAL(3)
23	3T	THROUGH HOLE(3)
24	4M	METAL(4)
25	4T	THROUGH HOLE(4)
26	5M	METAL(5)
27	PV	PASSIVATION

Optional layer: 3 layers

NO.	Layer	Description
1	1I	DNW
2	*K	*MIM Cap
3	8E	MTP Tunnel Ox define

➢**MTP need 1I&8E mask**

- **Standard (1P5M, memory compiler, OTP)**
- **Total masks (1P5M): Standard→25/masks(27 photo layers)**

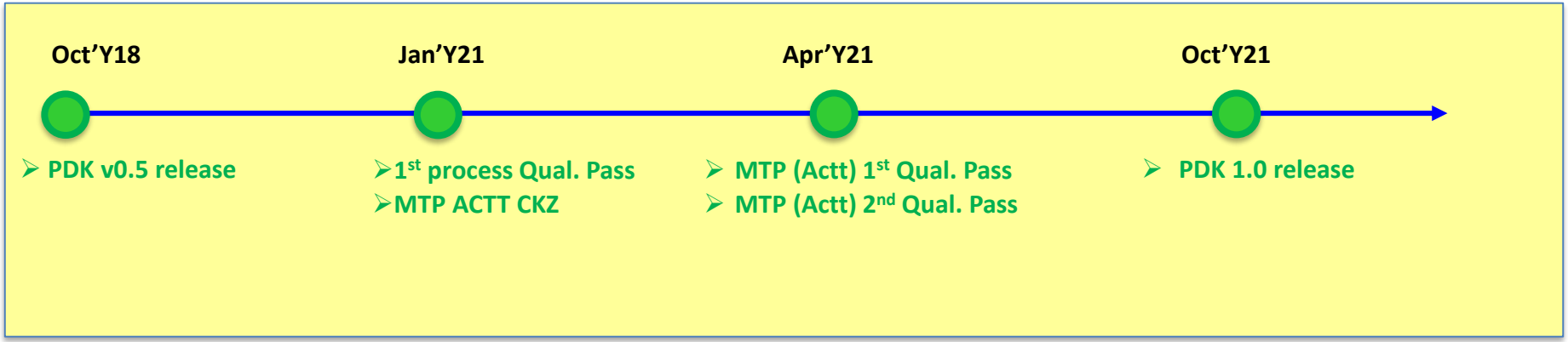
Note:

➢**LV device contain LVRVT, LVLVT at the same time; 5D/6D mask for LVRVT, LVLVT borrow 1N/1P mask;**

➢**LV device only LVRVT; LVRVT(5D/6D) borrow 1N/1P mask.**

Nexchip 110LP Platform Milestone

Release PDK 1.0 at Oct'21.



Thanks | 谢谢聆听