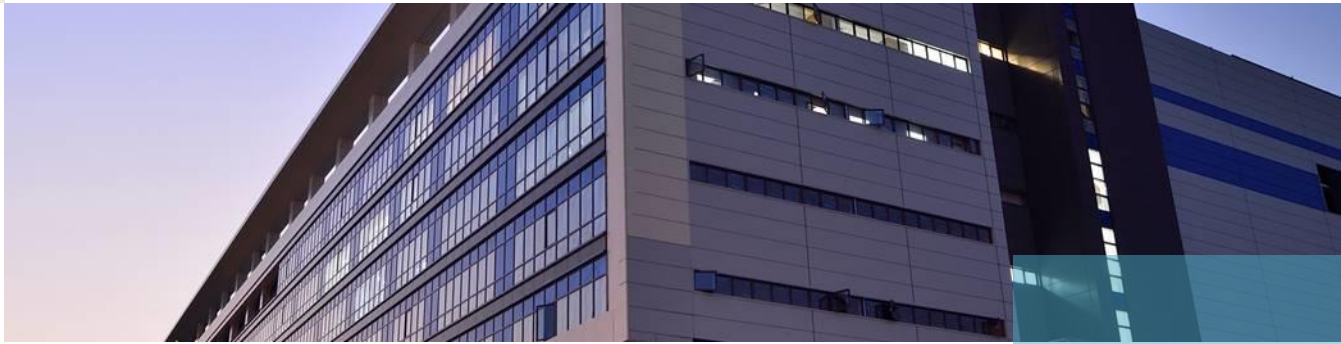
Nexchip

Confidential



Nexchip 110LP_eFlash Promotion Kit

2021. 09

Nexchip Advantage

➢全自动12吋产线

- 产线全自动晶圆搬运
- 生产日志自动生成上传

➢设备提供工艺进一步微缩性
➢(部份设备可达2xnm)

➢Inline control/自动化
➢(提高效率、稳定性)

➢更充沛的产能提供确保
➢(N1厂~N4厂,逐步并依计划扩充)

➢更佳的电脑整合制造能力
➢(8" - lot level; 12" - wafer level)

➢更良好制程工艺能力
➢(具延续性,可控制性,可追朔性)

➢更多的gross dies
➢(2.3~2.4x倍)

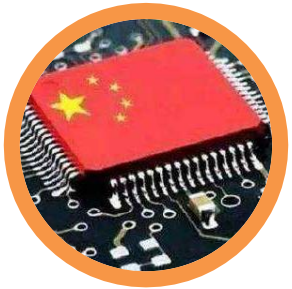
➢更优异交期能力
➢(1.8D / layer, 正常量产时)

➢更优资的缺陷密度值
➢(LDDI D0 ~ 0.1)

➢更高的良率
➢(LDDI ~ 97%)

➢贴近服务

➢+



➢中国制造

➢更近的距离
➢更快捷的市场反应
➢更低的物流成本

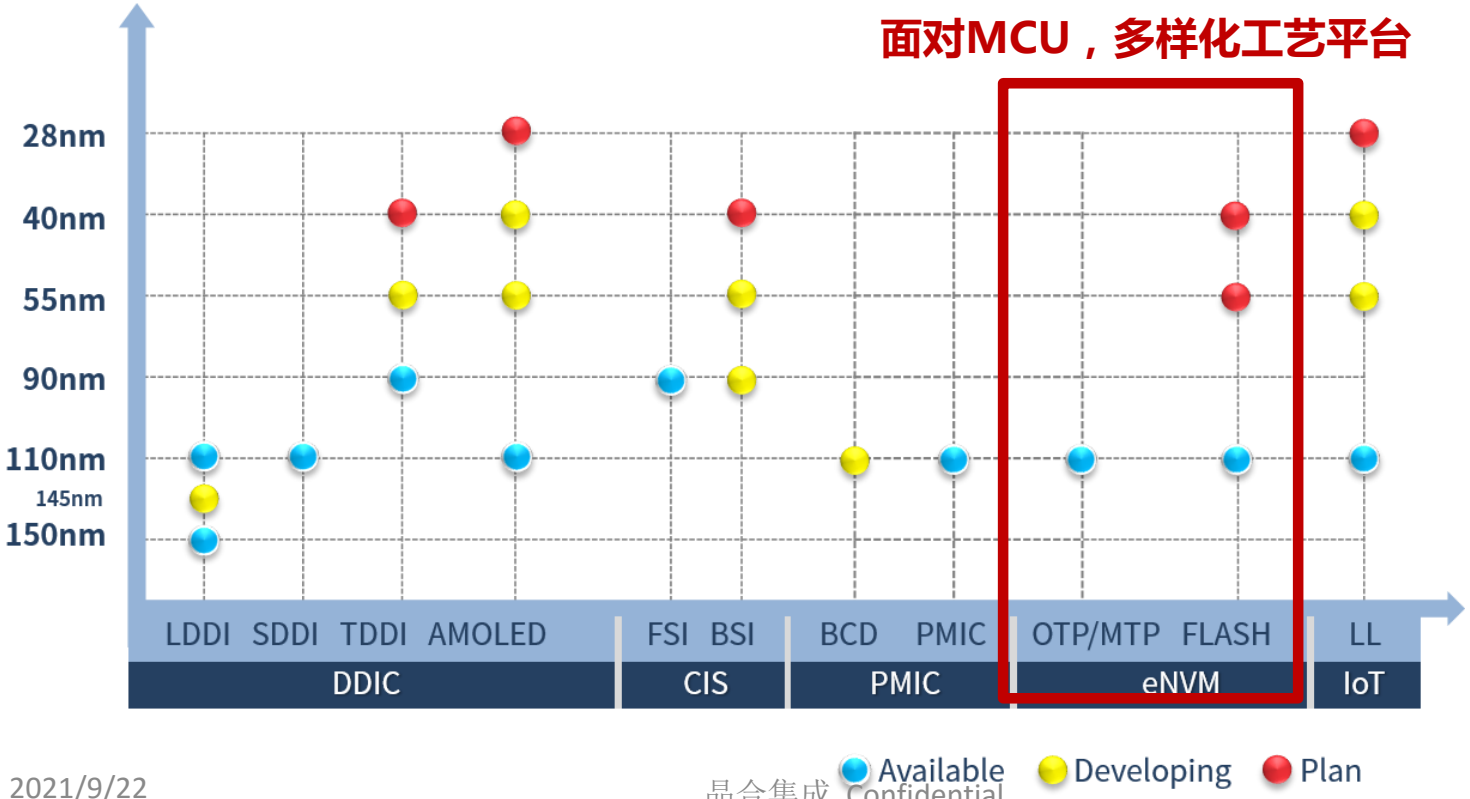
➢更多的资源投入
➢好的产业环境
➢更稳定的市场战略

➢长江三角洲经济区块链 / 集中的供应链

➢产业快速发展+中国制造优先

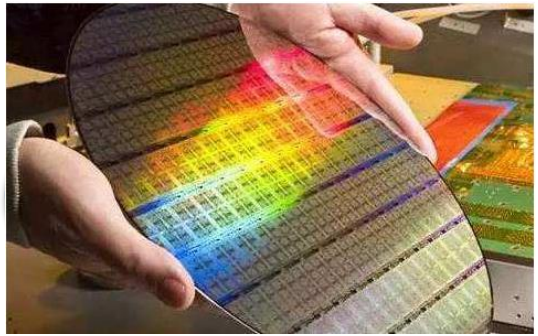
Nexchip Advantage

➢Nexchip 多样化工艺平台，丰富的工艺节点，12’ Foundry



Nexchip 110LPEF offers the MCU solution

110nm LPEF



- **Compatible to Logic process**
  - -- Same Model/PDK
  - -- IPs and Libraries can be re-used
- **Comprehensive eNVM solution**
  - -- pFlash
  - -- Excellent partners for customization IPs

MCU application

Consumer

Digital AV
Home Applications
Touch Controller…

Communication

Cell Phone
Mobile Handsets
Broadband Access…

Data Processing

Printer
Notebook
Smart Cards
Work Stations …

Industrial

Medical monitor
Motor Control
Building Management
…

Nexchip 110nm LPEF Process information

- **110nm LPEF: Flash IP(pFlash) embedded in Nexchip 110nm logic.**
  a) Logic: 23 lithos (5Metal with Al-BEOL)
  b) Flash: 11 lithos; 9 lithos (2021-2H)

Category	Content
Device	1.5v Core + 5v IO + Flash
Design rule	110LP(1.5v)
Technology	2P5M
Cell Type	2 Transistor (2T)
Flash/Total Layers	11/34(included SRAM)
Isolation	STI
Gate Material & Source/Drain	Co-Salicide
BEOL	NSC 110LP Al-BEOL

Nexchip 110nm LPEF Photo & Mask information

NO.	Layer	Description	Photo type	Pellicle type		Mask Tone	Grade.	Minimum line/space (um)
1	1F	AA	KrF	KrF	6%HT	Dark	I	0.16/0.16
2	2I	MV NWell	KrF	KrF	Binary	Clear	B	0.9/0.9
3	3I	MV PWell	KrF	KrF	Binary	Clear	B	0.9/0.9
4	4I	CG VT	KrF	KrF	Binary	Clear	B	0.4/0.4
5	5I	Cell VT	KrF	KrF	Binary	Clear	B	0.9/0.9
6	2G	FG(P0)	KrF	KrF	6%HT	Dark	J	0.23/0.13
7	3D	LV NWell	KrF	KrF	Binary	Clear	E	0.75/0.75
8	4D	LV PWell	KrF	KrF	Binary	Clear	E	0.75/0.75
9	6E	ONO	I-line	KrF	Binary	Dark	B	0.42/0.42
10	2E	Sacrifice gate	I-line	KrF	Binary	Dark	C	0.42/0.42
11	3G	CG	KrF	KrF	6%HT	Dark	J	0.18/0.16
12	8N	MV NLDD	KrF	KrF	Binary	Clear	D	0.4/0.4
13	8P	MV PLDD	KrF	KrF	Binary	Clear	D	0.4/0.4
14	9N	CSD	KrF	KrF	Binary	Clear	D	0.4/0.4
15	1G	Poly gate	KrF	KrF	6%HT	Dark	J	0.11/0.20
16	1N	LV NLDD	KrF	KrF	Binary	Clear	D	0.31/0.31
17	1P	LV PLDD	KrF	KrF	Binary	Clear	D	0.31/0.31
18	4N	ESD	KrF	KrF	Binary	Clear	C	0.31/0.31
19	2P	P+ S/D	KrF	KrF	Binary	Clear	E	0.31/0.31
20	2N	N+ S/D	KrF	KrF	Binary	Clear	E	0.31/0.31
21	3E	SAB	I-line	KrF	Binary	Dark	C	0.42/0.42

Nexchip 110nm LPEF Photo & Mask information

NO.	Layer	Description	Photo type	Pellicle type		Mask Tone	Grade.	Minimum line/space (um)
22	1C	CONTACT(1)	KrF	KrF	6%HT	Clear	J	0.12/0.16
23	1M	METAL(1)	KrF	KrF	6%HT	Dark	I	0.144/0.144
24	1T	THROUGH HOLE(1)	KrF	KrF	6%HT	Clear	I	0.16/0.20
25	2M	METAL(2)	KrF	KrF	6%HT	Dark	G	0.18/0.20
26	2T	THROUGH HOLE(2)	KrF	KrF	6%HT	Clear	I	0.16/0.20
27	3M	METAL(3)	KrF	KrF	6%HT	Dark	G	0.18/0.20
28	3T	THROUGH HOLE(3)	KrF	KrF	6%HT	Clear	I	0.16/0.20
29	4M	METAL(4)	KrF	KrF	6%HT	Dark	G	0.18/0.20
30	4T	THROUGH HOLE(4)	KrF	KrF	6%HT	Clear	I	0.16/0.20
31	5M	METAL(5)	KrF	KrF	Binary	Dark	D	0.39/0.40
32	PV	PASSIVATION	I-line	KrF	Binary	Clear	B	1.5/1.5

Total masks (2P5M): Standard 32 masks (KrF:28 PH layers, I-Line:4 PH layers) ,

Optional layer: 6 layers

NO.	Layer	Description	Photo type	Pellicle type		Mask Tone	Grade.	Minimum line/space(um)
1	5D	LVRVT Vtp	KrF	KrF	Binary	Clear	D	0.31/0.31
2	6D	LVRVT Vtn	KrF	KrF	Binary	Clear	D	0.31/0.31
3	1D	SRAM Vtp	I-line	KrF	Binary	Clear	D	1.0/1.0
4	2D	SRAM Vtn	I-line	KrF	Binary	Clear	D	1.0/1.0
5	*K	*MIM Cap	KrF	KrF	Binary	Dark	C	4.0/0.8
6	AR	COG mark	I-line	KrF	Binary	Clear	B	1.5/1.5

Nexchip 110nm LPEF Process Key Design Rules

Process	110nm LPEF (Width/Space) (um)
Active	0.16/0.16
Poly	0.11/0.20
CT	0.12/0.16
M1	0.144/0.144
Via n	0.16/0.2
Metal n	0.18/0.20
TM	0.39/0.40
SP-SRAM	1.32um^2

Nexchip 110nm LPEF Device Performance

Device	Core (1.5V)				IO (5V)	
N/PMOS	RVT (TT@25'C)		LVT (TT@25'C)		VT (TT@25'C)	
	NMOS	PMOS	NMOS	PMOS	NMOS	PMOS
W/L (um)	10/0.11	10/0.11	10/0.11	10/0.11	10/0.45	10/0.6
Gox (A)	25		25		150	
Vt (V)	0.61	-0.61	0.435	-0.48	0.78	-0.75
Idsat (uA/um)	425	-170	565	-220	475	-250
Ioff (pA/um)	2	-2	500	50	2	-2
BV N/PMOS (V)	> 3.5	< -3.5	> 3.0	< -3.5	> 11.5	< -11.5

➢Nexchip offer the competitive 110nm LPEF platform.

- 1.5V Core , RVT /LVT for speed/leakage optimization
- 5V I/O from Flash HV devices
- Compact Stdcell: 7T (319K gate/mm2), 9T (212K gate/mm2)
- Compact SRAM(1.32um2) memory compiler
- High-R poly (2K ohm/sq, w/o extra mask)
- MIM (2fF/um2, single stack)
- Built-in Schottky diode (SBD)

Nexchip 110nm LPEF Foundation IPs

IPs		Brief Specs			Readiness/Schedule		
STD Cell	Library	Category	Track (T)	Vt	DK	Si Report	Gradation
	Standard Cell Library	HD	7	RVT / LVT	V	V	Iron
		HS	9	RVT / LVT	V	V	Iron
	ECO Library	HD	7	RVT / LVT	V	V	Iron
		HS	9	RVT / LVT	V	V	Iron
	PMK	HD	7	RVT / LVT	V	V	Iron
		HS	9	RVT / LVT	V	V	Iron
Memory Compiler	Category	Function	Bit Cell (um2)	Vt	DK	Si Report	Gradation
	Generic	SP SRAM	1.32	RVT	V	V	Iron
IO	Category	Brief Specs			DK	Si Report	Gradation
	GPIO	2.0v~5.5v, Provides a wide variety of interrupt I/O for customers, Includes ultra-low power crystal driver: 150nA,32.768KHz XTAL; <60uA, 16MHz XTAL.			V	V	Iron
	ESD Protection	HBM>+/-4kV, MM>+/-200V, CDM>+/-500V, Latch-up>+/-200mA			V	2021/10/M	Paper

Nexchip 110nm LPEF MCU platform IP (1)

IP Category	IP name	Brief Specs	DK	Si Verified	Gradation
POR	With static current POR (for core voltage)	Internal counter to set power-on-reset time; 1.5V device only; With static current; Internal low voltage detector (1.1V)	V	V	Iron
	With static current POR (for IO voltage)	Internal counter to set power-on-reset time; 5V device only; With static current; Internal low voltage detector (1.8V)	V	V	Iron
	No static current POR (for core voltage)	Internal counter to set power-on-reset time; 1.5V device only; No static current; Internal low voltage detector (1.1V)	V	V	Iron
	No static current POR(for IO voltage)	Internal counter to set power-on-reset time; 5V device only; No static current; Internal low voltage detector (1.8V)	V	V	Iron
LDO	5V->1.5V low power LDO	Low to 0.8uA standby current; 120mA driving ability; Typically output 1.5V voltage, output range: 1.1V~1.8V.	V	V	Iron
	5V->1.5V capacitor-free LDO	Supports capacitor-free, fast transient; Typically 1.5V output voltage, 150mA driving ability, output range: 1.1V~1.8V.	V	V	Iron
DC-DC	Low power 5V-->1.5V Buck DC-DC converter	Quiescent current is low to 50uA(exclude BGP) Ultra-low shutdown leakage:100nA PWM and PFM model Low output ripple: <25mV 400mA peak output Current(Vin≥3.0V) Over-voltage and under-voltage protection Output Short and over-current protection	V	2021/12/E	Paper
IRC	8MHz RC OSC	Oscillator output frequency; Accuracy <1.5% @PVT Operating junction temperature: -40°C~+25°C~+125°C;	V	V	Iron
	48MHz RC OSC	Oscillator output frequency; Accuracy <1.5% @PVT Operating junction temperature: -40°C~+25°C~+125°C;	V	V	Iron
PLL	Delta-sigma fractional-N PLL	Supports integer-N divider application Supports 6MHz to 180MHz input clock frequency range output clock range from 25MHz to 1.0GHz Fractional-N divider application: <2.0ps@1GHz	V	V	Iron

Nexchip 110nm LPEF MCU platform IP (2)

IP Category	IP name	Brief Specs	DK	Si Verified	Gradation
ADC	Normal 12bit 3Msps SARADC	Supports 1Ksps~3Msps sampling rate; 16CH single-ended/8CH differetial; SNR:64dB @2Msps; THD:-72dB @2Msps;	V	2022/03/E	Paper
Interface	Crystal-less USB1.1 PHY	Low cost; Low EMI TX driver design	V	2021/12/E	Paper
	Crystal-less USB2.0 device PHY total solution	Ultra-low cost; 2-channel capacitor-free LDOs, fast transient: 5V->3.3V 250mA capacitor-free LDO, 5V->1.8V 120mA capacitor-free LDO;	V	2021/12/E	Paper
BGP	Ultra-low power bandgap	0.8V output reference with trimming registers Integrated reference voltage stability dectector	V	V	Iron
	Low noise and high PSRR bandgap	0.8V output reference with 5/6bit trimming registers, integrated buffered reference output As low as 20uA power consumption to realize low noise: 400uV@1Hz~10MHz High PSRR: ≥60dB@1KHz	V	2021/12/E	Paper

Nexchip IP Gradation

Nexchip 110nm LPEF Flash(ISSI) IP

Nexchip can offer varied density flash Macro(new design version).

	Macro spec	Macro spec	Macro spec	Macro spec	Macro spec	(UNIT)	Notes
Basic							
Memory Organization	16K	32K	64K	128K	256K	Bytes	Total density
Configuration(bit width)	x32	x32	x32	x32	x32	Bit	
Array bank	1	1	1	1	2	ea	
Page Size	1K	1K	1K	1K	1K	Bytes	
Information block	1Kbyte * 2	1Kbyte * 2	1Kbyte * 2	1Kbyte * 2	1Kbyte * 2	Bytes	
Endurance	100	100	100	100	100	K cycles	min
Data Retention	10	10	10	10	10	Years	min
Operation Temperature	-40C~85C	-40C~85C	-40C~85C	-40C~85C	-40C~85C	C	
Timing							
Access Time/Read cycle	40	40	40	40	40	ns	max
Byte Program Time	20	20	20	20	20	us	max
Page Erase Time	2	2	2	2	2	ms	max
Macro Erase Time	10	10	10	10	10	ms	max
Power							
Supply Voltage	1.5	1.5	1.5	1.5	1.5	V	
Standby current	1/20	1/20	1/20	1/20	1/20	uA	typ./max
Read current at 1MHz	350	350	350	350	400	uA	max
Program current	4/5	4/5	4/5	4/5	4/5	mA	typ./max
Erase current	4/5	4/5	4/5	4/5	4/5	mA	typ./max
Macro size							
Macro size	**0.63**	**0.69**	**0.79**	**0.99**	**1.67**	mm2	after shrink

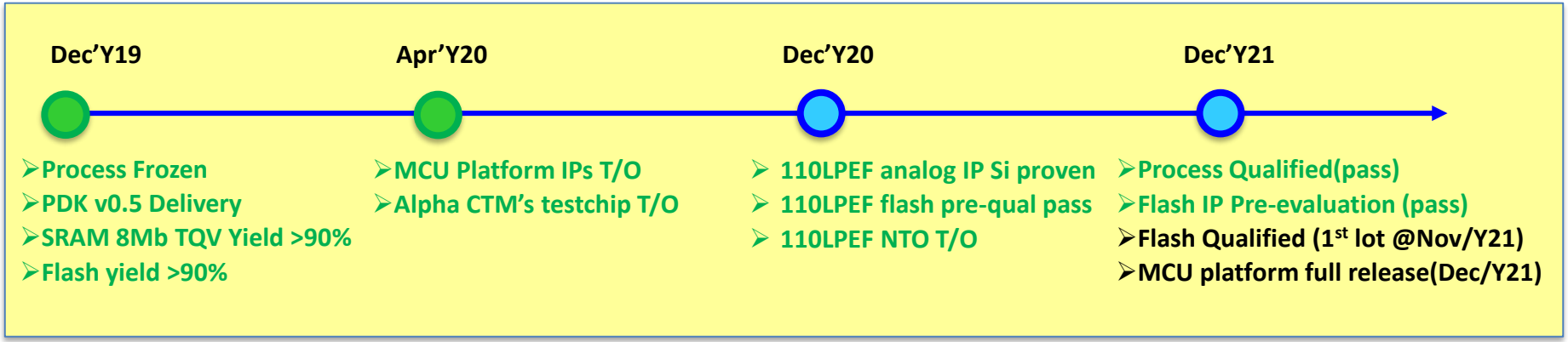
Nexchip' Cooperative Partner

Nexchip have good ecosystem and excellent customer service.

IP Alliance	M31, ememory, YMC, Syntronix, INNOPOWER, ISSI, Aett
EDA Alliance	Mentor A Siemens Business, SYNOPSYS, cadence, Empyrean
Mask Service Alliance	PDMC, TCE, TOPPAN
Back End Service	UMC UNIONSEMICON, CHIPMORE, CHIPBOND, ChipMOS

Nexchip 110nm LPEF Platform Milestone

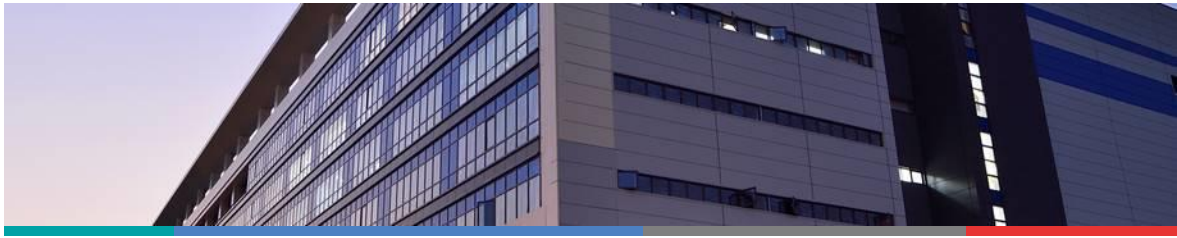
Platform alpha release at Dec'20; full Release at Dec'21.



Cooperation and Win-Win !

双赢

Thanks | 谢谢聆听



量产与研发

产品线		已量产	研发进度
			2021 Q1 Q2 Q3 Q4 / 2022 Q1 Q2 Q3 Q4 / 2023 Q1 Q2 Q3 Q4 / 2024 Q1 Q2 Q3 Q4 / 2025 Q1 Q2 Q3 Q4
DDIC	LDDI	➢150nm 3.3V/13.5 ➢150nm 3.3V/18V ➢150nm 1.8V/18V ➢110nm 1.5V/6V/32V ➢90nm 1.32V/6V	➢145nm 1.8V/18V ➢110nm 1.5V/7V/32V ➢110nm 1.2V/18V
	SDDI	➢110nm 1.2V/6V/32V ➢110nm 1.5V/6V/32V	
	TDDI	➢90nm-AL 1.32V/6V/32V	➢55nm 1.2V/6V/32V ➢40nm 1.2V/6V/32V
	AMOLED	➢110nm 1.5V/6V/32V	➢55nm 1.2V/8V/32V ➢40nm 1.1V/8V/32V ➢28nm 0.9V/8V/32V

量产与研发

产品线		已量产	研发进度																			
			2021				2022				2023				2024				2025			
			Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4
CIS	FSI		➢90nm-FSI 1.32V/3.3V																			
	BSI				➢90nm-BSI 1.32V/3.3V						➢55nm-BSI 1.2V/3.3V				➢40nm-BSI 1.2V/3.3V							
PMIC	BCD						➢110nm 1.5V/5V/12~200V															
	PMIC	➢110nm 5V																				
eNVM	OTP/MTP	➢110nm 1.5V/5V																				
	Flash	➢110nm ➢1.5V/5V							➢55nm 1.2V/3.3V						➢40nm 1.2V/3.3V							
IoT	LL		➢55nm-LL 1.2V/2.5V								➢40nm-LL 1.1V/1.8V&2.5V								➢28nm-LL 0.9~1.05V/1.8V			

Nexchip IP Gradation

Grade	Definition	IP Gradation
1	PDK V0.1+	Paper
2	PDK V0.5+ and either 1) IP Si-proven or 2) Production < 200 pcs	Iron
3	PDK V0.5+ /and IP Si-proven /and Production 200~500 pcs	Bronze
4	PDK V0.5+ /and IP Si-proven /and Production 500~2000 pcs	Silver
5	PDK V1.0+ /and IP Si-proven /and Production 2k~10k pcs	Gold
6	PDK V1.0+ /and IP Si-proven /and Production > 10k pcs	Platinum