TF Semiconductor Solutions

TF2101M

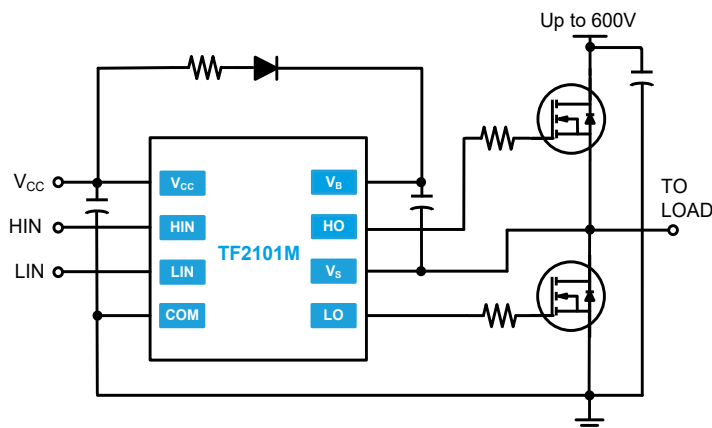## *High-Side and Low-Side Gate Driver*

Features

- **Floating high-side driver in bootstrap operation to 600V**
- **Drives two N-channel MOSFETs or IGBTs in high-side/ low-side configuration**
- **Outputs tolerant to negative transients**
- **Wide low-side gate driver and logic supply: 10V to 20V**
- **Logic inputs CMOS and TTL compatible (down to 3.3V)**
- **Schmitt triggered logic inputs with internal pull down**
- **Undervoltage lockout for V$_{CC}$**
- **Space-saving SOIC-8 package available**
- **Extended temperature range:-40°C to +125°C**

Applications

- DC-DC Converters
- AC-DC Inverters
- Motor Controls
- Class D Power Amplifiers

Description

The TF2101M is a high voltage, high speed gate driver capable of driving N-channel MOSFETs and IGBTs in a high-side/ low-side configuration. TF Semiconductor's high voltage process enables the TF2101M's high-side to switch to 600V in a bootstrap operation. The 50ns (max) propagation delay matching between the high and the low side drivers allows high frequency switching.

The TF2101M logic inputs are compatible with standard TTL and CMOS levels (down to 3.3V) for easy interfacing with controlling devices. The driver outputs feature high pulse current buffers designed for minimum driver cross conduction. The low-side gate driver and logic share a common ground

The TF2101M is available in a space-saving 8-pin SOIC package and an 8-pin PDIP; the operating temperature extends from -40°C to +125°C .
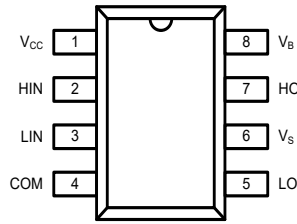
SOIC-8(N)   PDIP-8

Typical Application
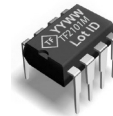
Ordering Information

| PART NUMBER	PACKAGE	PACK / Qty	MARK
			Year Year Week Week
TF2101M-TAU	SOIC-8(N)	Tube / 100	TF YYWW TF2101M Lot ID
TF2101M-TAH	SOIC-8(N)	T & R/ 2500	TF YYWW TF2101M Lot ID
TF2101M-3AS	PDIP-8	Tube / 50	TF YYWW TF2101M Lot ID

Pin Diagrams

Top View: PDIP-8, SOIC-8

TF2101M

Pin Descriptions

PIN NAME	PIN DESCRIPTION
HIN	Logic input for high-side gate driver output (HO), in phase
LIN	Logic input for low-side gate driver output (LO), in phase
V_B	High-side floating supply
HO	High-side gate drive output
V_S	High-side floating supply return
V_{CC}	Low-side and logic fixed supply
LO	Low-side gate drive output
COM	Low-side return
NC	"No connect" pin

Functional Block Diagram
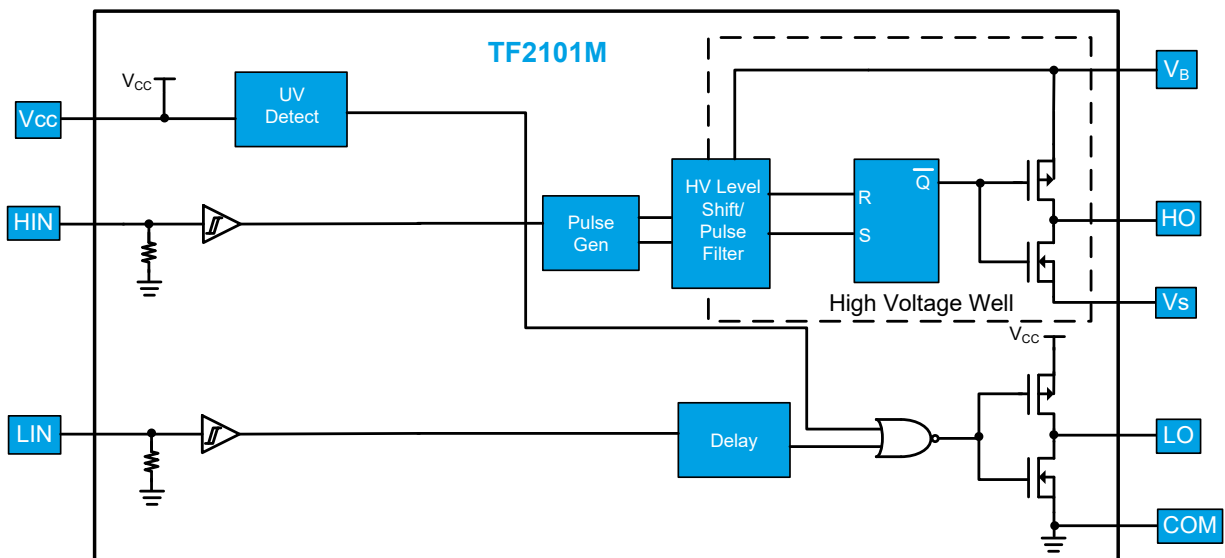
Absolute Maximum Ratings (NOTE1)

V_B - High side floating supply voltage...............-0.3V to +624V
V_S - High side floating supply offset voltage....V_B-24V to V_B+0.3V
V_{HO} - High side floating output voltage...............V_S-0.3V to V_B+0.3V
dV_S / dt - Offset supply voltage transient..............................50 V/ns

V_{CC} - Low side and logic fixed supply voltage..............-0.3V to +24V
V_{LO} - Low side output voltage.................................-0.3V to V_{CC}+0.3V
V_{IN} - Logic input voltage (HIN and LIN)... -0.3V to V_{CC}+0.3V

NOTE1 *Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

P_D - Package power dissipation at $T_A \le 25$ °C
   SOIC-8...0.625W
   PDIP-8...1.0W

SOIC-8 Thermal Resistance **(NOTE2)**
   θ_{JC}...45 °C/W
   θ_{JA}...200 °C/W

PDIP-8 Thermal Resistance **(NOTE2)**
   θ_{JC}...35 °C/W
   θ_{JA}...125 °C/W

T_J - Junction operating temperature ....+150 °C
T_L - Lead temperature (soldering, 10s) .... +300 °C
T_{stg} - Storage temperature range ....-55 °C to +150 °C

NOTE2 *When mounted on a standard JEDEC 2-layer FR-4 board.*

Recommended Operating Conditions

Symbol	Parameter	MIN	TYP	MAX	Unit
V_B	High side floating supply absolute voltage	V_S + 10		V_S + 20	V
V_S	High side floating supply offset voltage	*NOTE3*		600	V
V_{HO}	High side floating output voltage	V_S		V_B	V
V_{CC}	Low side and logic fixed supply voltage	10		20	V
V_{LO}	Low side output voltage	0		V_{CC}	V
V_{IN}	Logic input voltage (HIN and LIN)	0		5	V
T_A	Ambient temperature	-40		125	°C

NOTE3 *Logic operational for V_S = -5 to +600V.*

DC Electrical Characteristics *(NOTE4)*

V_{BIAS} (V_{CC}, V_{BS}) = 15V, T_A = 25 °C , unless otherwise specified.

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
V_{IH}	Logic "1" input voltage	V_{CC} = 10V to 20V **NOTE5**	2.5			V
V_{IL}	Logic "0" input voltage				0.8	V
V_{OH}	High level output voltage, V_{BIAS} - V_O	I_O = 2mA		0.05	0.2	V
V_{OL}	Low level output voltage, V_O	I_O = 2mA		0.02	0.1	V
I_{LK}	Offset supply leakage current	VB = VS = 600V			50	μA
I_{BSQ}	Quiescent V_{BS} supply current	V_{IN} = 0V or 5V		30	55	μA
I_{CCQ}	Quiescent V_{CC} supply current	V_{IN} = 0V or 5V		150	270	μA
I_{IN+}	Logic "1" input bias current	V_{IN} = 5V		3	10	μA
I_{IN-}	Logic "0" input bias current	V_{IN} = 0V			5	μA
V_{CCUV+}	V_{CC} supply under-voltage positive going threshold		8	8.9	9.8	V
V_{CCUV-}	V_{CC} supply under-voltage negative going threshold		7.4	8.2	9	V
I_{O+}	Output high short circuit pulsed current	V_O = 0V, V_{IN} = Logic "1", PW ≤ 10 μs	130	290		mA
I_{O-}	Output low short circuit pulsed current	V_O = 15V, V_{IN} = Logic "0", PW ≤ 10 μs	270	600		mA

AC Electrical Characteristics

V_{BIAS} (V_{CC}, V_{BS}) = 15V, T_A = 25 °C, and C_L = 1000pF, unless otherwise specified.

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
t_{ON}	Turn-on propagation delay	V_S = 0V		160	220	ns
t_{OFF}	Turn-off propagation delay	V_S = 600V		150	220	ns
t_r	Turn-on rise time			70	170	ns
t_f	Turn-off fall time			35	90	ns
t_{DM}	Delay matching				50	ns

NOTE4 *The V_{IN}, V_{TH}, and I_{IN} parameters are referenced to COM. The V_O and I_O parameters are referenced to COM and are applicable to the respective output pins: HO and LO.*

NOTE5 *For optimal operation, it is highly recommended that the input pulse (to HIN and LIN) should have an amplitude of 2.5V minimum with a pulse width of 300ns minimum.*
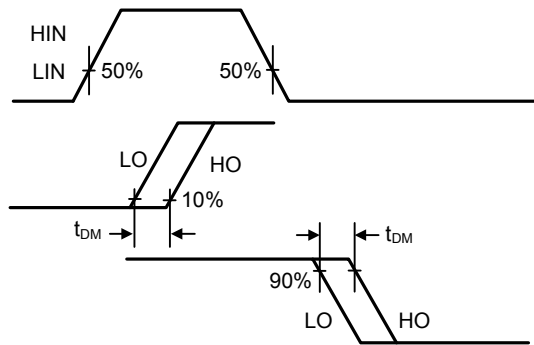
Timing Waveforms
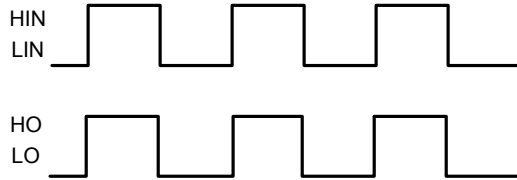
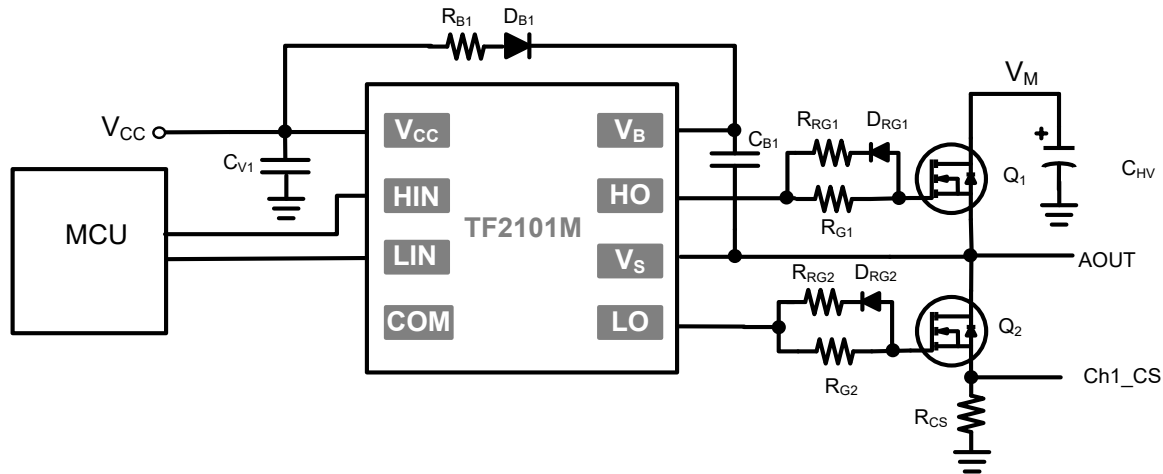**Figure 1.** Input / Output Timing Diagram
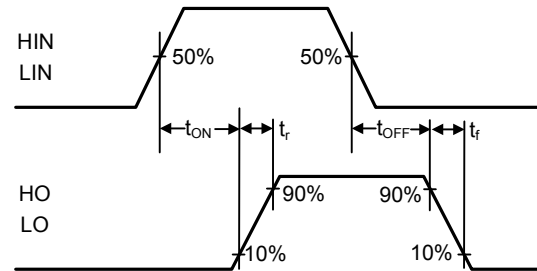
Figure 2. Switching Time Waveform Definitions

Figure 3. Delay Matching Waveform Definitions

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Application Information

Figure 4. Single phase (of four) for Stepper motor driver application using the TF2101M

■ RRG1 and RRG2 values are typically between 0Ω and 10Ω, exact value decided by MOSFET junction capacitance and drive current of gate driver; 10Ω is used in this example.

■ It is **highly recommended** that the input pulse (to HIN and LIN) should have an amplitude of 2.5V minimum (for VDD=15V) with a minimum pulse width of 300ns.

■ RG1 and RG2 values are typically between 10Ω and 100Ω, exact value decided by MOSFET junction capacitance and drive current of gate driver; 50Ω is used in this example.

■ RB1 value is typically between 3Ω and 20Ω, exact value depending on bootstrap capacitor value and amount of current limiting required for bootstrap capacitor charging; 10Ω is used in this example. Also DB should be an ultra fast diode of 1A rating minimum and voltage rating greater than system operating voltage.

Typical Characteristics
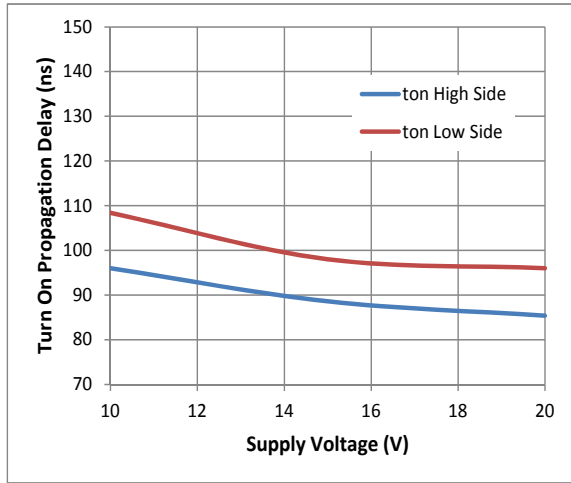
Figure 5. Turn-on Propagation Delay vs. Supply Voltage
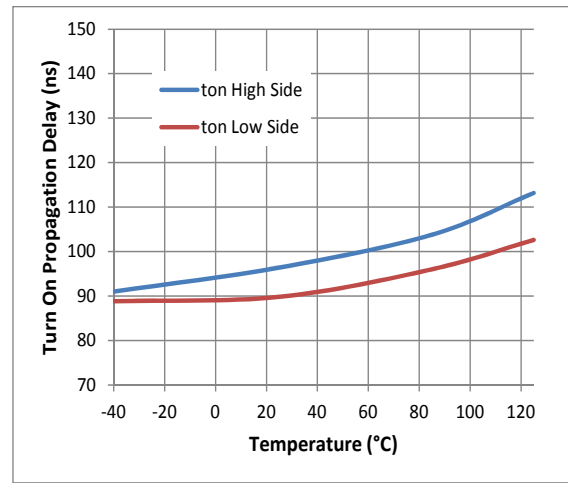
Figure 6. Turn-on Propagation Delay vs. Temperature
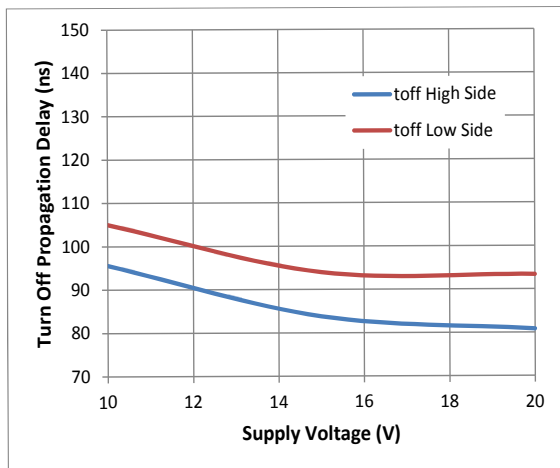
Figure 7. Turn-off Propagation Delay vs. Supply Voltage
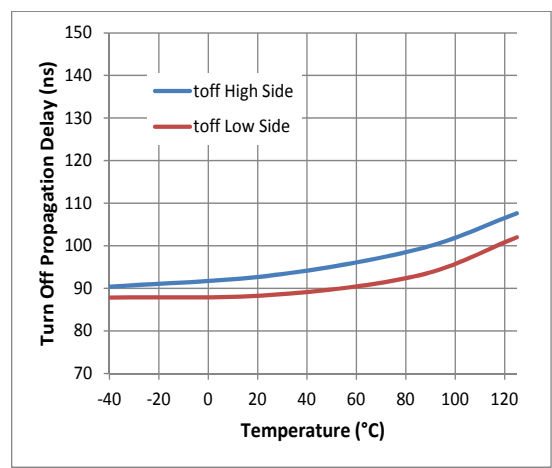
Figure 8. Turn-off Propagation Delay vs. Temperature
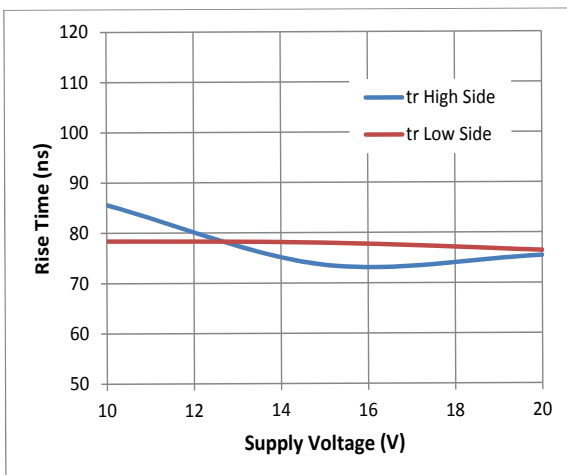
Figure 9. Rise Time vs. Supply Voltage
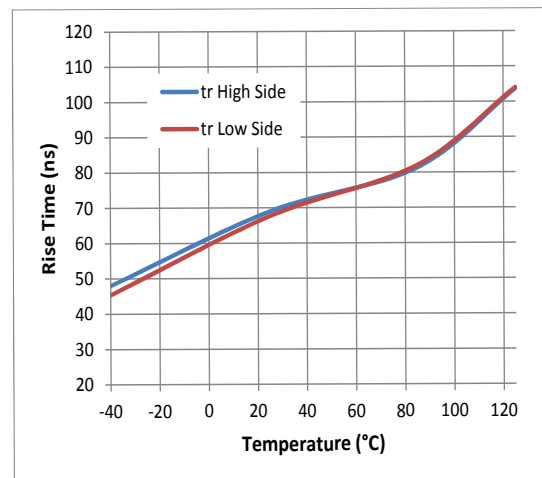
Figure 10. Rise Time vs. Temperature

Typical Characteristics, cont'd
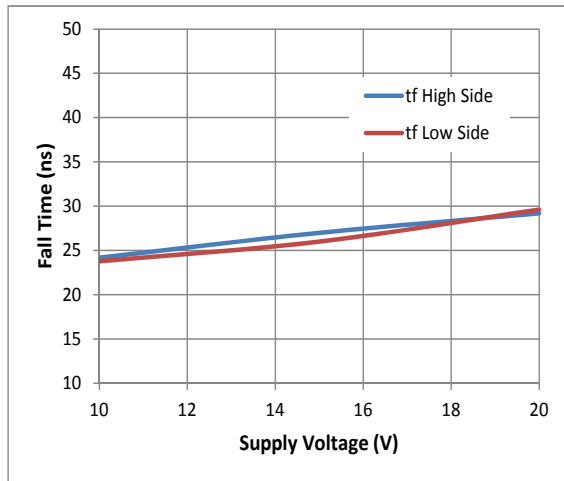
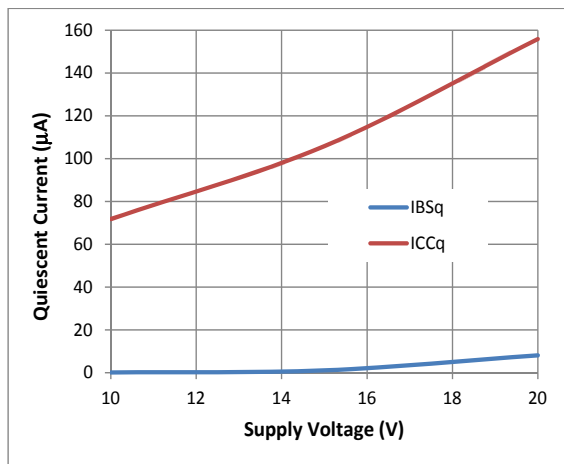**Figure 11.** Fall Time vs. Supply Voltage
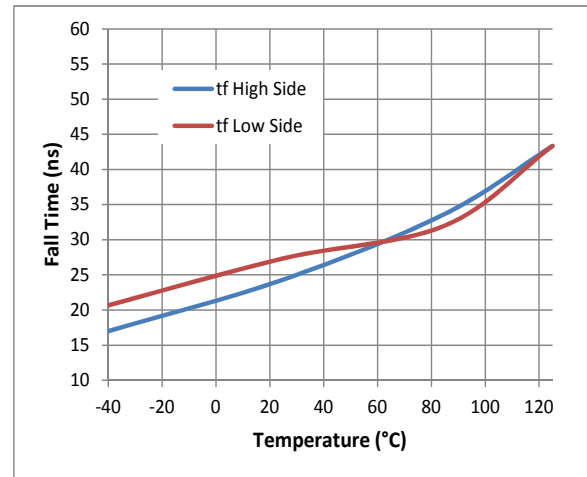
Figure 12. Fall Time vs. Temperature

Figure 13. Quiescent Current vs. Supply Voltage
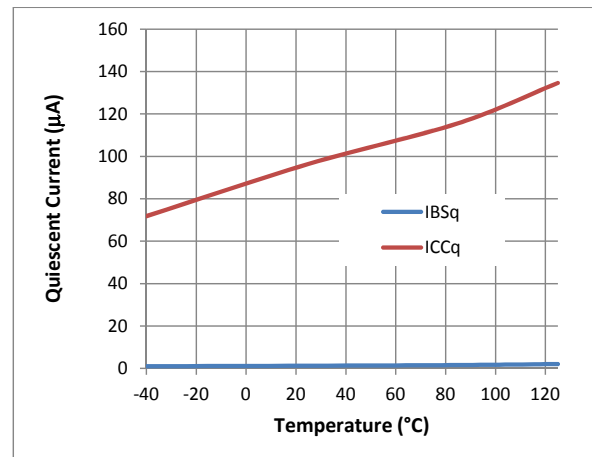
Figure 14. Quiescent Current vs. Temperature
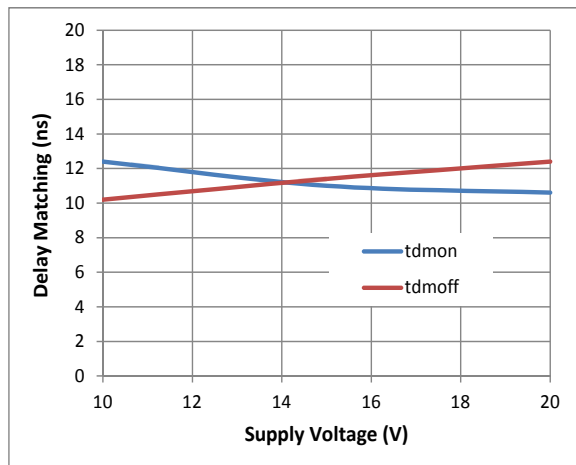
Figure 15. Delay Matching vs. Supply Voltage
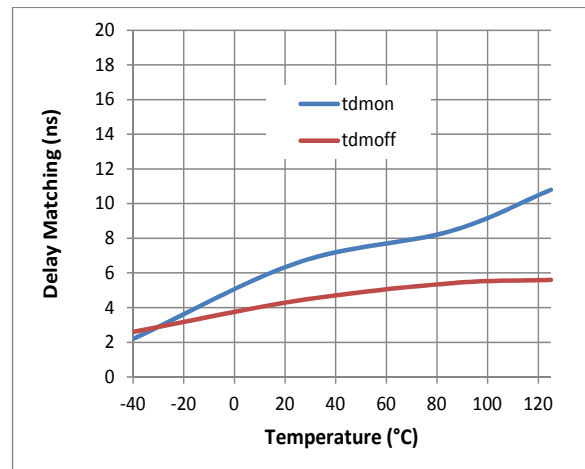
Figure 16. Delay Matching vs. Temperature

Typical Characteristics, cont'd
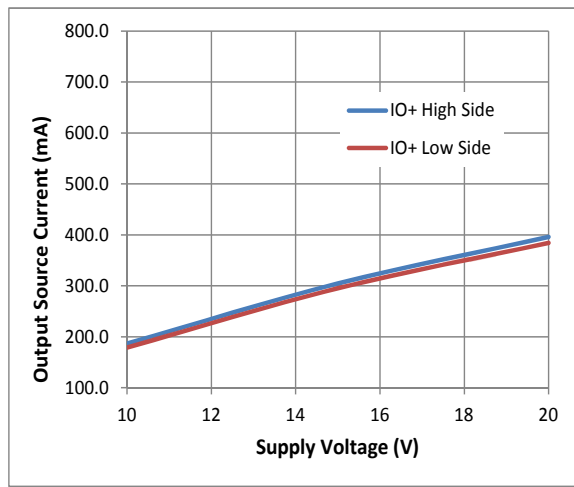
Figure 17. Output Source Current vs. Supply Voltage
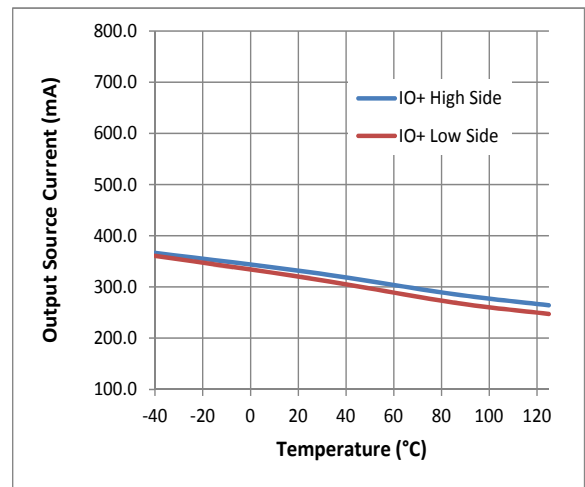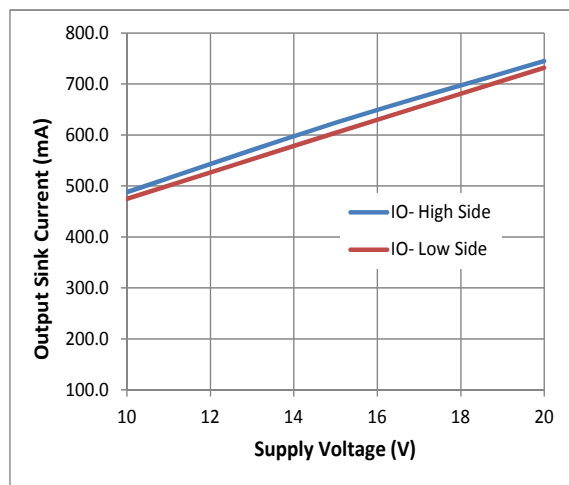

Figure 18. Output Source Current vs. Temperature

Figure 19. Output Sink Current vs. Supply Voltage
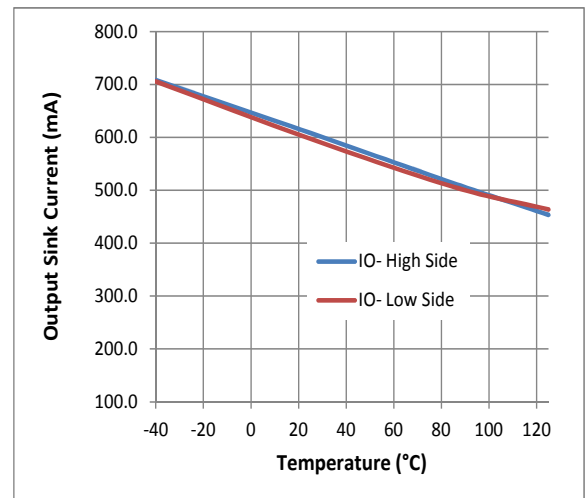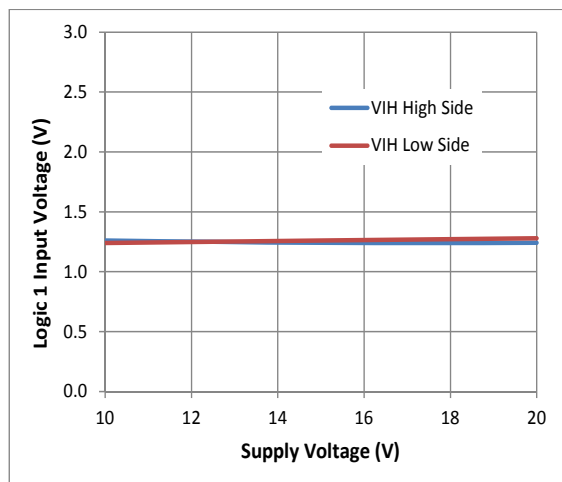

Figure 20. Output Sink Current vs. Temperature
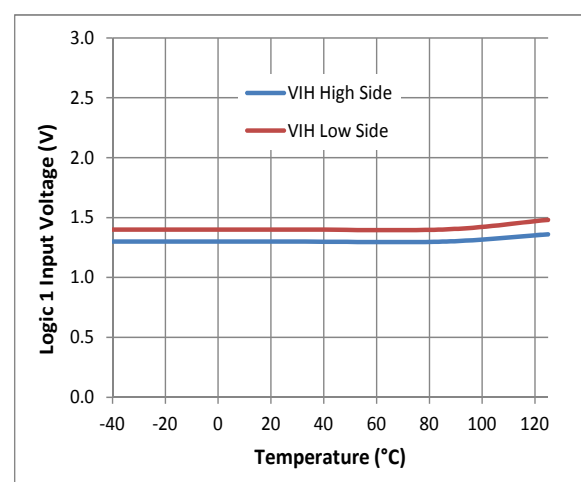

Figure 21. Logic 1 Input Voltage vs. Supply Voltage

Figure 22. Logic 1 Input Voltage vs. Temperature
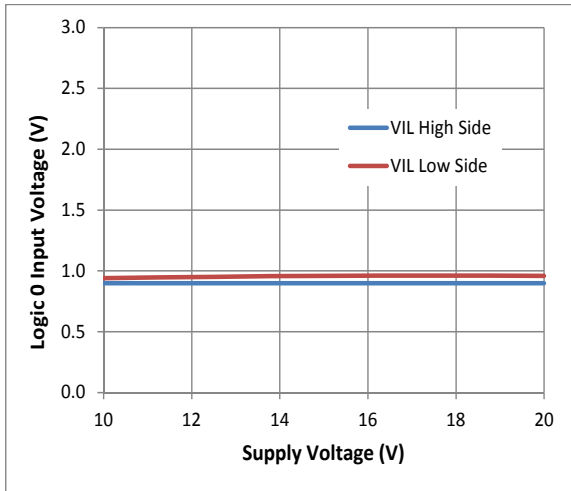
Typical Characteristics, cont'd

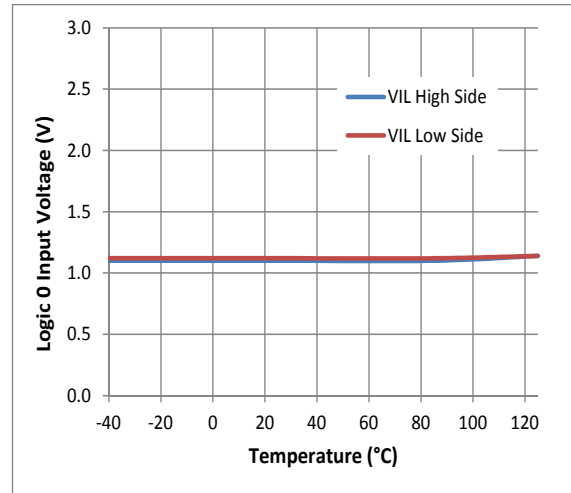**Figure 23.** Logic 0 Input Voltage vs. Supply Voltage

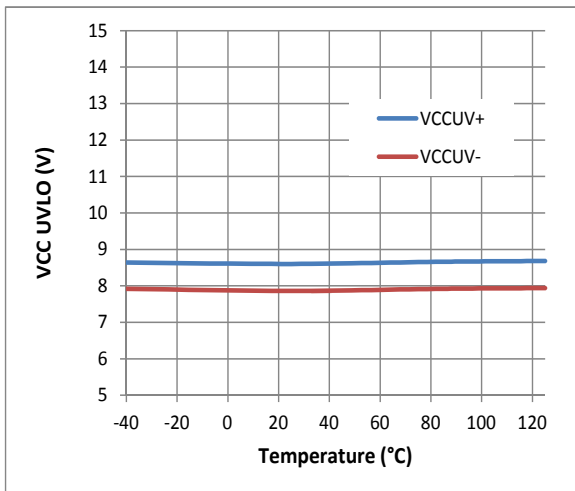**Figure 24.** Logic 0 Input Voltage vs. Temperature
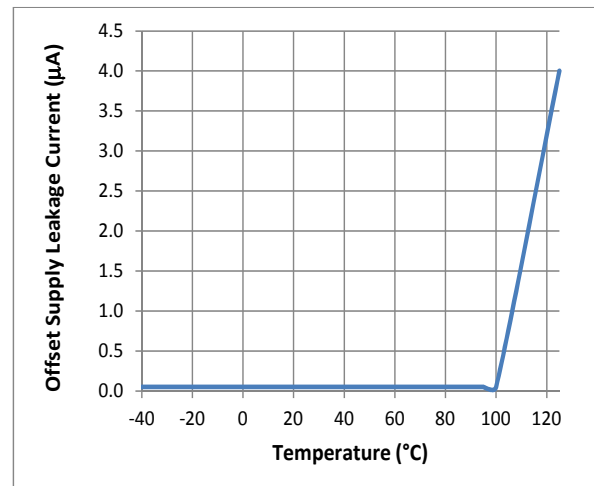
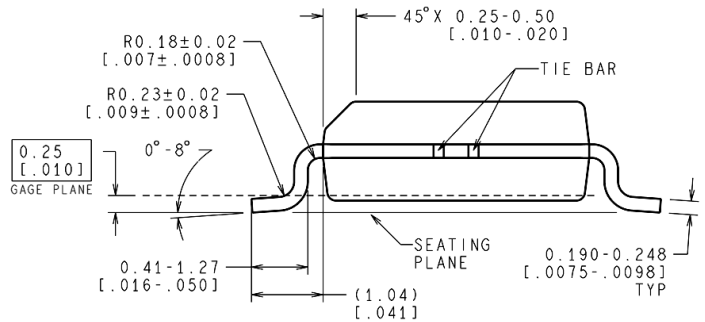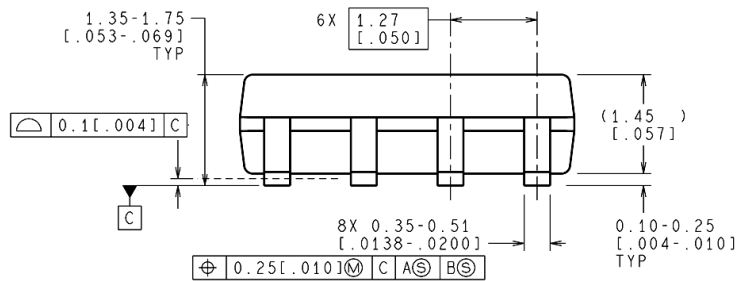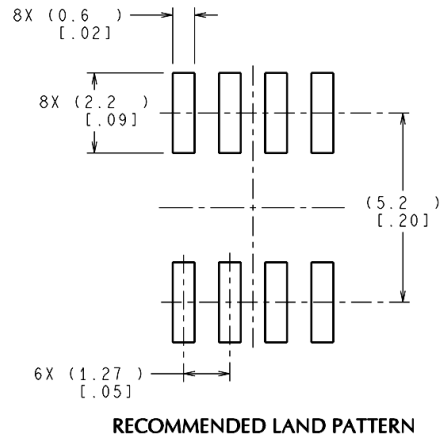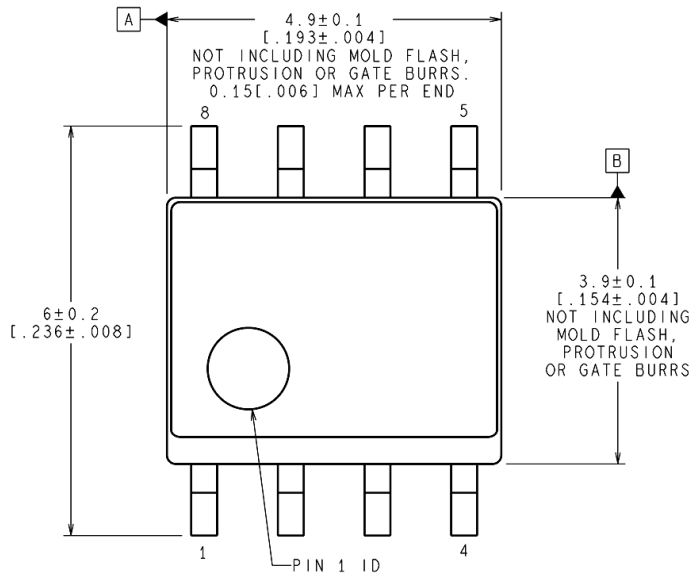**Figure 25.** V$_{CC}$ UVLO vs. Temperature

Figure 26. Offset Supply Leakage Current Temperature

Package Dimensions (SOIC-8 N)

Please contact support@tfsemiconductors.com for package availability.

A
4.9±0.1
[.193±.004]
NOT INCLUDING MOLD FLASH,
PROTRUSION OR GATE BURRS.
0.15[.006] MAX PER END
8   5
B
3.9±0.1
[.154±.004]
NOT INCLUDING
MOLD FLASH,
PROTRUSION
OR GATE BURRS
6±0.2
[.236±.008]
1   4
PIN 1 ID

8X (0.6)
[.02]
8X (2.2)
[.09]
(5.2)
[.20]
6X (1.27)
[.05]

RECOMMENDED LAND PATTERN

1.35-1.75
[.053-.069]
TYP
6X 1.27
[.050]
0.1[.004] C
C
(1.45)
[.057]
8X 0.35-0.51
[.0138-.0200]
0.10-0.25
[.004-.010]
TYP
0.25[.010] M C A S B S

R0.18±0.02
[.007±.0008]
R0.23±0.02
[.009±.0008]
45°X 0.25-0.50
[.010-.020]
TIE BAR
0.25
[.010]
GAGE PLANE
0°-8°
SEATING PLANE
0.41-1.27
[.016-.050]
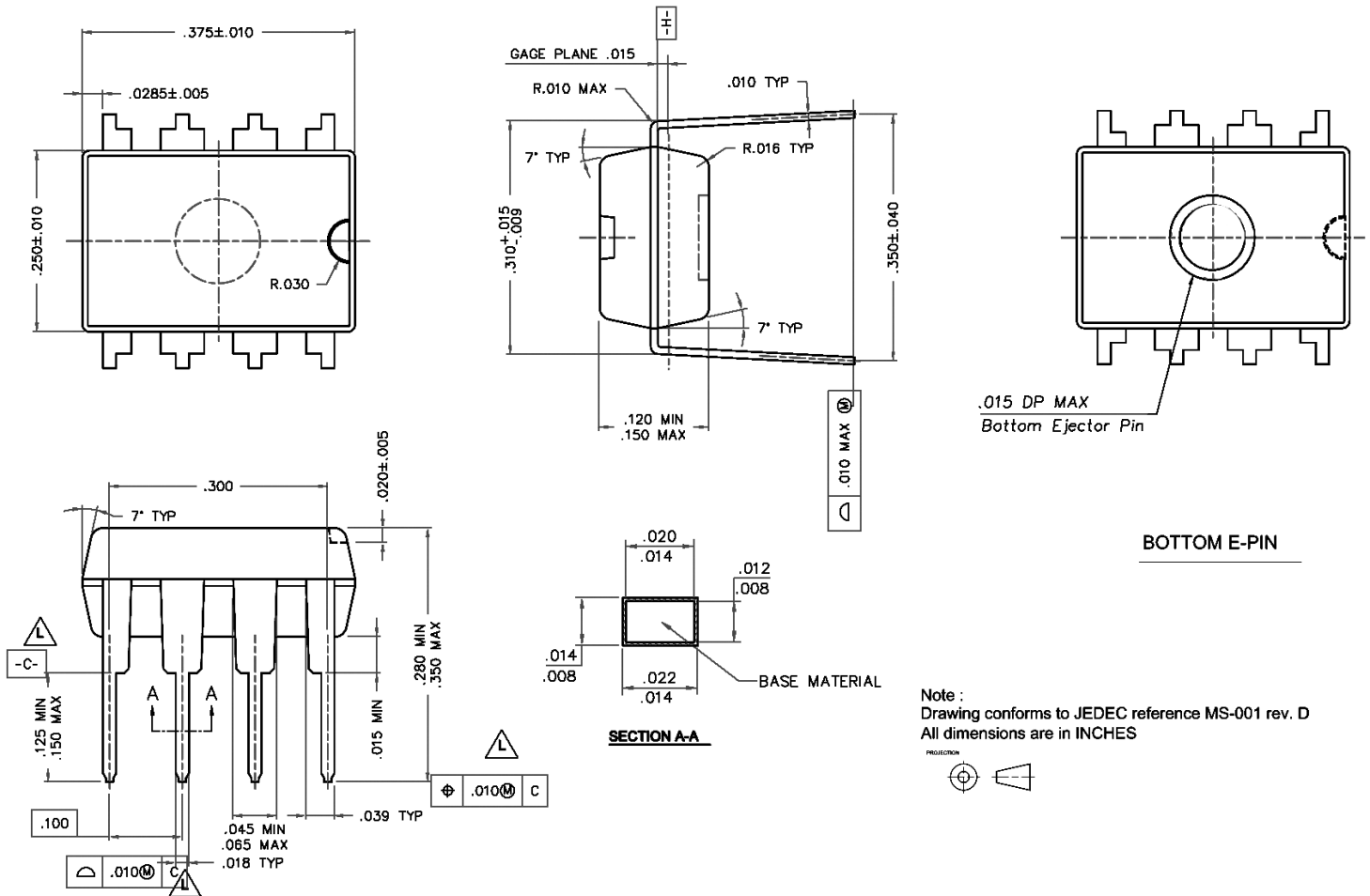(1.04)
[.041]
0.190-0.248
[.0075-.0098]
TYP

NOTES: UNLESS OTHERWISE SPECIFIED
1. REFERENCE JEDEC REGISTRATION MS-012, VARIATION AA.

CONTROLLING DIMENSION IS MILLIMETER
VALUES IN [ ] ARE INCHES
DIMENSIONS IN ( ) FOR REFERENCE ONLY

Package Dimensions (PDIP-8)

.375±.010

.0285±.005

.250±.010

R.030

GAGE PLANE .015

R.010 MAX

7° TYP

R.016 TYP

.010 TYP

.310 +.015 -.009

.350±.040

7° TYP

.120 MIN
.150 MAX

.010 MAX

.300

7° TYP

.020±.005

-C-

.125 MIN
.150 MAX

A   A

.280 MIN
.350 MAX

.015 MIN

.100

.045 MIN
.065 MAX
.018 TYP

.039 TYP

⊕ | .010 M | C

△ | .010 M | C

.020
.014

.012
.008

.014
.008

.022
.014

BASE MATERIAL

SECTION A-A

.015 DP MAX
Bottom Ejector Pin

BOTTOM E-PIN

Note :
Drawing conforms to JEDEC reference MS-001 rev. D
All dimensions are in INCHES

PROJECTION

Revision History

Rev.	Change	Owner	Date
1.0	First release	Keith Spaulding	4/20/2017
1.1	Add Note 5	Duke Walton	7/28/2019
1.2	Add Application Information	Keith Spaulding	10/10/2020
1.3	Application notes update	Raj Selvaraj	06/28/2021

Important Notice

For additional information please contact support@tfsemi.com or visit www.tfsemi.com