# 8 O/P 1.5V PCIe Gen1-2-3 ZDB/FOB w/Zo=100ohms

# 9DBU0841

**DATASHEET**

## Description

The 9DBU0841 is a member of IDT's 1.5V Ultra-Low-Power (ULP) PCIe family. It has integrated output terminations providing Zo=100Ω for direct connection to 100Ω transmission lines. The device has 8 output enables for clock management and 3 selectable SMBus addresses.

## Recommended Application

1.5V PCIe Gen1-2-3 Zero Delay/Fanout Buffer (ZDB/FOB)

## Output Features

- 8 – 1-167MHz Low-Power (LP) HCSL DIF pairs w/ZO=100Ω

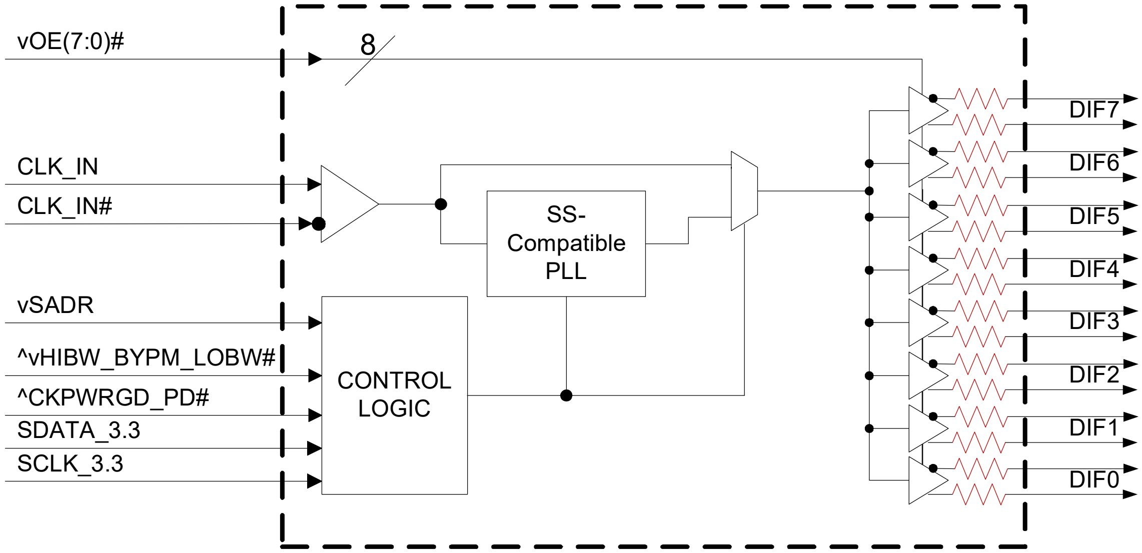
## Key Specifications

- DIF cycle-to-cycle jitter <50ps
- DIF output-to-output skew < 80ps
- DIF phase jitter is PCIe Gen1-2-3 compliant
- Very low additive phase jitter in bypass mode

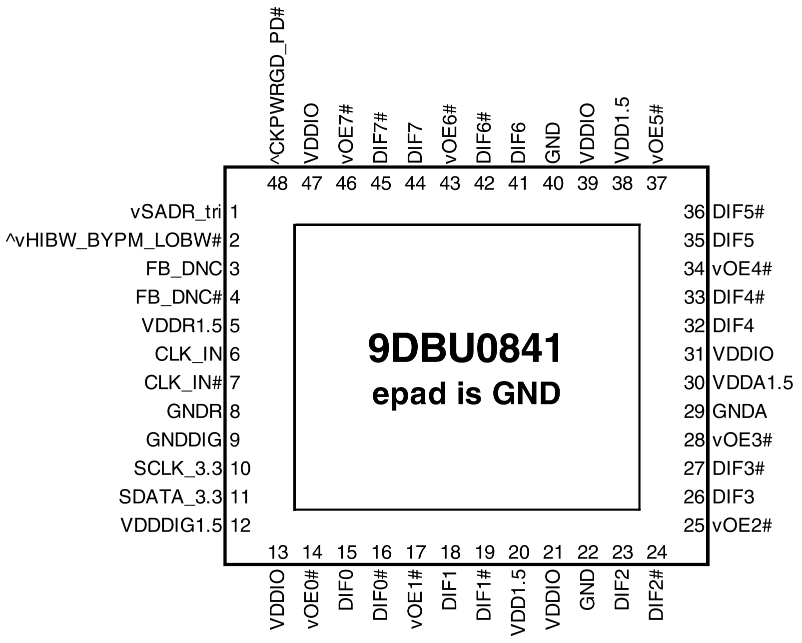
## Features/Benefits

- Direct connection to 100Ω transmission lines; saves 32 resistors compared to standard HCSL outputs
- 53mW typical power consumption in PLL mode; eliminates thermal concerns
- Outputs can optionally be supplied from any voltage between 1.05 and 1.5V; maximum power savings
- Spread Spectrum (SS) compatible; allows SS for EMI reduction
- OE# pins; support DIF power management
- HCSL-compatible differential input; can be driven by common clock sources
- Spread Spectrum tolerant; allows reduction of EMI
- SMBus-selectable features; optimize signal integrity to application
  - slew rate for each output
  - differential output amplitude
- Pin/SMBus selectable PLL bandwidth and PLL Bypass; optimize PLL to application
- Outputs blocked until PLL is locked; clean system start-up
- Device contains default configuration; SMBus interface not required for device control
- Three selectable SMBus addresses; multiple devices can easily share an SMBus segment
- 3.3V tolerant SMBus interface works with legacy controllers
- Space saving 48-pin 6x6mm VFQFPN; minimal board space

## Block Diagram



# Pin Configuration



**48-pin VFQFPN, 6x6 mm, 0.4mm pitch**

^v prefix indicates internal 120KOhm pull up *AND pull* down resistor (biased to VDD/2)
v prefix indicates internal 120KOhm pull down resistor
^ prefix indicates internal 120KOhm pull up resistor

## SMBus Address Selection Table

| | SADR | Address | + Read/Write bit |
|---|---|---|---|
| State of SADR on first application of CKPWRGD_PD# | 0 | 1101011 | x |
| | M | 1101100 | x |
| | 1 | 1101101 | x |

## Power Management Table

| CKPWRGD_PD# | CLK_IN | SMBus OEx bit | OEx# Pin | DIFx | | PLL |
|---|---|---|---|---|---|---|
| | | | | True O/P | Comp. O/P | |
| 0 | X | X | X | Low | Low | Off |
| 1 | Running | 0 | X | Low | Low | On[1] |
| 1 | Running | 1 | 0 | Running | Running | On[1] |
| 1 | Running | 1 | 1 | Low | Low | On[1] |

1. If Bypass mode is selected, the PLL will be off, and outputs will be running.

## Power Connections

| Pin Number | | | Description |
|---|---|---|---|
| VDD | VDDIO | GND | |
| 5 | | 8 | Input receiver analog |
| 12 | | 9 | Digital Power |
| 20, 31, 38 | 13, 21, 31, 39, 47 | 22, 29, 40 | DIF outputs |
| 30 | | 29 | PLL Analog |

Note: epad on this device is not electrically connected to the die.
It should be connected to ground for best thermal performance.

## PLL Operating Mode

| HiBW_BypM_LoBW# | MODE | Byte1 [7:6] Readback | Byte1 [4:3] Control |
|---|---|---|---|
| 0 | PLL Lo BW | 00 | 00 |
| M | Bypass | 01 | 01 |
| 1 | PLL Hi BW | 11 | 11 |

## Pin Descriptions

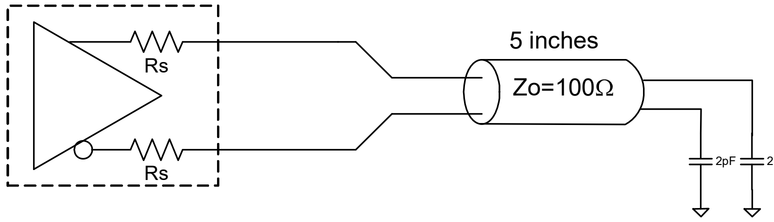
| PIN # | PIN NAME | TYPE | DESCRIPTION |
|---|---|---|---|
| 1 | vSADR_tri | LATCHED IN | Tri-level latch to select SMBus Address. See SMBus Address Selection Table. |
| 2 | ^vHIBW_BYPM_LOBW# | LATCHED IN | Trilevel input to select High BW, Bypass or Low BW mode.<br>See PLL Operating Mode Table for Details. |
| 3 | FB_DNC | DNC | True clock of differential feedback. The feedback output and feedback input are connected internally on this pin. Do not connect anything to this pin. |
| 4 | FB_DNC# | DNC | Complement clock of differential feedback. The feedback output and feedback input are connected internally on this pin. Do not connect anything to this pin. |
| 5 | VDDR1.5 | PWR | 1.5V power for differential input clock (receiver). This VDD should be treated as an Analog power rail and filtered appropriately. |
| 6 | CLK_IN | IN | True Input for differential reference clock. |
| 7 | CLK_IN# | IN | Complementary Input for differential reference clock. |
| 8 | GNDR | GND | Analog Ground pin for the differential input (receiver) |
| 9 | GNDDIG | GND | Ground pin for digital circuitry |
| 10 | SCLK_3.3 | IN | Clock pin of SMBus circuitry, 3.3V tolerant. |
| 11 | SDATA_3.3 | I/O | Data pin for SMBus circuitry, 3.3V tolerant. |
| 12 | VDDDIG1.5 | PWR | 1.5V digital power (dirty power) |
| 13 | VDDIO | PWR | Power supply for differential outputs |
| 14 | vOE0# | IN | Active low input for enabling DIF pair 0. This pin has an internal pull-down.<br>1 =disable outputs, 0 = enable outputs |
| 15 | DIF0 | OUT | Differential true clock output |
| 16 | DIF0# | OUT | Differential Complementary clock output |
| 17 | vOE1# | IN | Active low input for enabling DIF pair 1. This pin has an internal pull-down.<br>1 =disable outputs, 0 = enable outputs |
| 18 | DIF1 | OUT | Differential true clock output |
| 19 | DIF1# | OUT | Differential Complementary clock output |
| 20 | VDD1.5 | PWR | Power supply, nominally 1.5V |
| 21 | VDDIO | PWR | Power supply for differential outputs |
| 22 | GND | GND | Ground pin. |
| 23 | DIF2 | OUT | Differential true clock output |
| 24 | DIF2# | OUT | Differential Complementary clock output |
| 25 | vOE2# | IN | Active low input for enabling DIF pair 2. This pin has an internal pull-down.<br>1 =disable outputs, 0 = enable outputs |
| 26 | DIF3 | OUT | Differential true clock output |
| 27 | DIF3# | OUT | Differential Complementary clock output |
| 28 | vOE3# | IN | Active low input for enabling DIF pair 3. This pin has an internal pull-down.<br>1 =disable outputs, 0 = enable outputs |
| 29 | GNDA | GND | Ground pin for the PLL core. |
| 30 | VDDA1.5 | PWR | 1.5V power for the PLL core. |
| 31 | VDDIO | PWR | Power supply for differential outputs |
| 32 | DIF4 | OUT | Differential true clock output |
| 33 | DIF4# | OUT | Differential Complementary clock output |
| 34 | vOE4# | IN | Active low input for enabling DIF pair 4. This pin has an internal pull-down.<br>1 =disable outputs, 0 = enable outputs |
| 35 | DIF5 | OUT | Differential true clock output |
| 36 | DIF5# | OUT | Differential Complementary clock output |
| 37 | vOE5# | IN | Active low input for enabling DIF pair 5. This pin has an internal pull-down.<br>1 =disable outputs, 0 = enable outputs |
| 38 | VDD1.5 | PWR | Power supply, nominally 1.5V |
| 39 | VDDIO | PWR | Power supply for differential outputs |
| 40 | GND | GND | Ground pin. |

## Pin Descriptions (cont.)

| PIN # | PIN NAME | TYPE | DESCRIPTION |
|---|---|---|---|
| 41 | DIF6 | OUT | Differential true clock output |
| 42 | DIF6# | OUT | Differential Complementary clock output |
| 43 | vOE6# | IN | Active low input for enabling DIF pair 6. This pin has an internal pull-down.<br>1 =disable outputs, 0 = enable outputs |
| 44 | DIF7 | OUT | Differential true clock output |
| 45 | DIF7# | OUT | Differential Complementary clock output |
| 46 | vOE7# | IN | Active low input for enabling DIF pair 7. This pin has an internal pull-down.<br>1 =disable outputs, 0 = enable outputs |
| 47 | VDDIO | PWR | Power supply for differential outputs |
| 48 | ^CKPWRGD_PD# | IN | Input notifies device to sample latched inputs and start up on first high assertion. Low enters Power Down Mode, subsequent high assertions exit Power Down Mode. This pin has internal pull-up resistor. |
| 49 | EPAD | GND | Connect ePAD to ground. |

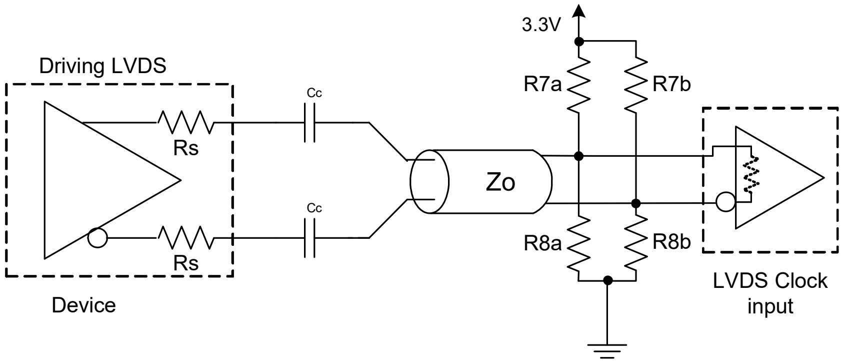
## Test Loads

Low-Power HCSL Differential Output Test Load



Note: The device can drive transmission line lengths greater than those allowed by the PCIe SIG

## Driving LVDS



**Driving LVDS inputs**

|  | Value |  |  |
|---|---|---|---|
| Component | Receiver has termination | Receiver does not have termination | Note |
| R7a, R7b | 10K ohm | 140 ohm |  |
| R8a, R8b | 5.6K ohm | 75 ohm |  |
| Cc | 0.1 uF | 0.1 uF |  |
| Vcm | 1.2 volts | 1.2 volts |  |

## Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the 9DBU0841. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|---|
| Supply Voltage | VDDx | | -0.5 | | 2 | V | 1,2 |
| Input Voltage | $V_{IN}$ | | -0.5 | | $V_{DD}$+0.5 | V | 1,3 |
| Input High Voltage, SMBus | $V_{IHSMB}$ | SMBus clock and data pins | | | 3.3 | V | 1 |
| Storage Temperature | Ts | | -65 | | 150 | °C | 1 |
| Junction Temperature | Tj | | | | 125 | °C | 1 |
| Input ESD protection | ESD prot | Human Body Model | 2000 | | | V | 1 |

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Operation under these conditions is neither implied nor guaranteed.

[3] Not to exceed 2.0V.

## Electrical Characteristics–Clock Input Parameters

TA = $T_{AMB,}$ Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|---|
| Input Common Mode Voltage - DIF_IN | $V_{COM}$ | Common Mode Input Voltage | 200 | | 725 | mV | 1 |
| Input Swing - DIF_IN | $V_{SWING}$ | Differential value | 300 | | 1450 | mV | 1 |
| Input Slew Rate - DIF_IN | dv/dt | Measured differentially | 0.4 | | 8 | V/ns | 1,2 |
| Input Leakage Current | $I_{IN}$ | $V_{IN} = V_{DD}$ , $V_{IN}$ = GND | -5 | | 5 | uA | |
| Input Duty Cycle | $d_{tin}$ | Measurement from differential wavefrom | 45 | 50 | 55 | % | 1 |
| Input Jitter - Cycle to Cycle | $J_{DIFIn}$ | Differential Measurement | 0 | | 150 | ps | 1 |

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Slew rate measured through +/-75mV window centered around differential zero

# Electrical Characteristics–Input/Supply/Common Parameters–Normal Operating Conditions

TA = $T_{AMB,}$ Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|---|
| Supply Voltage | VDDx | Supply voltage for core and analog | 1.425 | 1.5 | 1.575 | V | |
| Output Supply Voltage | VDDIO | Supply voltage for Low Power HCSL Outputs | 0.95 | 1.05-1.5 | 1.575 | V | |
| Ambient Operating Temperature | $T_{AMB}$ | Commmercial range | 0 | 25 | 70 | °C | 1 |
| | | Industrial range | -40 | 25 | 85 | °C | 1 |
| Input High Voltage | $V_{IH}$ | Single-ended inputs, except SMBus | 0.75 $V_{DD}$ | | $V_{DD}$ + 0.3 | V | |
| Input Mid Voltage | $V_{IM}$ | Single-ended tri-level inputs ('_tri' suffix) | 0.4 $V_{DD}$ | | 0.6 $V_{DD}$ | V | |
| Input Low Voltage | $V_{IL}$ | Single-ended inputs, except SMBus | -0.3 | | 0.25 $V_{DD}$ | V | |
| Input Current | $I_{IN}$ | Single-ended inputs, $V_{IN}$ = GND, $V_{IN}$ = VDD | -5 | | 5 | uA | |
| | $I_{INP}$ | Single-ended inputs<br>$V_{IN}$ = 0 V; Inputs with internal pull-up resistors<br>$V_{IN}$ = VDD; Inputs with internal pull-down resistors | -200 | | 200 | uA | |
| Input Frequency | $F_{ibyp}$ | Bypass mode | 1 | | 167 | MHz | 2 |
| | $F_{ipll}$ | 100MHz PLL mode | 20 | 100.00 | 110 | MHz | 2 |
| Pin Inductance | $L_{pin}$ | | | | 7 | nH | 1 |
| Capacitance | $C_{IN}$ | Logic Inputs, except DIF_IN | 1.5 | | 5 | pF | 1 |
| | $C_{INDIF\_IN}$ | DIF_IN differential clock inputs | 1.5 | | 2.7 | pF | 1,5 |
| | $C_{OUT}$ | Output pin capacitance | | | 6 | pF | 1 |
| Clk Stabilization | $T_{STAB}$ | From $V_{DD}$ Power-Up and after input clock stabilization or de-assertion of PD# to 1st clock | | | 1 | ms | 1,2 |
| Input SS Modulation Frequency PCIe | $f_{MODINPCIe}$ | Allowable Frequency for PCIe Applications (Triangular Modulation) | 30 | | 33 | kHz | |
| Input SS Modulation Frequency non-PCIe | $f_{MODIN}$ | Allowable Frequency for non-PCIe Applications (Triangular Modulation) | 0 | | 66 | kHz | |
| OE# Latency | $t_{LATOE\#}$ | DIF start after OE# assertion<br>DIF stop after OE# deassertion | 1 | | 3 | clocks | 1,3 |
| Tdrive_PD# | $t_{DRVPD}$ | DIF output enable after PD# de-assertion | | | 300 | us | 1,3 |
| Tfall | $t_F$ | Fall time of single-ended control inputs | | | 5 | ns | 2 |
| Trise | $t_R$ | Rise time of single-ended control inputs | | | 5 | ns | 2 |
| SMBus Input Low Voltage | $V_{ILSMB}$ | | | | 0.6 | V | |
| SMBus Input High Voltage | $V_{IHSMB}$ | $V_{DDSMB}$ = 3.3V, see note 4 for $V_{DDSMB}$ < 3.3V | 2.1 | | 3.3 | V | 4 |
| SMBus Output Low Voltage | $V_{OLSMB}$ | @ $I_{PULLUP}$ | | | 0.4 | V | |
| SMBus Sink Current | $I_{PULLUP}$ | @ $V_{OL}$ | 4 | | | mA | |
| Nominal Bus Voltage | $V_{DDSMB}$ | Bus Voltage | 1.425 | | 3.3 | V | |
| SCLK/SDATA Rise Time | $t_{RSMB}$ | (Max VIL - 0.15) to (Min VIH + 0.15) | | | 1000 | ns | 1 |
| SCLK/SDATA Fall Time | $t_{FSMB}$ | (Min VIH + 0.15) to (Max VIL - 0.15) | | | 300 | ns | 1 |
| SMBus Operating Frequency | $f_{MAXSMB}$ | Maximum SMBus operating frequency | | | 400 | kHz | 6 |

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Control input must be monotonic from 20% to 80% of input swing.

[3] Time from deassertion until outputs are >200 mV

[4] For $V_{DDSMB}$ < 3.3V, $V_{IHSMB}$ >= $0.8xV_{DDSMB}$

[5] DIF_IN input

[6] The differential input clock must be running for the SMBus to be active

## Electrical Characteristics–DIF Low-Power HCSL Outputs

TA = $T_{AMB,}$ Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|---|
| Slew rate | dV/dt | Scope averaging on, fast setting | 1 | 2.4 | 3.5 | V/ns | 1,2,3 |
| | dV/dt | Scope averaging on, slow setting | 0.7 | 1.7 | 2.5 | V/ns | 1,2,3 |
| Slew rate matching | ΔdV/dt | Slew rate matching, Scope averaging on | | 9 | 20 | % | 1,2,4 |
| Voltage High | $V_{HIGH}$ | Statistical measurement on single-ended signal using oscilloscope math function. (Scope averaging on) | 630 | 750 | 850 | mV | 7 |
| Voltage Low | $V_{LOW}$ | | -150 | 26 | 150 | | 7 |
| Max Voltage | Vmax | Measurement on single ended signal using absolute value. (Scope averaging off) | | 763 | 1150 | mV | 7 |
| Min Voltage | Vmin | | -300 | 22 | | | 7 |
| Vswing | Vswing | Scope averaging off | 300 | 1448 | | mV | 1,2 |
| Crossing Voltage (abs) | Vcross_abs | Scope averaging off | 250 | 390 | 550 | mV | 1,5 |
| Crossing Voltage (var) | Δ-Vcross | Scope averaging off | | 11 | 140 | mV | 1,6 |

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Measured from differential waveform

[3] Slew rate is measured through the Vswing voltage range centered around differential 0V. This results in a +/-150mV window around differential 0V.

[4] Matching applies to rising edge rate for Clock and falling edge rate for Clock#. It is measured using a +/-75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations.

[5] Vcross is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).

[6] The total variation of all Vcross measurements in any particular system. Note that this is a subset of Vcross_min/max (Vcross absolute) allowed. The intent is to limit Vcross induced modulation by setting Δ-Vcross to be smaller than Vcross absolute.

[7] At default SMBus settings.

## Electrical Characteristics–Current Consumption

TA = $T_{AMB,}$ Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|---|
| Operating Supply Current | $I_{DDA}$ | VDDA+VDDR, PLL Mode, @100MHz | | 11 | 15 | mA | |
| | $I_{DD}$ | VDD, All outputs active @100MHz | | 6 | 9 | mA | |
| | $I_{DDIO}$ | VDDIO, All outputs active @100MHz | | 28 | 35 | mA | |
| Powerdown Current | $I_{DDAPD}$ | VDDA+VDDR, CKPWRGD_PD#=0 | | 0.5 | 1 | mA | 2 |
| | $I_{DDPD}$ | VDDx, CKPWRGD_PD#=0 | | 0.6 | 1 | mA | 2 |
| | $I_{DDIOPD}$ | VDDIO, CKPWRGD_PD#=0 | | 0.003 | 0.01 | mA | 2 |

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Input clock stopped.

# Electrical Characteristics–Output Duty Cycle, Jitter, Skew and PLL Characteristics

TA = $T_{AMB,}$ Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|---|
| PLL Bandwidth | BW | -3dB point in High BW Mode (100MHz) | 2.3 | 3.6 | 4.7 | MHz | 1,5 |
| | | -3dB point in Low BW Mode (100MHz) | 1 | 1.6 | 2.5 | MHz | 1,5 |
| PLL Jitter Peaking | $t_{JPEAK}$ | Peak Pass band Gain (100MHz) | | 1.3 | 2.5 | dB | 1 |
| Duty Cycle | $t_{DC}$ | Measured differentially, PLL Mode | 45 | 50 | 55 | % | 1 |
| Duty Cycle Distortion | $t_{DCD}$ | Measured differentially, Bypass Mode | -1 | -0.6 | 0 | % | 1,3 |
| Skew, Input to Output | $t_{pdBYP}$ | Bypass Mode, $V_T$ = 50% | 3400 | 4301 | 5200 | ps | 1 |
| | $t_{pdPLL}$ | PLL Mode $V_T$ = 50% | 0 | 50 | 150 | ps | 1,4 |
| Skew, Output to Output | $t_{sk3}$ | $V_T$ = 50% | | 37 | 75 | ps | 1,4 |
| Jitter, Cycle to cycle | $t_{jcyc\text{-}cyc}$ | PLL mode | | 24 | 50 | ps | 1,2 |
| | | *Additive* Jitter in Bypass Mode | | 0.1 | 10 | ps | 1,2 |

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Measured from differential waveform

[3] Duty cycle distortion is the difference in duty cycle between the output and the input clock when the device is operated in bypass mode.

[4] All outputs at default slew rate

[5] The MIN/TYP/MAX values of each BW setting track each other, i.e., Low BW MAX will never occur with Hi BW MIN.

# Electrical Characteristics–Phase Jitter Parameters

TA = $T_{AMB,}$ Supply Voltages per normal operation conditions, See Test Loads for Loading Conditions

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | INDUSTRY LIMIT | UNITS | Notes |
|---|---|---|---|---|---|---|---|---|
| Phase Jitter, PLL Mode | $t_{jphPCIeG1}$ | PCIe Gen 1 | | 30 | 58 | 86 | ps (p-p) | 1,2,3,5 |
| | $t_{jphPCIeG2}$ | PCIe Gen 2 Lo Band<br>10kHz < f < 1.5MHz | | 0.9 | 1.4 | 3 | ps (rms) | 1,2,3,5 |
| | | PCIe Gen 2 High Band<br>1.5MHz < f < Nyquist (50MHz) | | 2.1 | 2.6 | 3.1 | ps (rms) | 1,2,3,5 |
| | $t_{jphPCIeG3}$ | PCIe Gen 3 Common Clock Architecture<br>(PLL BW of 2-4 or 2-5MHz, CDR = 10MHz) | | 0.5 | 0.6 | 1 | ps (rms) | 1,2,3,5 |
| | $t_{jphPCIeG3SRnS}$ | PCIe Gen 3 Separate Reference No Spread (SRnS)<br>(PLL BW of 2-4 or 2-5MHz, CDR = 10MHz) | | 0.5 | 0.6 | 0.7 | ps (rms) | 1,2,3,5 |
| Additive Phase Jitter, Bypass Mode | $t_{jphPCIeG1}$ | PCIe Gen 1 | | 0.1 | 5 | N/A | ps (p-p) | 1,2,3,5 |
| | $t_{jphPCIeG2}$ | PCIe Gen 2 Lo Band<br>10kHz < f < 1.5MHz | | 0.1 | 0.5 | N/A | ps (rms) | 1,2,3,4,5 |
| | | PCIe Gen 2 High Band<br>1.5MHz < f < Nyquist (50MHz) | | 0.1 | 0.7 | N/A | ps (rms) | 1,2,3,4 |
| | $t_{jphPCIeG3}$ | PCIe Gen 3<br>(PLL BW of 2-4 or 2-5MHz, CDR = 10MHz) | | 0.2 | 0.3 | N/A | ps (rms) | 1,2,3,4 |
| | $t_{jph125M0}$ | 125MHz, 1.5MHz to 10MHz, -20dB/decade rollover < 1.5MHz, -40db/decade rolloff > 10MHz | | 200 | 250 | N/A | fs (rms) | 1,6 |
| | $t_{jph125M1}$ | 125MHz, 12KHz to 20MHz, -20dB/decade rollover < 1.5MHz, -40db/decade rolloff > 10MHz | | 313 | 350 | N/A | fs (rms) | 1,6 |

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] See http://www.pcisig.com for complete specs

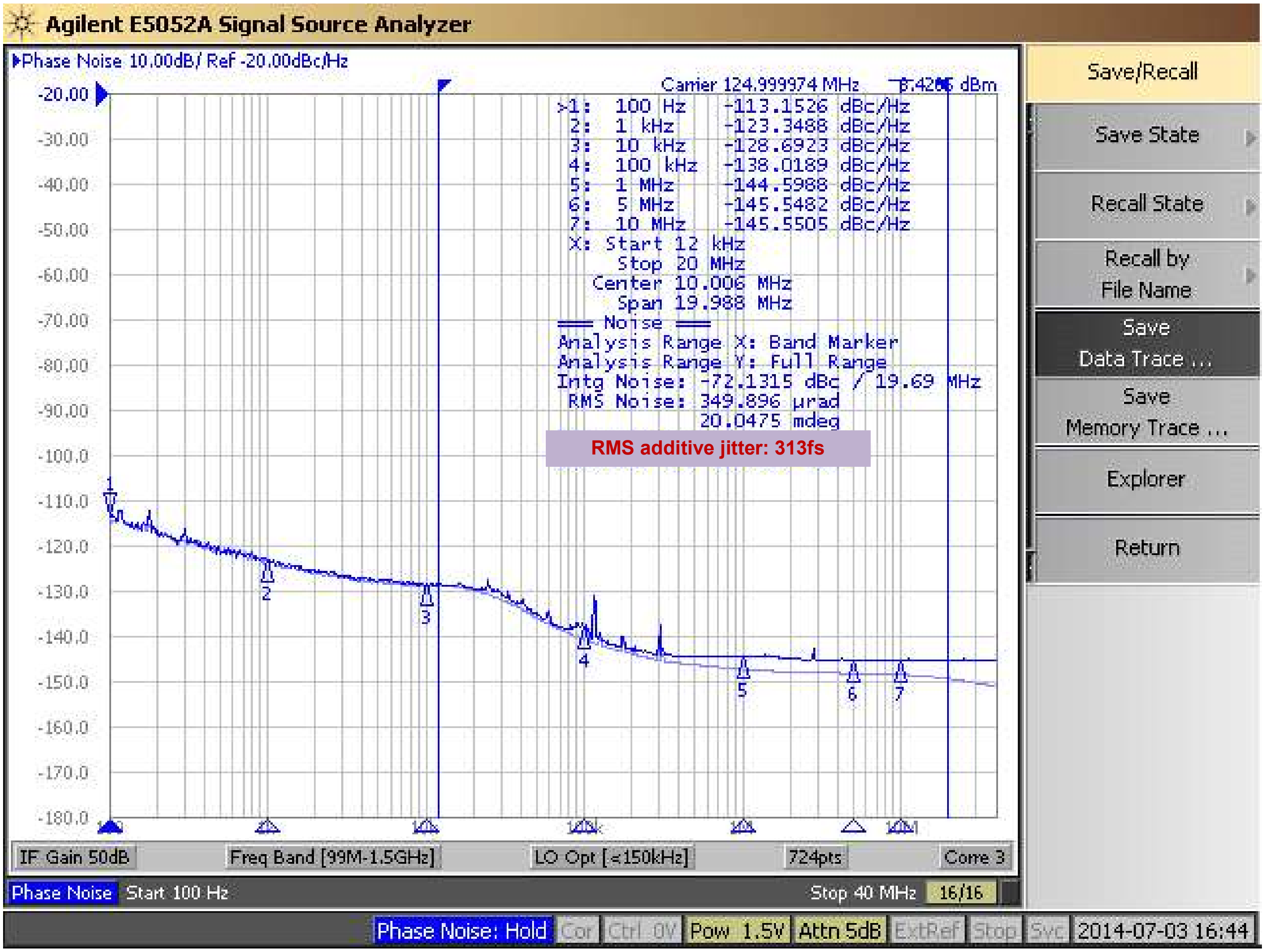
[3] Sample size of at least 100K cycles. This figures extrapolates to 108ps pk-pk @ 1M cycles for a BER of 1-12.

[4] For RMS figures, additive jitter is calculated by solving the following equation: Additive jitter = SQRT[(total jitter)^2 - (input jitter)^2]

[5] Driven by 9FGU0831 or equivalent

[6] Rohde&Schartz SMA100

# Additive Phase Jitter Plot: 125M (12kHz to 20MHz)



```
Carrier 124.999974 MHz     8.4266 dBm
>1:  100 Hz     -113.1526 dBc/Hz
 2:  1 kHz      -123.3488 dBc/Hz
 3:  10 kHz     -128.6923 dBc/Hz
 4:  100 kHz    -138.0189 dBc/Hz
 5:  1 MHz      -144.5988 dBc/Hz
 6:  5 MHz      -145.5482 dBc/Hz
 7:  10 MHz     -145.5505 dBc/Hz
 X: Start 12 kHz
     Stop 20 MHz
   Center 10.006 MHz
     Span 19.988 MHz
 ═══ Noise ═══
Analysis Range X: Band Marker
Analysis Range Y: Full Range
Intg Noise: -72.1315 dBc / 19.69 MHz
 RMS Noise: 349.896 µrad
            20.0475 mdeg
```

RMS additive jitter: 313fs

# General SMBus Serial Interface Information

## How to Write

- Controller (host) sends a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) sends the byte count = X
- IDT clock will **acknowledge**
- Controller (host) starts sending Byte **N through Byte N+X-1**
- IDT clock will **acknowledg**e each byte **one at a time**
- Controller (host) sends a Stop bit

**Index Block Write Operation**

| Controller (Host) | | | IDT (Slave/Receiver) |
|---|---|---|---|
| T | starT bit | | |
| Slave Address | | | |
| WR | WRite | | |
| | | | ACK |
| Beginning Byte = N | | | |
| | | | ACK |
| Data Byte Count = X | | | |
| | | | ACK |
| Beginning Byte N | | X Byte | |
| | | | ACK |
| O | | | |
| O | | | O |
| O | | | O |
| | | | O |
| Byte N + X - 1 | | | |
| | | | ACK |
| P | stoP bit | | |

**Note: SMBus Address is Latched on SADR pin.**

## How to Read

- Controller (host) will send a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) will send a separate start bit
- Controller (host) sends the read address
- IDT clock will **acknowledge**
- IDT clock will send the data byte count = X
- IDT clock sends Byte **N+X-1**
- IDT clock sends **Byte 0 through Byte X (if $X_{(H)}$ was written to Byte 8)**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

**Index Block Read Operation**

| Controller (Host) | | | IDT (Slave/Receiver) |
|---|---|---|---|
| T | starT bit | | |
| Slave Address | | | |
| WR | WRite | | |
| | | | ACK |
| Beginning Byte = N | | | |
| | | | ACK |
| RT | Repeat starT | | |
| Slave Address | | | |
| RD | ReaD | | |
| | | | ACK |
| | | | |
| | | | Data Byte Count=X |
| ACK | | | |
| | | X Byte | Beginning Byte N |
| ACK | | | |
| | | | O |
| O | | | O |
| O | | | O |
| O | | | |
| | | | Byte N + X - 1 |
| N | Not acknowledge | | |
| P | stoP bit | | |

**SMBus Table: Output Enable Register** [1]

| Byte 0 | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|
| **Bit 7** | DIF OE7 | Output Enable | RW | Low/Low | Enabled | 1 |
| **Bit 6** | DIF OE6 | Output Enable | RW | Low/Low | Enabled | 1 |
| **Bit 5** | DIF OE5 | Output Enable | RW | Low/Low | Enabled | 1 |
| **Bit 4** | DIF OE4 | Output Enable | RW | Low/Low | Enabled | 1 |
| **Bit 3** | DIF OE3 | Output Enable | RW | Low/Low | Enabled | 1 |
| **Bit 2** | DIF OE2 | Output Enable | RW | Low/Low | Enabled | 1 |
| **Bit 1** | DIF OE1 | Output Enable | RW | Low/Low | Enabled | 1 |
| **Bit 0** | DIF OE0 | Output Enable | RW | Low/Low | Enabled | 1 |

1. A low on these bits will overide the OE# pin and force the differential output Low/Low

**SMBus Table: PLL Operating Mode and Output Amplitude Control Register**

| Byte 1 | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|
| **Bit 7** | PLLMODERB1 | PLL Mode Readback Bit 1 | **R** | See PLL Operating Mode Table | | Latch |
| **Bit 6** | PLLMODERB0 | PLL Mode Readback Bit 0 | **R** | | | Latch |
| **Bit 5** | PLLMODE_SWCNTRL | Enable SW control of PLL Mode | RW | Values in B1[7:6] set PLL Mode | Values in B1[4:3] set PLL Mode | 0 |
| **Bit 4** | PLLMODE1 | PLL Mode Control Bit 1 | RW[1] | See PLL Operating Mode Table | | 0 |
| **Bit 3** | PLLMODE0 | PLL Mode Control Bit 0 | RW[1] | | | 0 |
| **Bit 2** | Reserved | | | | | 1 |
| **Bit 1** | AMPLITUDE 1 | Controls Output Amplitude | RW | 00 = 0.55V | 01= 0.65V | 1 |
| **Bit 0** | AMPLITUDE 0 | | RW | 10 = 0.7V | 11 = 0.8V | 0 |

1. B1[5] must be set to a 1 for these bits to have any effect on the part.

**SMBus Table: DIF Slew Rate Control Register**

| Byte 2 | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|
| **Bit 7** | SLEWRATESEL DIF7 | Adjust Slew Rate of DIF7 | RW | Slow Setting | Fast Setting | 1 |
| **Bit 6** | SLEWRATESEL DIF6 | Adjust Slew Rate of DIF6 | RW | Slow Setting | Fast Setting | 1 |
| **Bit 5** | SLEWRATESEL DIF5 | Adjust Slew Rate of DIF5 | RW | Slow Setting | Fast Setting | 1 |
| **Bit 4** | SLEWRATESEL DIF4 | Adjust Slew Rate of DIF4 | RW | Slow Setting | Fast Setting | 1 |
| **Bit 3** | SLEWRATESEL DIF3 | Adjust Slew Rate of DIF3 | RW | Slow Setting | Fast Setting | 1 |
| **Bit 2** | SLEWRATESEL DIF2 | Adjust Slew Rate of DIF2 | RW | Slow Setting | Fast Setting | 1 |
| **Bit 1** | SLEWRATESEL DIF1 | Adjust Slew Rate of DIF1 | RW | Slow Setting | Fast Setting | 1 |
| **Bit 0** | SLEWRATESEL DIF0 | Adjust Slew Rate of DIF0 | RW | Slow Setting | Fast Setting | 1 |

**Note: See "Low-Power HCSL Outputs" table for slew rates.**

**SMBus Table: Frequency Select Control Register**

| Byte 3 | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|
| **Bit 7** | Reserved | | | | | 1 |
| **Bit 6** | Reserved | | | | | 1 |
| **Bit 5** | Reserved | | | | | 0 |
| **Bit 4** | Reserved | | | | | 0 |
| **Bit 3** | Reserved | | | | | 0 |
| **Bit 2** | Reserved | | | | | 1 |
| **Bit 1** | Reserved | | | | | 1 |
| **Bit 0** | SLEWRATESEL FB | Adjust Slew Rate of FB | RW | Slow Setting | Fast Setting | 1 |

**Byte 4 is Reserved and reads back 'hFF**

**SMBus Table: Revision and Vendor ID Register**

| Byte 5 | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|
| **Bit 7** | RID3 | Revision ID | **R** | A rev = 0000 | | 0 |
| **Bit 6** | RID2 | | **R** | | | 0 |
| **Bit 5** | RID1 | | **R** | | | 0 |
| **Bit 4** | RID0 | | **R** | | | 0 |
| **Bit 3** | VID3 | VENDOR ID | **R** | 0001 = IDT | | 0 |
| **Bit 2** | VID2 | | **R** | | | 0 |
| **Bit 1** | VID1 | | **R** | | | 0 |
| **Bit 0** | VID0 | | **R** | | | 1 |

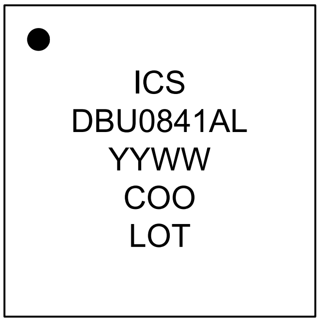
**SMBus Table: Device Type/Device ID**

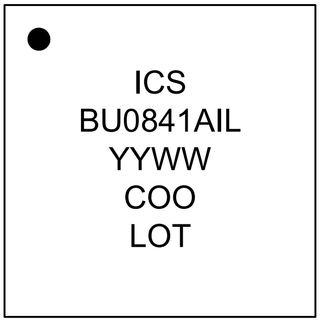
| Byte 6 | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|
| **Bit 7** | Device Type1 | Device Type | **R** | 00 = FGx, 01 = DBx ZDB/FOB, 10 = DMx, 11= DBx FOB | | 0 |
| **Bit 6** | Device Type0 | | **R** | | | 1 |
| **Bit 5** | Device ID5 | Device ID | **R** | 001000 binary or 08 hex | | 0 |
| **Bit 4** | Device ID4 | | **R** | | | 0 |
| **Bit 3** | Device ID3 | | **R** | | | 1 |
| **Bit 2** | Device ID2 | | **R** | | | 0 |
| **Bit 1** | Device ID1 | | **R** | | | 0 |
| **Bit 0** | Device ID0 | | **R** | | | 0 |

**SMBus Table: Byte Count Register**

| Byte 7 | Name | Control Function | Type | 0 | 1 | Default |
|---|---|---|---|---|---|---|
| **Bit 7** | Reserved | | | | | 0 |
| **Bit 6** | Reserved | | | | | 0 |
| **Bit 5** | Reserved | | | | | 0 |
| **Bit 4** | BC4 | Byte Count Programming | RW | Writing to this register will configure how many bytes will be read back, default is = 8 bytes. | | 0 |
| **Bit 3** | BC3 | | RW | | | 1 |
| **Bit 2** | BC2 | | RW | | | 0 |
| **Bit 1** | BC1 | | RW | | | 0 |
| **Bit 0** | BC0 | | RW | | | 0 |

## Marking Diagrams





Notes:
1. “LOT” is the lot sequence number.
2. “COO” denotes country of origin.
3. YYWW is the last two digits of the year and week that the part was assembled.
4. Line 2: truncated part number
5. “L” denotes RoHS compliant package.
6. “I” denotes industrial temperature range device.

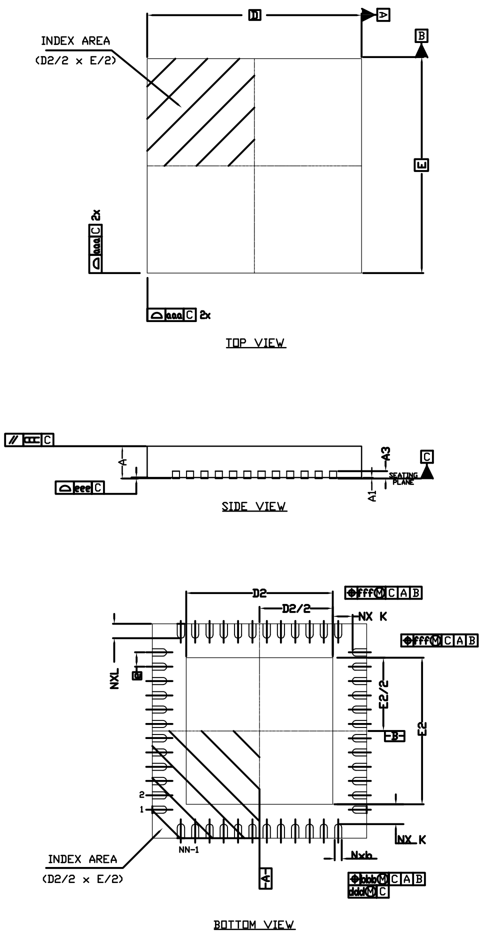
## Thermal Characteristics

| PARAMETER | SYMBOL | CONDITIONS | PKG | TYP VALUE | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Thermal Resistance | $\theta_{JC}$ | Junction to Case | NDG48 | 33 | °C/W | 1 |
| | $\theta_{Jb}$ | Junction to Base | | 2.1 | °C/W | 1 |
| | $\theta_{JA0\theta}$ | Junction to Air, still air | | 37 | °C/W | 1 |
| | $\theta_{JA1}$ | Junction to Air, 1 m/s air flow | | 30 | °C/W | 1 |
| | $\theta_{JA3}$ | Junction to Air, 3 m/s air flow | | 27 | °C/W | 1 |
| | $\theta_{JA5}$ | Junction to Air, 5 m/s air flow | | 26 | °C/W | 1 |

[1] ePad soldered to board

# Package Outline and Package Dimensions (NDG48) – use EPAD Option 1

| REVISIONS | | | |
|---|---|---|---|
| REV | DESCRIPTION | DATE | APPROVED |
| 00 | INITIAL RELEASE | 01/10/08 | DP |
| 01 | UPDATE EXPOSED PAD ADD TABLE | 08/05/10 | DP |
| 02 | COMBINE POD & LAND PATTERN | 10/29/13 | J.HUA |



OPTION 1:

| SYMBOL | DIMENSION | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| D2 | 3.95 | 4.10 | 4.20 |
| E2 | 3.95 | 4.10 | 4.20 |
| L | 0.30 | 0.40 | 0.50 |
| D | 6.00 BSC | | |
| E | 6.00 BSC | | |
| e | 0.40 BSC | | |
| A | 0.80 | 0.90 | 1.00 |
| A1 | 0.00 | 0.02 | 0.05 |
| A3 | --- | 0.20 ref | --- |
| N | 48 | | |
| ND | 12 | | |
| NE | 12 | | |
| b | .15 | .20 | .25 |
| TOLERANCE of FORM & POSITION | | | |
| aaa | 0.10 | | |
| bbb | 0.07 | | |
| ccc | 0.10 | | |
| ddd | 0.05 | | |
| eee | 0.08 | | |
| fff | 0.10 | | |

OPTION 2:

| SYMBOL | DIMENSION | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| D2 | 4.10 | 4.20 | 4.30 |
| E2 | 4.10 | 4.20 | 4.30 |
| L | 0.35 | 0.40 | 0.45 |

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. N REFERS TO THE NUMBER OF LEADS.
4. ND AND NE REFER TO THE NUMBER OF LEADS PER SIDE.

TOLERANCES
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XX±
XXX±

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| APPROVALS | DATE |
|---|---|
| DRAWN RAC | 01/11/08 |
| CHECKED | |

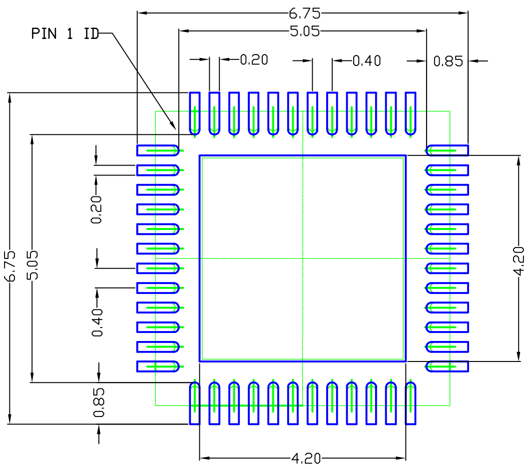
TITLE ND/NDG 48 PACKAGE OUTLINE
6.0 x 6.0 mm BODY
0.40 mm PITCH VFQFN

| SIZE | DRAWING No. | REV |
|---|---|---|
| C | PSC-4212 | 02 |

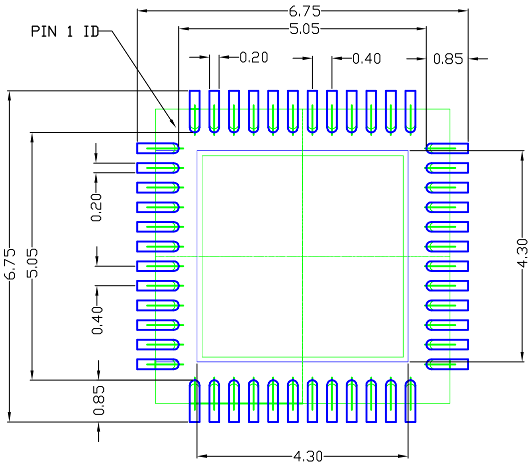
DO NOT SCALE DRAWING
SHEET 1 OF 2

# Package Outline and Package Dimensions (NDG48) – use EPAD 4.2 mm SQ

| REVISIONS | | | |
|---|---|---|---|
| REV | DESCRIPTION | DATE | APPROVED |
| 00 | INITIAL RELEASE | 01/10/08 | DP |
| 01 | UPDATE EXPOSED PAD ADD TABLE | 08/05/10 | DP |
| 02 | COMBINE POD & LAND PATTERN | 10/29/13 | J.HUA |



EPAD 4.2 mm SQ



EPAD 4.3 mm SQ

NOTES:
1. ALL DIMENSION ARE IN mm. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. COMPONENT OUTLINE SHOW FOR REFERENCE IN GREEN.
4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

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XXX±

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| APPROVALS | DATE |
|---|---|
| DRAWN RAC | 01/11/08 |
| CHECKED | |

TITLE ND/NDG 48 PACKAGE OUTLINE
6.0 x 6.0 mm BODY
0.40 mm PITCH VFQFN

SIZE C
DRAWING No. PSC-4212
REV 02

DO NOT SCALE DRAWING
SHEET 2 OF 2

## Ordering Information

| Part / Order Number | Shipping Packaging | Package | Temperature |
|---|---|---|---|
| 9DBU0841AKLF | Trays | 48-pin VFQFPN | 0 to +70° C |
| 9DBU0841AKLFT | Tape and Reel | 48-pin VFQFPN | 0 to +70° C |
| 9DBU0841AKILF | Trays | 48-pin VFQFPN | -40 to +85° C |
| 9DBU0841AKILFT | Tape and Reel | 48-pin VFQFPN | -40 to +85° C |

**"LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.**

**“A” is the device revision designator (will not correlate with the datasheet revision).**

## Revision History

| Rev. | Initiator | Issue Date | Description | Page # |
|---|---|---|---|---|
| A | RDW | 7/16/2014 | 1. Updated electrical tables with char data.<br>2. Added an additive phase jitter plot.<br>3. Added 12kHz to 20MHz *additive* phase jitter spec.<br>4. Updated Amplitude control bit *descriptions* in Byte 1. | Various |
| B | RDW | 9/19/2014 | Updated SMBus Input High/Low parameters conditions, MAX values, and footnotes. | 6 |
| C | RDW | 4/17/2015 | 1. Updated pin out and pin descriptions to show ePad on package connected to ground.<br>2. Minor updates to front page text for family consistency.<br>3. Updated Clock Input Parameters table to be consistent with PCIe Vswing parameter. | 1-6 |

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