acoustics

NR2048

High Performance Voice Processor
for Mobile Applications

Product Data Sheet

1. Introduction

NR2048 is the new generation of voice processor capable of HD Voice (wideband) and narrow band voice processing, and it is designed to improve intelligibility for voice calls, as well as helping to improve voice recognition command inputs in noisy environments. It delivers state-of-the-art voice processing capabilities to improve the listening experience of both near-end and far-end users. With acoustics's proprietary voice processing technology, the NR2048 uses advanced beam-forming technology to track the caller's voice and filters out the unwanted background noises, providing natural and clear conversations for users in any environment.

1.1 Overview

With low power consumption and highly compact footprint, the NR2048 voice processor provides noise suppression, acoustic echo cancellation (AEC) and other adaptive voice enhancements for mobile communications. It also contains specific processing modules to improve voice recognization (VR) rate and improve voice recording in noisy environments.

NR2048 provides system integrators and designers great degree of flexibilities to customize each processing module and fine-tune the algorithms to adapt to each device's unique needs and acoustic path characteristics. This IC can be easily integrated into system architectures with either a split Applications Processor(AP)-CODEC-Baseband or a highly integrated SOC basedband framework.

1.2 Key Features

- Highly integrated SOC
  - High performance voice processor with built-in hardware support for signals from 8KHz to 48KHz sampling rate
  - Voice processor with on-chip dual-core digital signal processor (DSP) sub-system, which includes hardware computation accelerators, RAM, and ROM
  - Three indepedent sets of serial port supporting flexible digital data formats, and each can be programmed as PCM, I2S or slave-mode TDM
  - Five TDM channels support up to three independent formats, and each TDM channel can be configured as either I2S or PCM
  - Highly configuable pins programmable to support up to three PDM inputs and four PDM outputs
  - PDM clock for PDM output data can be at 1.024, 2.048, 3.072 or 4.096 MHz.
  - Serial Host Interface(SHI) is I^2C-compatible and supports on-the-fly command and parameter download for processor control and configuration
  - Flexible clocking input with built-in PLL, supports 3 to 48MHz (in 1 or 2.048MHz steps, as well as 3.684, 7.68, 14.4, 15.36, 16.8, 19.2, 19.68, and 38.2MHz
  - Programmable digital gain control:-143.25 to +24dB in 0.75dB increments on voice input/output ports

- **High performance**
  - Robust AEC providing full-duplex conversation with overall Echo Return Loss Enhancement (ERLE) up to 85dB
  - Noise Suppression providing natural and clear conversation in noisy environment
  - Supports Wideband (HD Voice) and narrow band voice applications
  - Bright Voice Enhancement (BVE) for inbound listening improvement
  - Dynamic Range Control (DRC) for inbound and outbound voice paths
  - Automatic Gain Control (AGC) on inbound and outbound voice paths
  - Far-field voice pick-up for hands-free conferencing application
  - Automatic microphone calibration to compensate for ±3dB microphone sensitivity variances on multiple microphone implementation
  - High resolution equalizer to compensate for the loudspeaker frequency response in music playback mode
  - Audio equalizer to compensate for the receiving and sending frequency responses in voice communication mode
  - Supports true 3-mircrophone voice processing in handheld narrow band calls
  - Built-in side-tone generation
  - Voice recognition(VR) rate enhancement mode for voice search application under high noise environments for both handset and handsfree mode
  - Noise Reduction in sound recording mode for 8/16/24/32/44.1/48 KHz signals

- **Specifications**
  - 0.11um low power process
  - Operation voltages
    - IO:1.8V~3.3V digital input/output.
    - Core: built-in LDO provide power for internal core voltage.
  - Packages:
    - 25 ball WLCSP Package, 2.966×2.966 mm^2, 0.45mm ball pitch

NR2048 Voice Processing Capability	Inbound Voice from far-end	Outbound Voice towards far-end
Acoustic Echo Canceller		Yes
2- and 3- microphone Beamforming		Yes
Stationary and Non-Stationary Noise Reduction	Yes	Yes
Far field pickup for conferencing/recording		Yes
Automatic Gain Control	Yes	Yes
Audio Equalization	Yes	Yes
Dynamic Range Control	Yes	Yes
Ambient noise-cued Adaptive Speech Enhancement (BVE)	Yes	
Wideband(HD) and Narrowband Voice Processing	Yes	Yes
Voice Recognition Enhance mode		Yes
8KHz, 16KHz, 24KHz, 32KHz, 44.1KHz, and 48KHz Sound Recording with Noise Reduction		Yes

Summary of NR2048 Voice Processing Functions

1.3 Pin Configuration

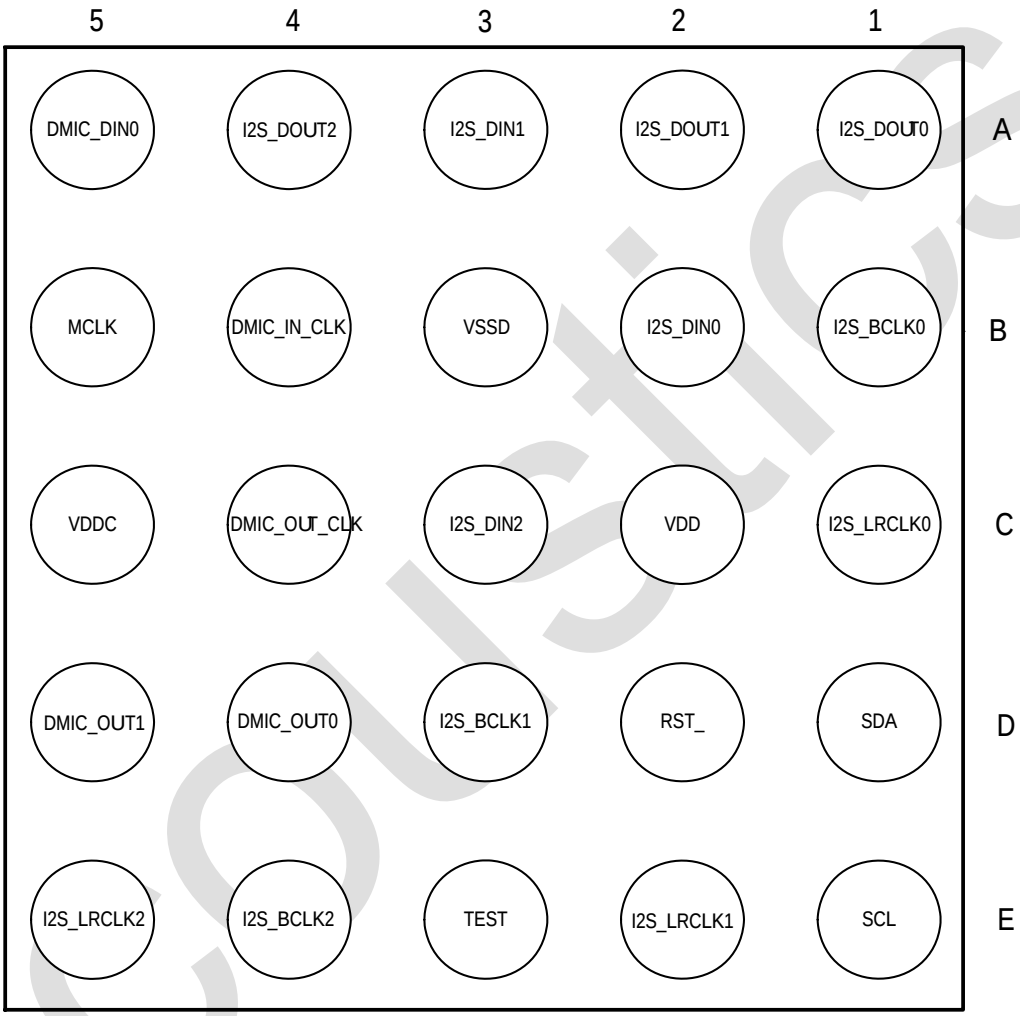


Figure 1: 25-pin WLCSP Pin Configuration - Bottom View

1.4 Device Terminal Functions

Clock	Lead	Pad Type	Supply Domain	Description
MCLK	B5	In	VDD	For external clock in

Controls	Lead	Pad Type	Supply Domain	Description
TEST	E3	In	VDD	Test only, active high
RST_	D2	In	VDD	Reset control, active high

Power Supplies	Lead	Description
VDD	C2	Positive supply for digital input/output, to 1.8V/2.5V/3.3V power supply
VSSD	B3	Ground Connection – Digital Ground
VDDC	C5	Connect via 10uF capacitor to ground, decoupling capacitor is for internal LDO that generates 1.2V for IC internal circuitry.

Serial Host Interface (SHI)	Lead	Pad Type	Supply Domain	Description
SDA	D1	In/Out	VDD	IIC-compatible serial slave data
SCL	E1	In	VDD	IIC-compatible serial slave clock

Digital Audio I/O (PCM/TDM/IIS/PDM)	Lead	Pad Type	Supply Domain	Description
I2S_DOUT0	A1	Out	VDD	Synchronous data output
I2S_DOUT1	A2	Out	VDD	Synchronous data output
I2S_DOUT2	A4	Out	VDD	Synchronous data output
DMIC_OUT0	D4	Out	VDD	Synchronous data output
DMIC_OUT1	D5	Out	VDD	Synchronous data output
I2S_DIN0	B2	In	VDD	Synchronous data input
I2S_DIN1	A3	In	VDD	Synchronous data input
I2S_DIN2	C3	In	VDD	Synchronous data input
DMIC_DIN0	A5	In	VDD	Synchronous data input
I2S_BCLK2	E4	In	VDD	Synchronous Clock/data input
I2S_BCLK1	D3	In	VDD	Synchronous Clock/data input
I2S_LRCLK0	C1	In	VDD	Synchronous Frame Sync
I2S_LRCLK1	E2	In/Out	VDD	Synchronous Frame Sync input or data output
I2S_LRCLK2	E5	In/Out	VDD	Synchronous Frame Sync input or data output
I2S_BCLK0	B1	In	VDD	Synchronous Clock input
DMIC_IN_CLK	B4	Out	VDD	Synchronous Clock input
DMIC_OUT_CLK	C4	In/Out	VDD	Synchronous Clock Input or Output

1.5 Internal Hardware Block Diagram

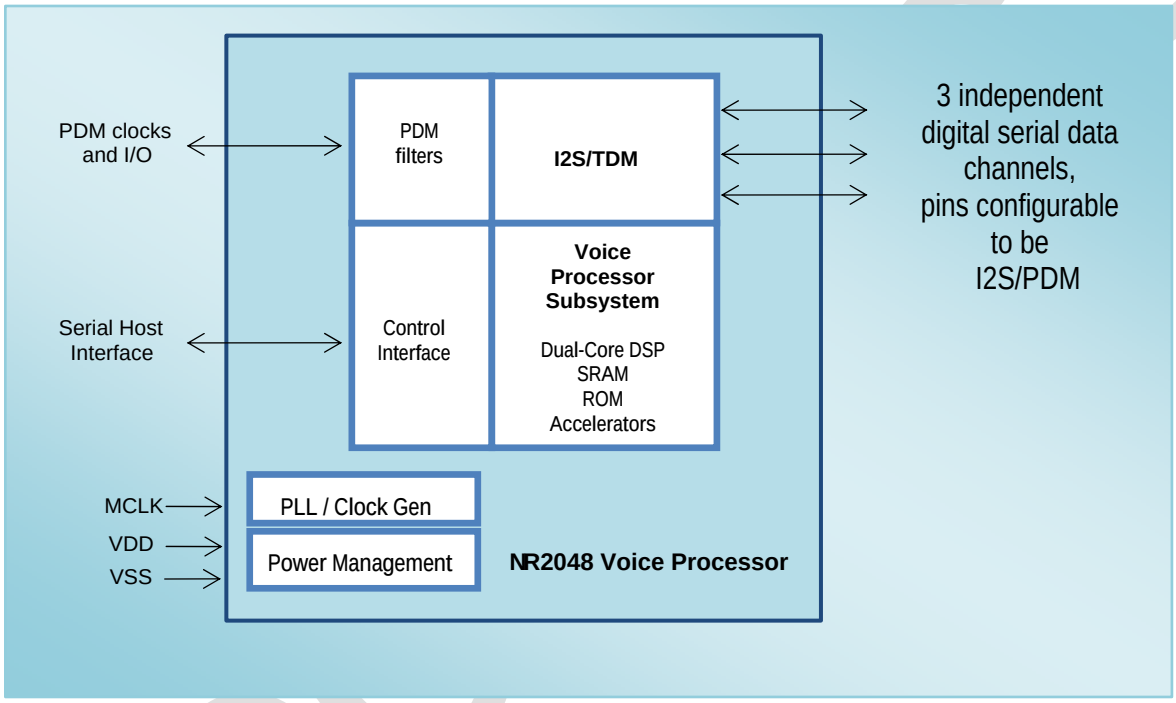


Figure 2: NR2048 Hardware Block Diagram

1.6 System Application Block Diagram

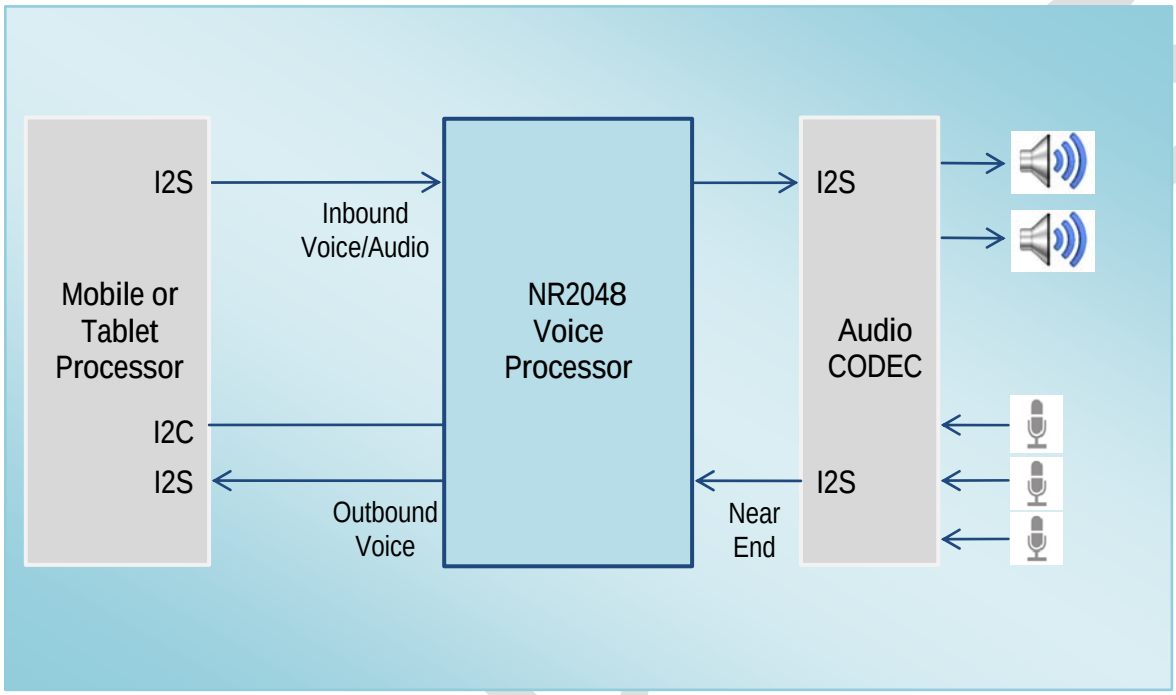


Figure 3: NR2048 Example Usage: with Mobile Processor and Audio Codec

2. Functional Description

2.1 Power Domain and Voltages

The VDDC is provided by built-in LDO which accepts voltage from 1.8V to 3.3V from VDD, or and it supplies power to the internal core and the PLL block.

In power-down mode, the majority of circuitries is shut down, and only the PLL block, together with a small portion of parameter storage memory, are still powered by VDDC.

Please follow the typical high speed circuitry guidelines and apply appropriate noise immunity capacitors at the input of these power sources. It is recommended to connect all VDDC with 0.1uF for high frequency and 2.2uF to 10uF for power decoupling to ground.

The power-down transition is controlled by parameters downloading through SHI interface.

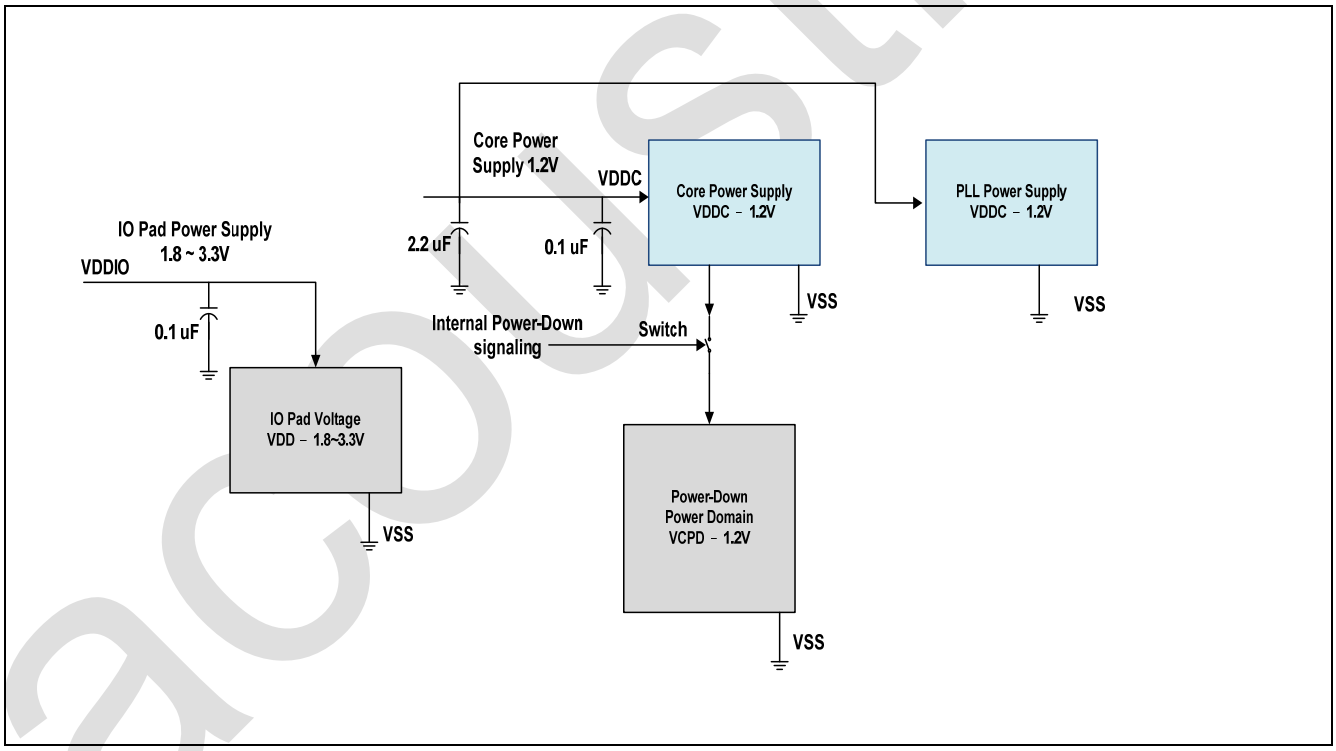


Figure 3: NR2048 Internal Power Domain

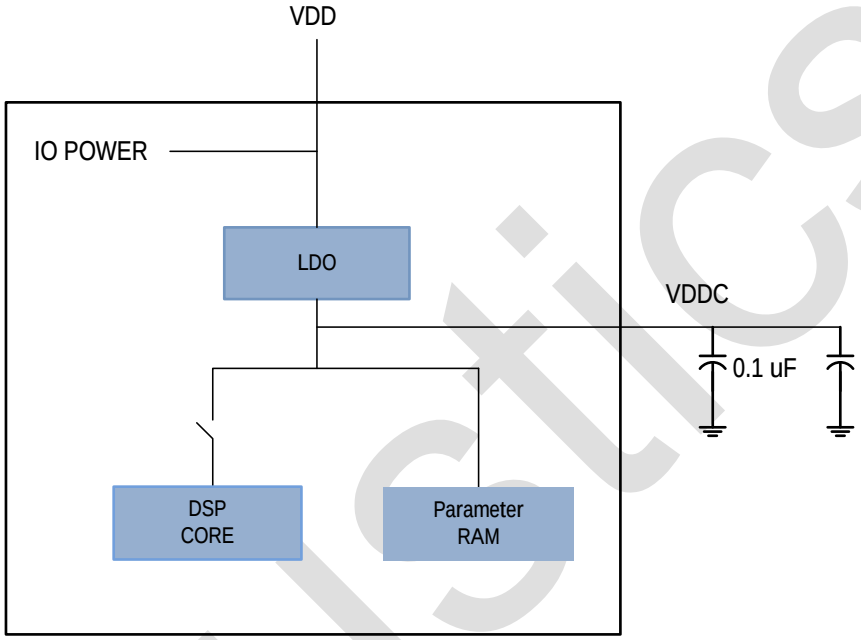


Figure 4: NR2048 On-chip LDO - power domain management

2.2 Serial Host Interface - SHI (Pins D1, E1)

The NR2048 implements a Serial Host Interface (SHI) which is an IIC-compatible, slave mode only, serial interface between NR2048 and an external processor for control information communications. It can be used to

- Transmit and receive control commands at run-time, and
- Download the necessary initialization configuration parameters during reset and power-up, should the system designer elect this option.

On this SHI, NR2048 communicates to the host processor through a bi-directional serial data line (SDA) and a serial clock line (SCL). The NR2048 SHI operates as a slave device and its serial clock is driven from the host. The master on the host processor controls SCL clocking, data transfer start bit and stop bit, and also addressing of slave devices. The NR2048 supports 8-bit address and its device address is "**0xC0**

Depending on the host processor instruction, the SHI can operate as a transmitter (writing data) or a receiver (reading data). Note that the SHI interface supports the standard clock speed of 100 kHz or up to a maximum speed of 400 kHz (if MCLK is above 10MHz).

The standard byte format of SHI data line must be 8–bit long in every byte. Each byte consists of 8 bits plus 1 acknowledge bit, and it is one data bit per clock pulse. If operating as a receiver, it will return an acknowledge bit upon each successful byte transfer, otherwise it will return a NOACK signal. There is no restriction on the maximum number of bytes per data transfer. Data transfer can be aborted if the master device generate a STOP condition to terminate a transfer. Each data transfer frame must start with a START or a RESTART symbol and ends by a STOP symbol.

Table 1: SHI START and STOP data transition

S: START	SDA transition from 1 to 0 when SCL=1
P: STOP	SDA transition from 0 to 1 when SCL=1

Within the data transfer frame, multiple command sequences are allowed and there is no restriction on the maximum numbers of bytes per frame. Each command sequence starts with a sync word "0xFCF3", follows by a command entry byte (e.g. 0x3B is MEM_WRITE) and number of bytes per specific command. The following figures and tables summarize the details for the SHI command sequence.

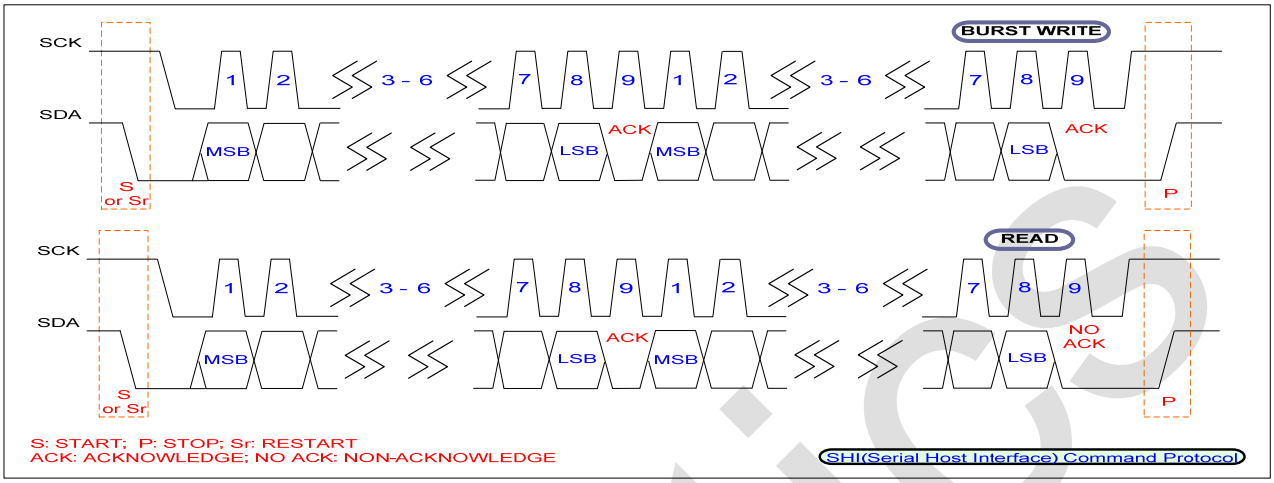


Figure 5: SHI Data Transfer Command Protocol

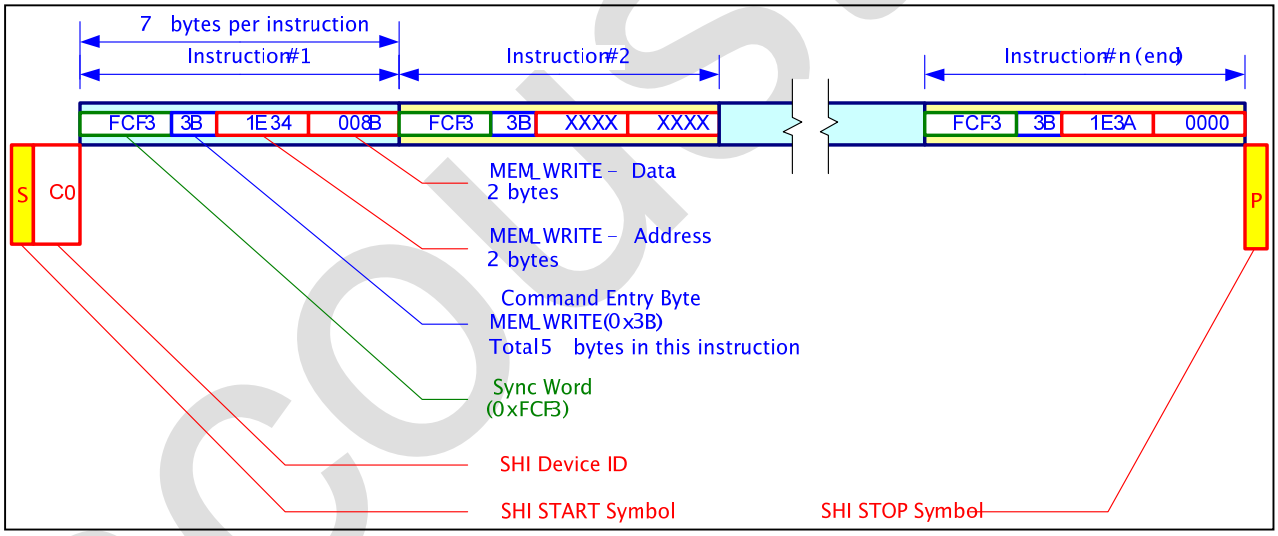


Figure 6: SHI Command Sequence

Table 2: SHI Command Name

Command Entry Name	Command Entry Byte	Number of the bytes for each functional bytes		
		Address Byte	Data Byte	Total (cmd+address+data)
MEM_WRITE	0x3B	2	2	5
MEM_READ	0x37	2	0	3
REG_READ	0x60	1	0	2

Table 3: SHI Command Byte Format

Serial Command Entry Byte								
Bit	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Description	Access object type				Read /Write	Data byte number		Address byte number
Value Details	Data Memory (0011b) DataPort(0110b)(e.g. register)				Read: 0 Write: 1	2bytes (01b) 1byte (00b) 0byte (11b)		Two address bytes(1b) Data memory access One address byte(0b) Data port access

Table 4: SHI Command Byte Bit Definition

Data length	1byte	
Bit	**Pattern**	**Descriptions**
D7 - D4	0011b	For accessing Data Memory
	0110b	For reading the Data ports.
D3	0b	Read
	1b	Write
D2-D1	00b	1 byte data write, or in Data Port Read mode.
	01b	2 bytes data write
	11b	0 byte data (in Data Memory Read mode).
D0	1b	Two address bytes for accessing Data Memory
	0b	One address byte for reading Data Port (Either 0x25 for lower byte or 0x26 for upper byte.

2.3 Digital Data Intefaces

The NR2048 inputs digitized voice data from microphone inputs of the near-end talker signal and performs acoustic echo cancellation, beamforming, and noise suppression on it. Other voice signal enhancements such as gain adjustment and equalization can also be performed to improve the voice signal. The processed signal is then sent digitally along the outbound voice path. The far-end talker voice enters as digital inbound signal via the serial data path, and it could be further enhanced by Bright Voice Enhancement, Equalization, or Dynamic Range Control before sent out digitally towards the loudpeaker.

The NR2048 is designed to be highly compact,and some the data I/O pins are multiplexed and configurable to support a variety of data modes. With mix and match, it has very flexible digital data interconnect capabilities to be used in various system configurations.

For the PDM support,

- The highly configuable pins are programmable to support up to three PDM inputs and up to four PDM outputs, and
- The PDM clock for PDM output data can be at 1.024, 2.048, 3.072 or 4.096 MHz.

PDM Data Interface	Lead	Name	Mode	Pin Multiplexed with	Comments
PDM inputs	A5	PDMI0	Master	-	
	C3	PDMI1		Rx_2	
	E4	PDMI2		Rx_3	
PDM Outputs	D4	PDMO0	Master or Slave	-	
	D5	PDMO1		GPIO0	
	A4	PDMO2		Tx_2	
	E5	PDMO3		Tx_3	

PDM Clocks	Lead	Description
PDMI_CLK	B4	Output, and master mode only for PDM input
PDMO_CLK	C4	Can be Input or Output, slave or master mode for PDM output

For the PCM/I2S serial data, there could be up to three indepedent sets of serial port supporting flexible digital data input and output, and each can be programmed as PCM, I2S or slave-mode TDM.

Data Interface	Lead	Name	TDM slots	Pin Multiplexed with	Comments
TX TDM outputs	A1	Tx_0	8	-	
	A2	Tx_1	8	-	
	A4	Tx_2	8	PDM02	
	E5	Tx_3	2	PDM03	
	E2	Tx_4	2	-	
RX TDM inputs	B2	Rx_0	8	-	
	A3	Rx_1	8	-	
	C3	Rx_2	8	PDMI1	
	E4	RX_3	2	PDMI2	
	D3	Rx_4	2	-	

As could be seen from the table above:

- There are five TDM channels supporting up to three independent formats each with its own frame sync and bit clock, and in addition each TDM channel can be configured as either I2S or PCM
- The serial data data inputs/outputs Rx0,Rx1,Rx2,Tx0,Tx1,Tx2 can each support up to 8 TDM slots, and Rx3,Rx4,Tx3,Tx4 can each support up to 2 TDM time-slots

Serial Channel	Lead	Name	TDM slots	Pin Multiplexed with	Comments
Clock	B1	BCLK_0	8	-	
	D3	BCLK_1	8	Rx_3/PDMI2	
	E4	BCLK_2	8	Rx_4	
Frame Sync	C1	FRAME_0	8	-	
	E2	FRAME_1	8	Tx_4	
	E5	FRAME_2	8	Tx_3/PDMO2	

2.4 Serial Port Data Interfaces

NR2048 provides 5 sets of TX(TX0, TX1, TX2, TX3, and TX4) and RX(RX0, RX1, RX2, RX3, and RX4), which are associated with 3 sets of frame-sync's (FRAME0, FRAME1, and FRAME2) and bit clocks BCLK (BCLK0, BCLK1, and BCLK2). Each TX and RX are independent and can be programmed to use FRAME0 and BCLK0, or FRAME1 and BCLK1, or FRAME2 and BCLK2. FRAME0, FRAME1 and FRAME2 are always paired with BCLK0, BCLK1 and BCLK2, respectively.

(1) TX0, TX1, TX2, RX0, RX1 and RX2 can provide 1 to 8 data slots and TX3, TX4, RX3 and RX3 can provide 1 or 2 data slots.

(2) TX0, TX1, TX2, TX3, and TX4 can be driven or tri-stated.

(3) The three sets of serial port (FRAME0 and BCLK0, FRAME1 and BCLK1, FRAME2 and BCLK2) can be programmed to provide PCM(slot number =1), I2S(slot number = 2,4,6,8), or TDM formats.

(4) The rate of FRAME0, FRAME1, and FRAME2 can be set to 8kHz, 16kHz, 24kHz, 32kHz, 44.1kHz, or 48kHz.

2.4.1 TDM data transfer

TDM data format is used to transfer data between NR2048 and external devices. The TDM data transfer is supported by clock, data and frame sync signals. All the data bits are synchronous to the serial clock, and the data bits are organized into time slots or TDM channels. A frame consists of multiple slots/channels. The start of each TDM frame is defined by the frame sync signal.

The three sets of FRAME and BCLK:

- Programmable clock and frame sync polarity (rising or falling edge)
- Supports 1 to 8 time slots
- Slot length: 16-,20-,24-,28-,and 32-bits
- Word length: 16-,20-, and 24-bits
- First-bit data delay: 0, 1 clock cycle
- Left/right alignment of word inside slot
- Frame(LRCK can be started with low or high)
- Frame(LRCK)width can be 1 to (slot number)*(slot length)-1 cycles of BCLK
- Data can be transmitted/received at both rising or falling edge of BCLK.
- Bit order: MSB first or LSB first
- Bit pad: Automatically masks non-significant bits (sets to "0").

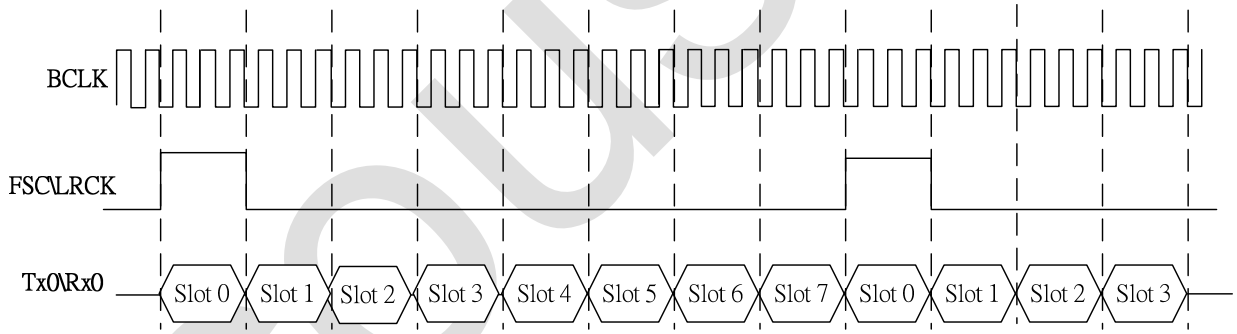


Figure 7: TDM format 8 channel example

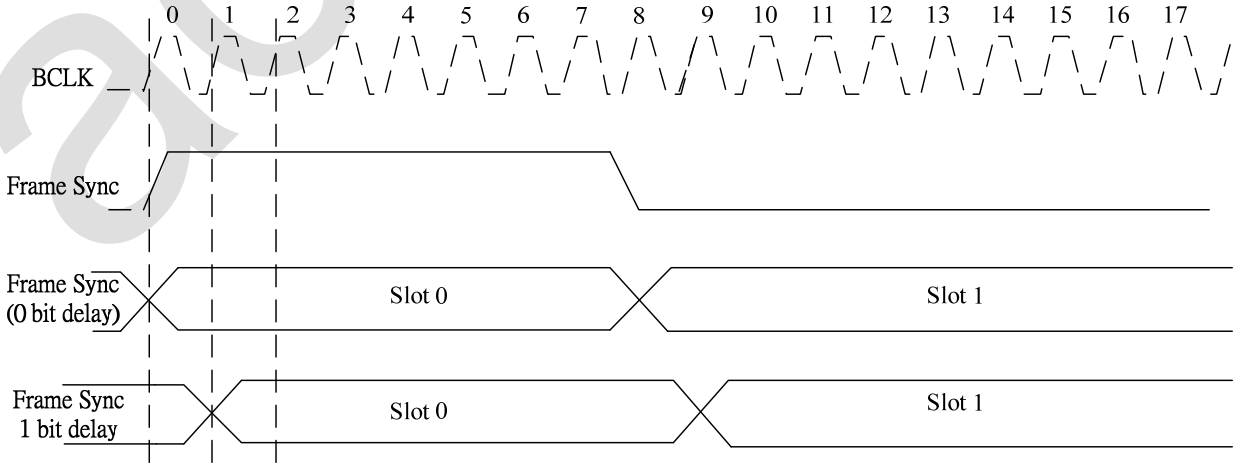


Figure 8: TDM Frame Bit delays from Frame Sync

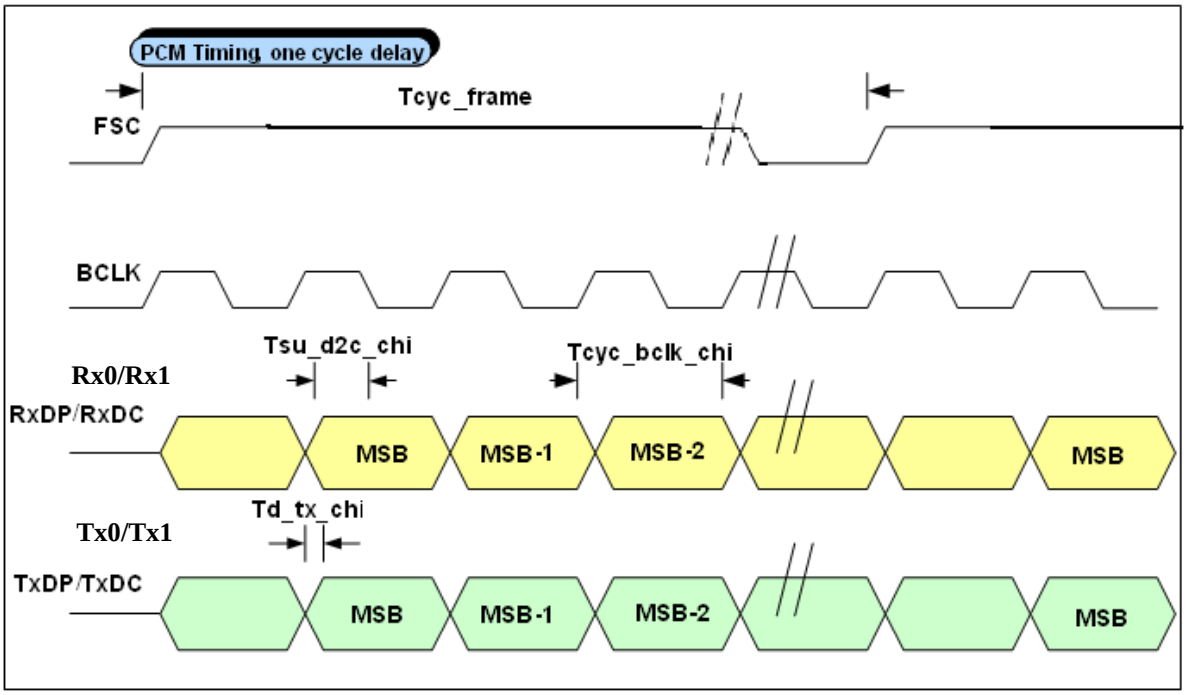
2.4.1 PCM Interface Master/Slave

PCM mode can be provided by serial port of NR2048 by setting the slot number to "1". FRAME signal can be set to 8kHz, 16kHz, 24kHz, 32kHz, 44.1kHz, or 48kHz, and BCLK rate can be set to 16, 32, 64,128, or 256 times of FRAME signal in slave mode. In master mode, BCLK can be only 32 times of FRAME.

Long frame and short frame both have same timing. "Tsu_f2b" is same between short frame and long frame. The diagram below shows long and short frames. Short frame is FRAME pulse which is only one BLCK wide and long frame is Frame width has multiple of BCLK. In our design, falling edge of BCLK is to detect start of FRAME and word length is determined by word-length bits in the Serial Port control register (Table 5).

In master mode, the width of the FRAME is always one BCLK cycle; in slave mode, hardware detects the first rising of FRAME, and there is no need to set the length of FRAME. .

The figures below show the PCM timings with two different cycle delays.



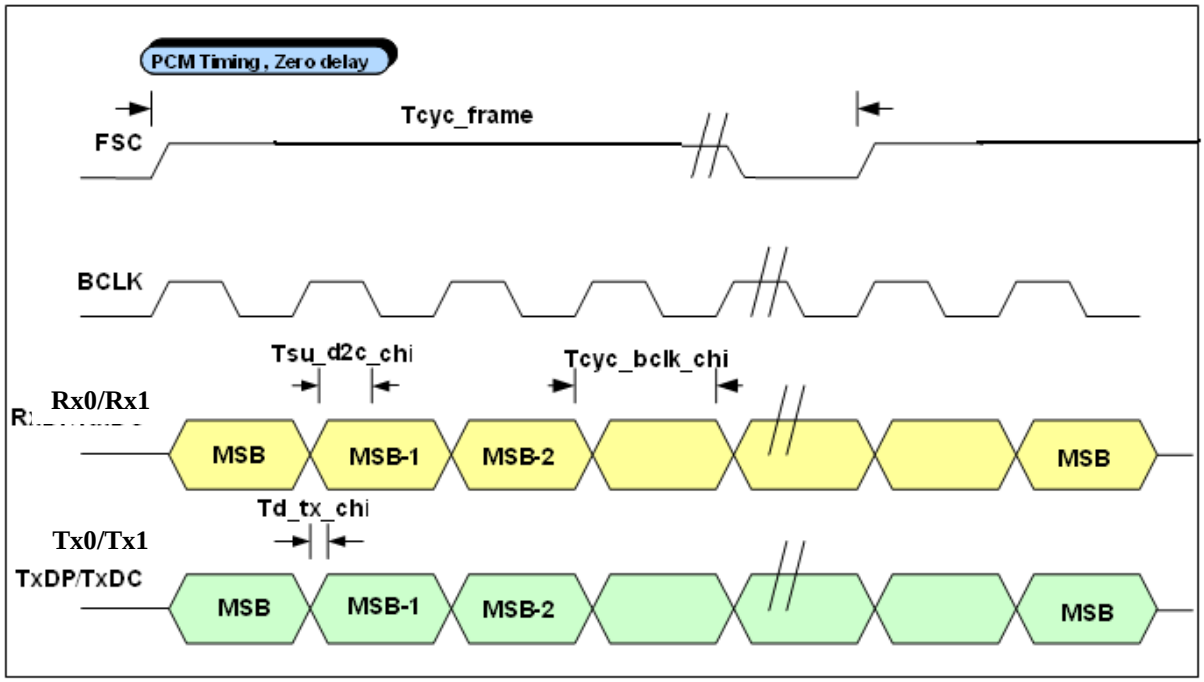
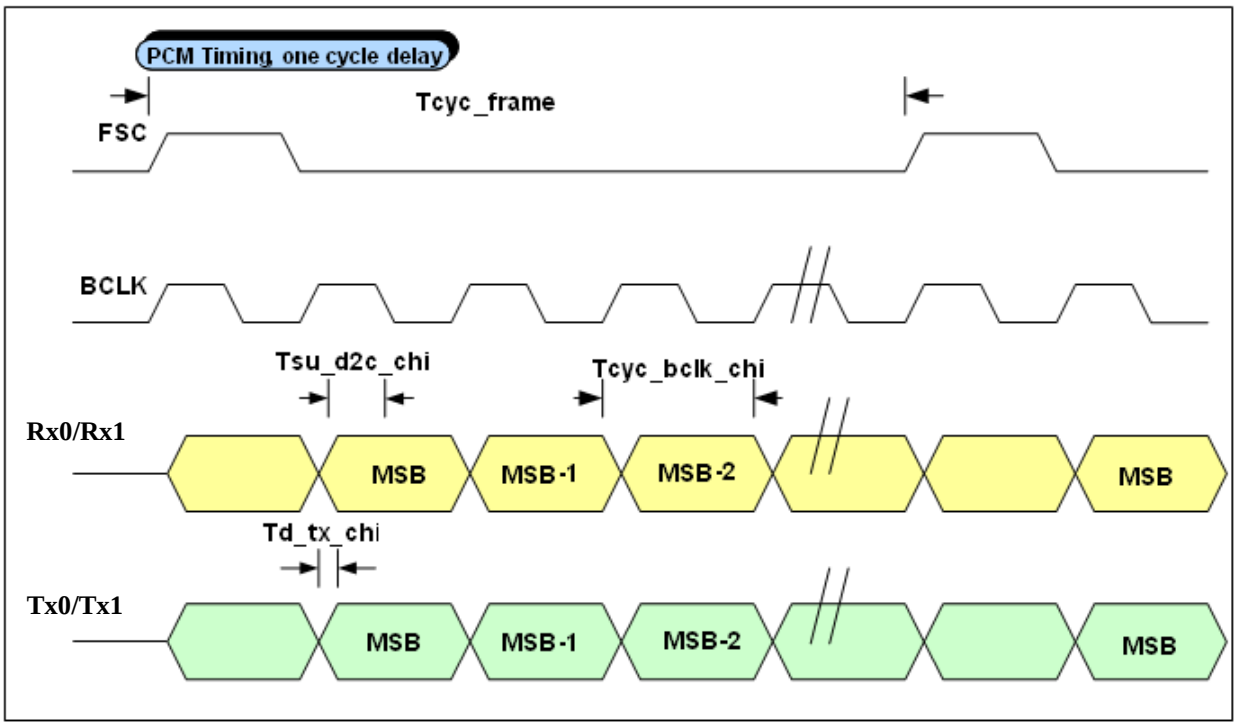


Figure 9: Long Frame PCM Timing



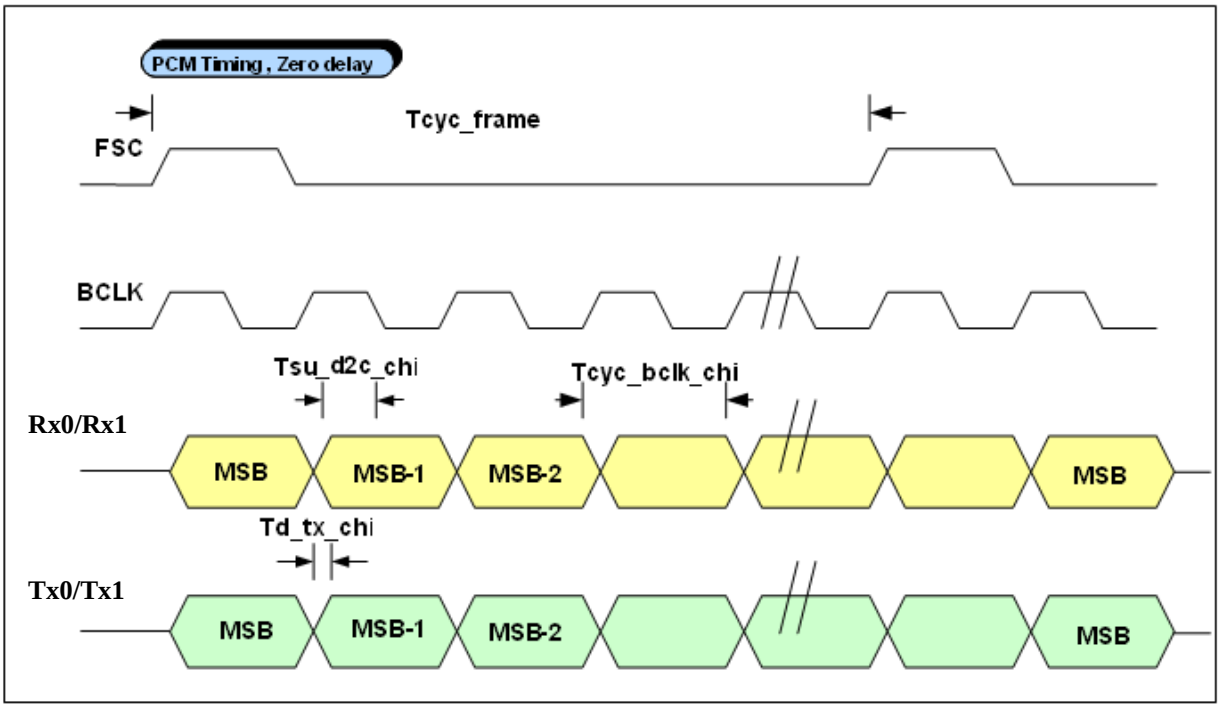


Figure 10: Short Frame PCM Timing

2.4.2 I2S Interface Master/Slave

The serial port pins are program to run in I2S mode by setting the slot number to "2", "4", "6", or "8" depending on rate of BCLK. The LRBCK signal can be set at 8kHz, 16kHz, 24kHz, 32kHz, 44.1kHz, or 48kHz.

In slave mode, the BCLK rate can be set to 16 or 32 times of LRBCK when slot number is programmed to "2", it could be set at 64 or 128 times of LRBCK when the slot number is programmed to "4", it could be set at 96 or 192 times of LRBCK when the slot number is programmed to "6", and it could be set at 128 or 256 times of LRBCK when slot number is programmed to "8".

In master mode, the BCLK rate can be only set at 32 times of LRBCK.

The following diagrams illustrate the different types of IIS timings in terms of cycle delay, edge latch and LRCK high for channels.

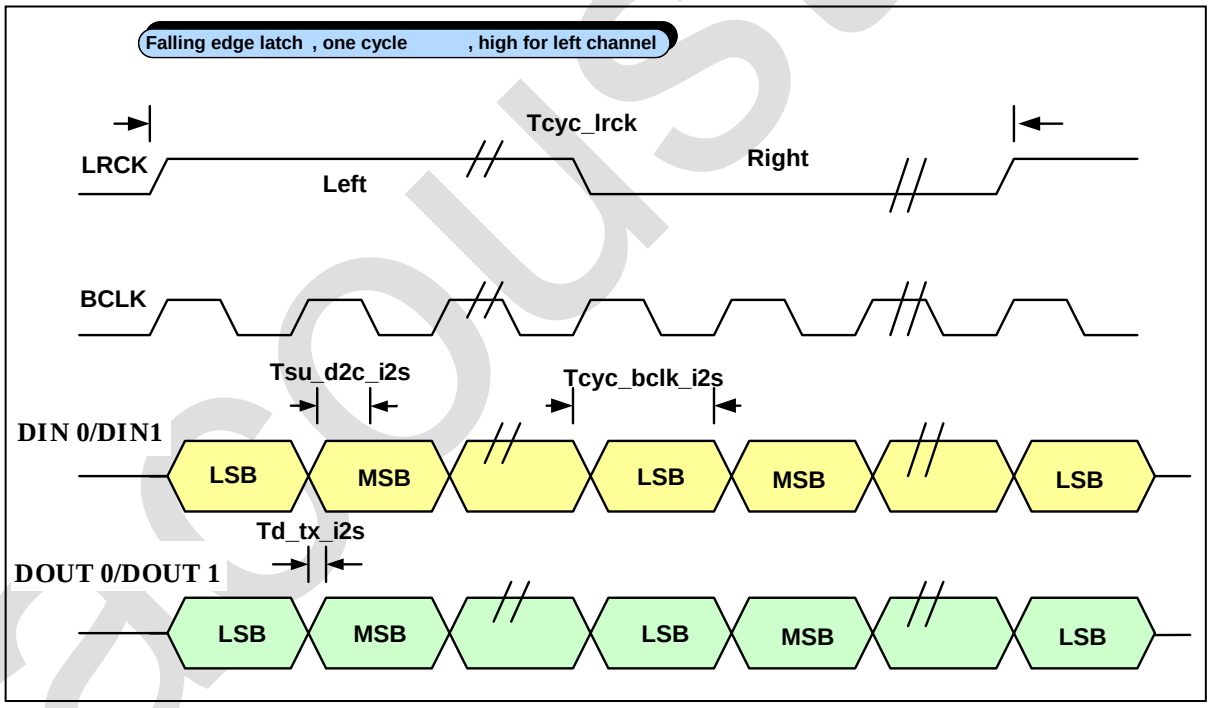


Figure 11: IIS Falling Edge Latch, LRCK High for Left Channel, 1 Cycle Delay

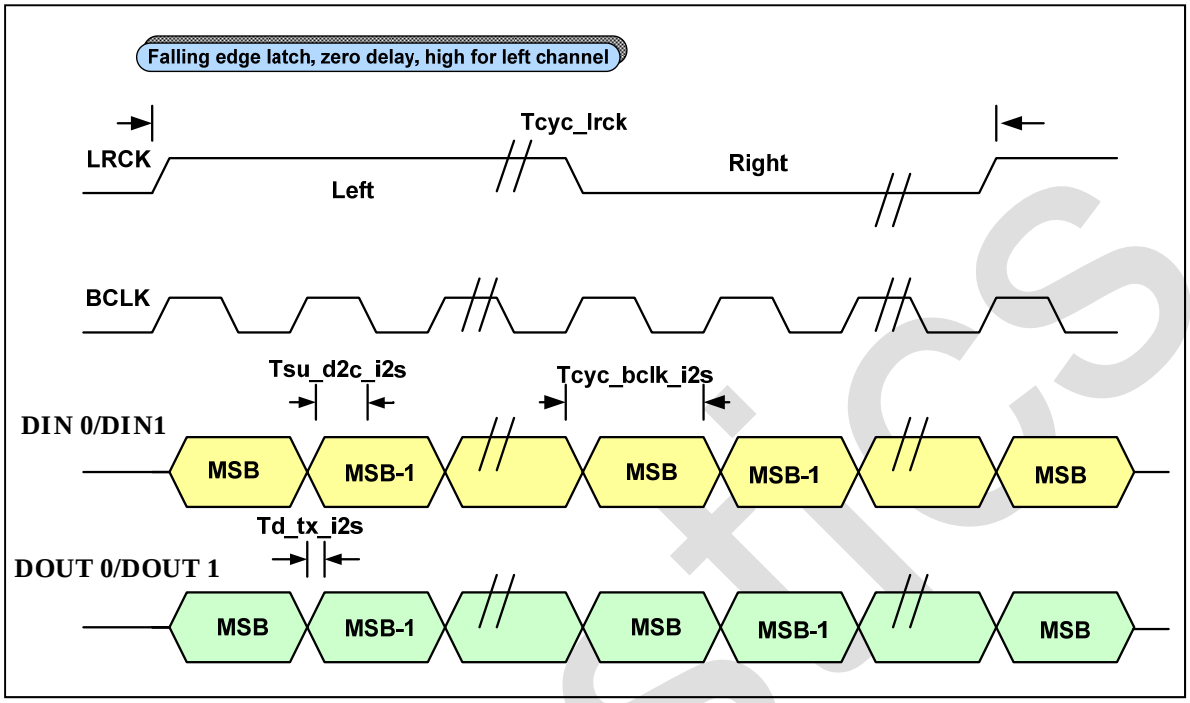


Figure 12: IIS Falling Edge Latch, LRCK High for Left Channel, 0 Cycle Delay

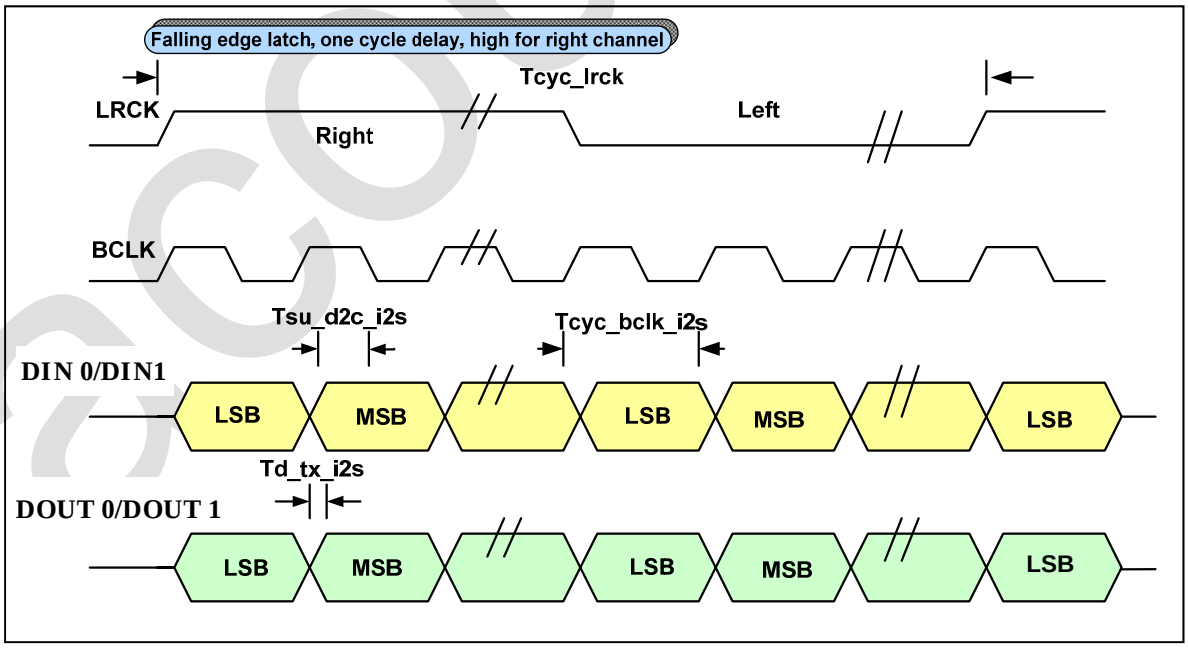


Figure 13: IIS Falling Edge Latch, LRCK High for Right Channel, 1 Cycle Delay

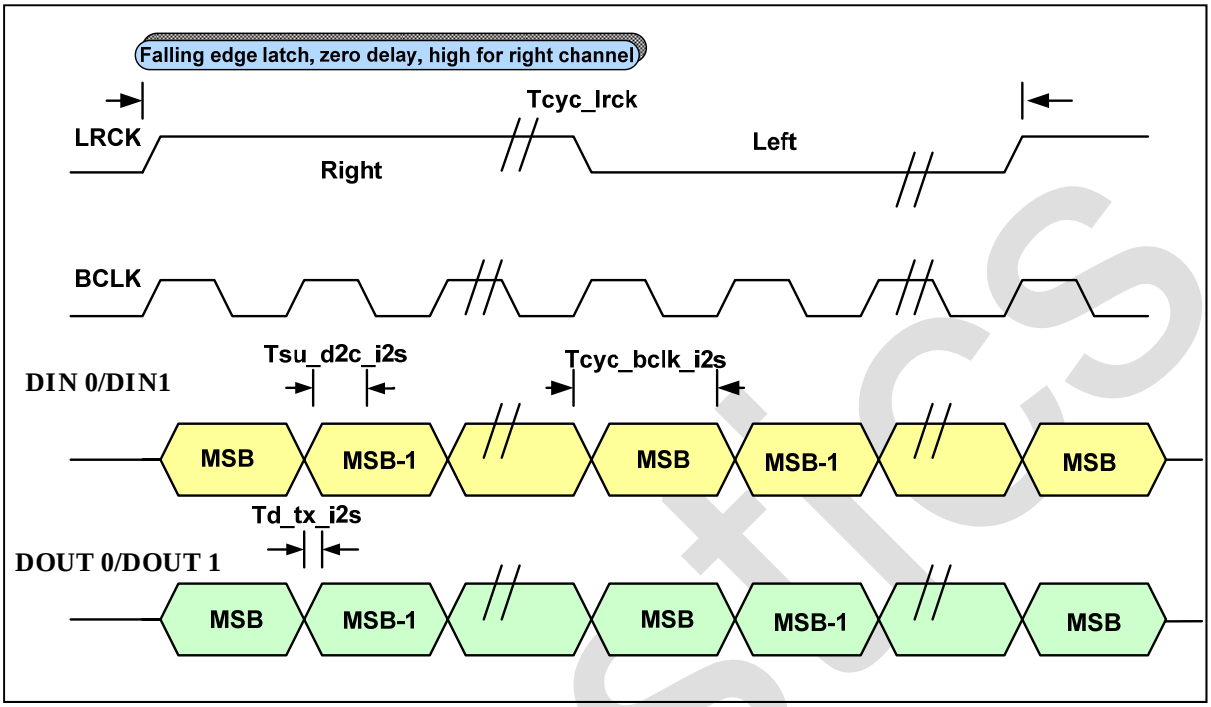


Figure 14: IIS Falling Edge Latch, LRCK High for Right Channel, 0 Cycle Delay

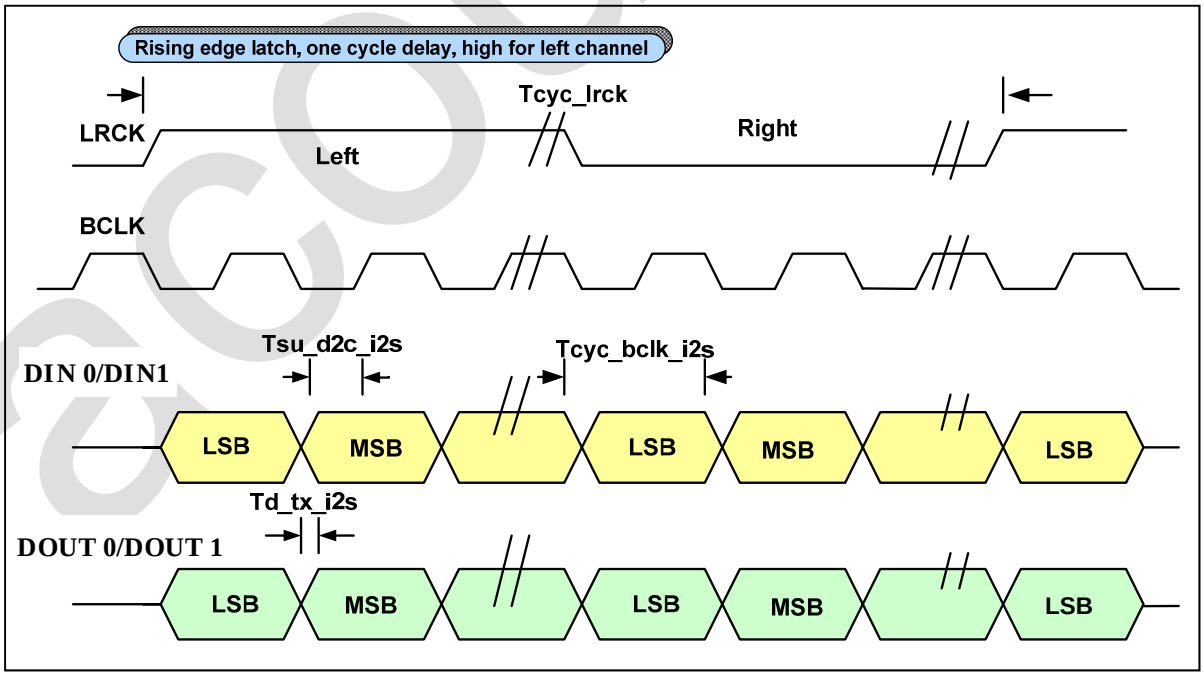


Figure 15: IIS Rising Edge Latch, LRCK High for Left Channel, 1 Cycle Delay

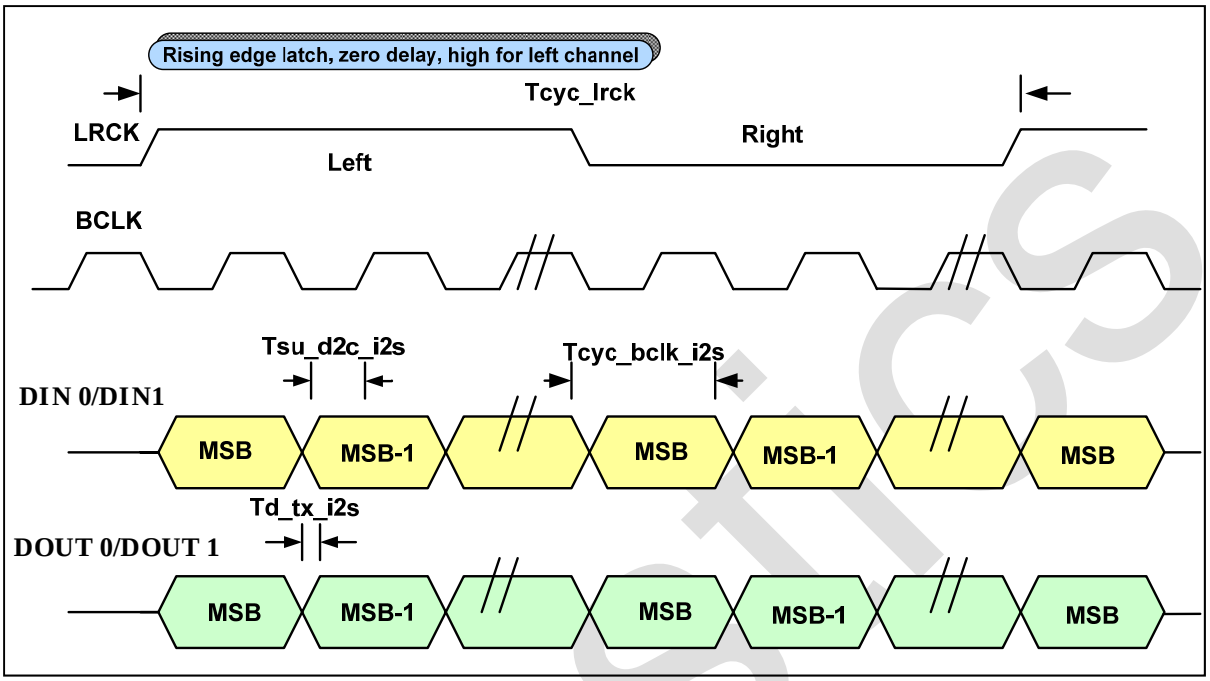


Figure 16: IIS Rising Edge Latch, LRCK High for Left Channel, 0 Cycle Delay

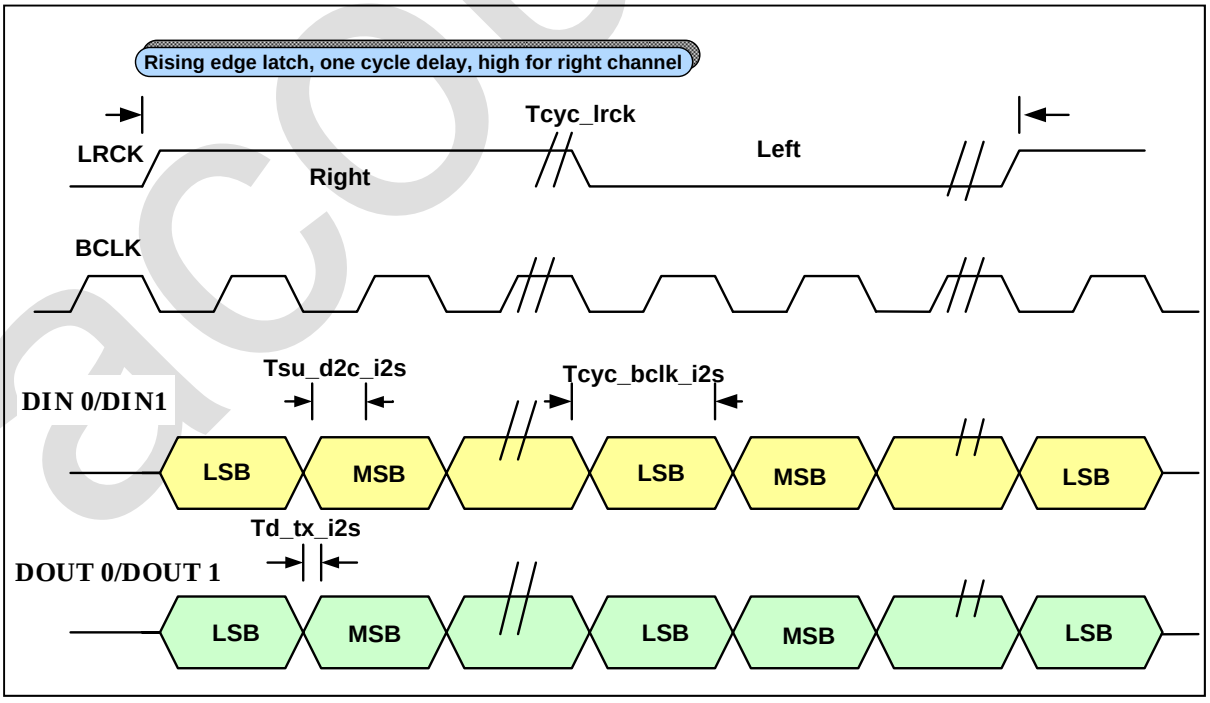


Figure 17: IIS Rising Edge Latch, LRCK High for Right Channel, 1 Cycle Delay

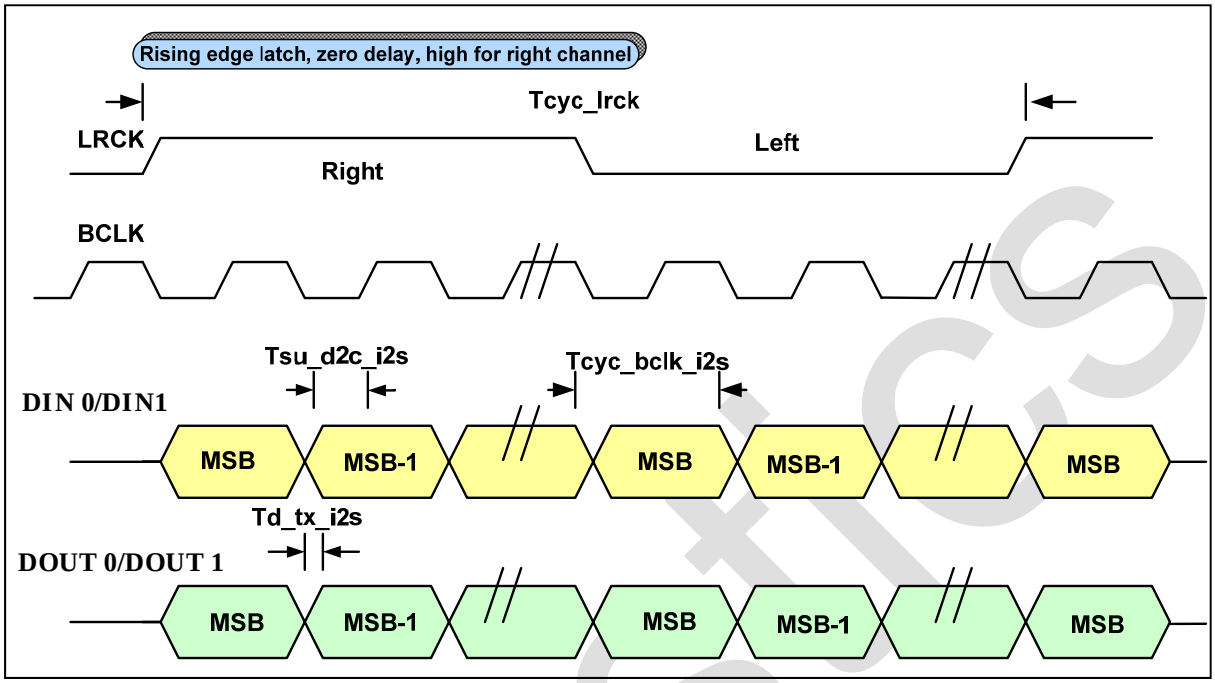


Figure 18: IIS Rising Edge Latch, LRCK High for Right Channel, 0 Cycle Delay

2.5 PDM Interface

NR2048 has configurable pins that can support up to three PDM inputs (6 microphones in) and four PDM outputs (8 speakers out). Both PDM inputs and PDM outputs could support the clock rates of 1.024, 2.048, 3.072 and 4.096 MHz in the master mode (when PDM clock is generated by NR2048).

PDM inputs on the NR2048 can work in master mode only, but PDM outputs could work in either master mode or slave mode.

The PDM bit stream provides NR2048 the raw samples to process from one or more digital microphone input. In master mode, the NR2048 generates the PDMCLK at the aforementioned 1.024, 2.048, 3.072 or 4.096 MHz, the microphone transmits oversampled raw data through the PDM data input pins. The digital filter hardware on the NR2048 processor handles and performs the re-sampling of the microphone bit stream to fixed 16-bit PCM samples at the desired sampling rate for the voice processor.

Note that the MIC0 and MIC1 data on the PDM serial data input can be swapped by register setting (0x22fA bit13: PDM_CLK_POLARITY). Please refer to the NR2048 Users Configuration Guide for details, the diagram below illustrates the PDM serial data input format.

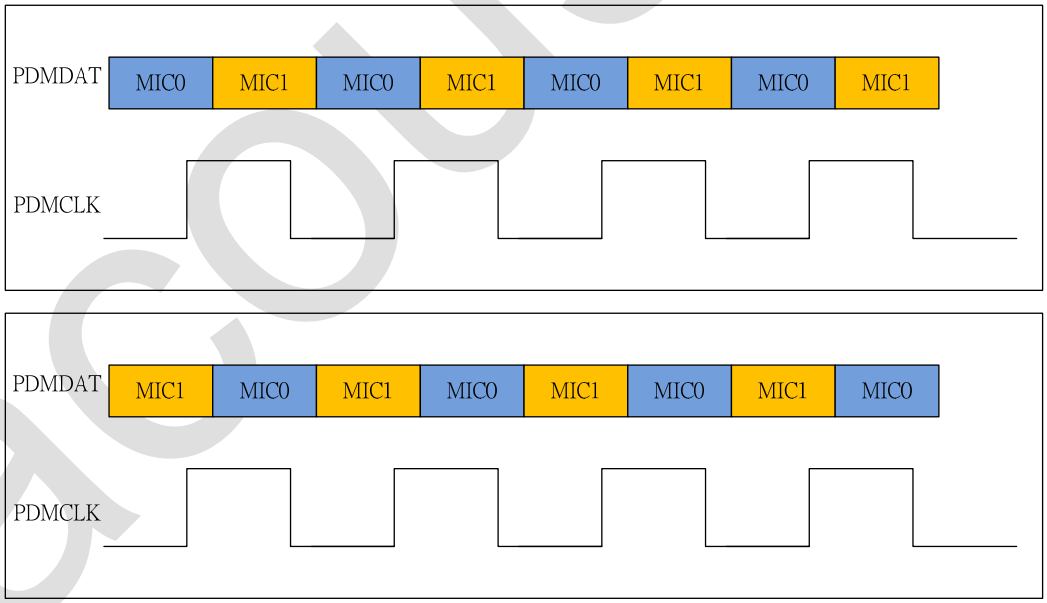


Figure 19: NR2048 Digital Microphones Interface Clock and Data

(MIC0 and MIC1data can be swapped)

2.6 Modes of Operation

Depending on the condition, the NR2048 operates in one of the following 4 modes.

Hardware Reset Mode

Whenever power is applied or when RST_ is low, the processor enters into this mode and remains in it until 10ms after the RST_ pin is pulled high. In this mode, the processor waits for the external clock and the internal PLL to stablize. 10ms after the RST assertion, the processor enters into the Software Reset Mode. Note that the RST_ pin should not be used as power-down function but instead as the power-down wake-up function.

Software Reset Mode

In software reset mode, The NR2048 takes command parameters from an external host processor through the IIC-compatible SHI. These commands sets up the various operational configuration of NR2048.

The maximum speed of SHI at this time is about 1/25 of that rate of the "MCLK"(master clock) rate. The processor exits this mode to enter the Operational Mode when the parameter value at DM(0x22FB) set to 0 (done by the NR2048 processor after parameter configuration is done). The SHI won't be able to communicate during the first 4096 cycles of "MCLK" after DM(0x22FB) is programmed.

Operational Mode

Entering this mode, the software sets up hardware internal registers according to the parameter configuration which is then followed by a nominal 70 milli-seconds initialization procedure. Afterwards, the NR2048 starts the data transfer its inputs and outputs through the digital interfaces. The processor can be commanded to enter the Power Down Mode through the IIC-compatible SHI.

Power Down Mode

In NR2048, the power down is commanded to setan internal register bit through SHI, and then wake up can then be via asserting reset pin only(RST_).

After the Power Down wake up, the processor can enter into either the Software Reset or the Operation mode, depending on the setting of the parameter at DM(0x22F1). If it enters Operation Mode, no parameter setting is required since all the internal register value will be maintained. In order for the processor to exit the Power Down Mode correctly, it will need 13ms for state-management work before it can accept any new set of parameter download, or re-enter the Operational Mode. Power-down wake up or power down "reset mode" are determined by parameters setting in NR2048 tuning guide.

The following figure is a state transition diagram which shows the NR2048 chip transition between these 4 states.

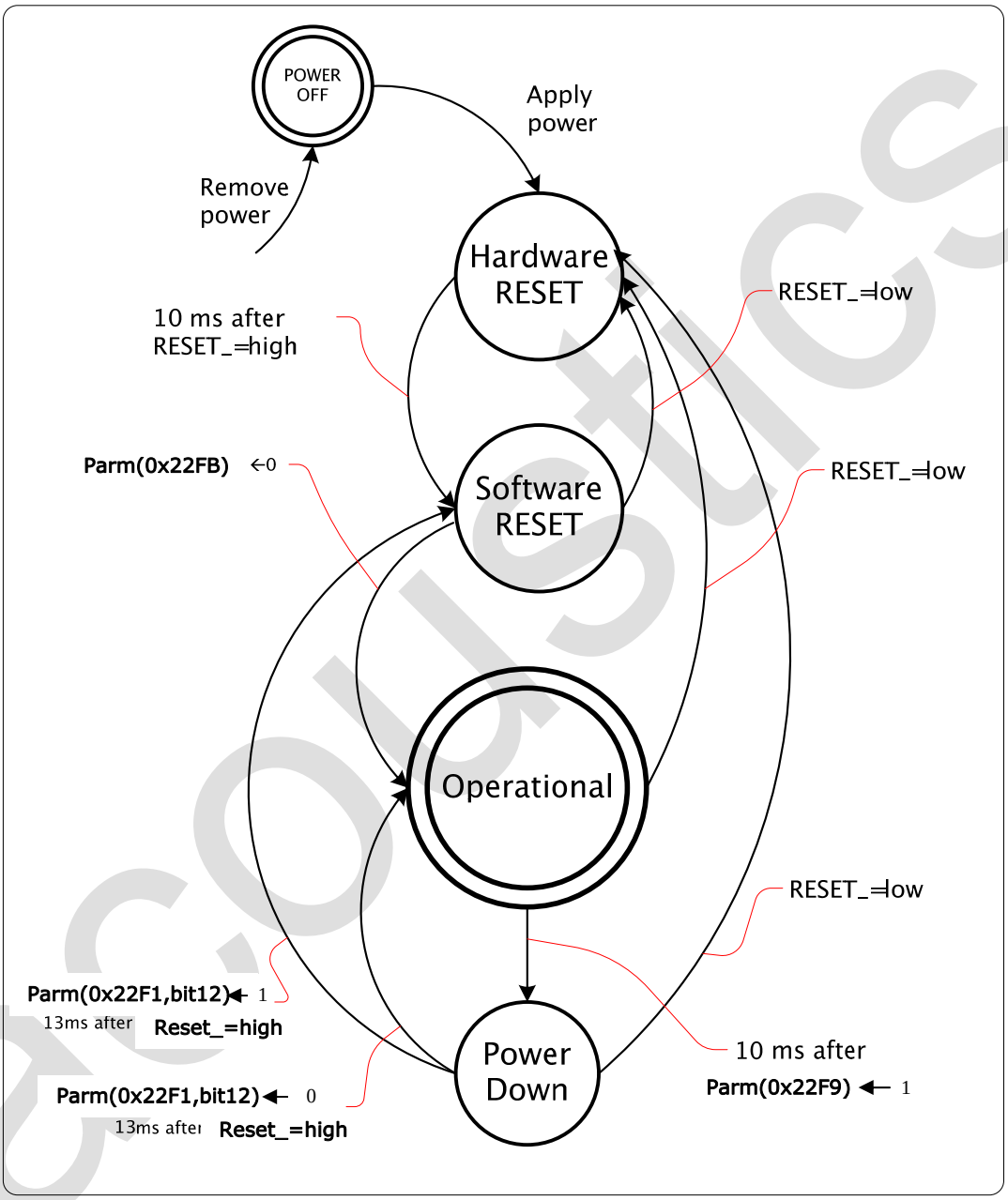


Figure 20: State Transition Diagram

2.7 HW Bypass Mode

This mode is only enabled in power down mode. The NR2048 supports a Bypass Communication mode which can be commanded to enter via SHI parameters download. The available hardware data path bypasses are from Rx1 to Tx0 and from Rx0 to Tx1.

Please refer to Fig. 27 for the operation mode to HW bypass mode.

3. Electrical and Timing Specification

Note that all data in this section are measured at room temperture and in normal operating condition.

3.1 Absolute Maximum Ratings

Absolute maximum continuous ratings are those values beyond which damage to the device could occur. Exposure to those conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under these conditions is not implied.

Table 5: Absolute Maximum Ratings

Parameter	Symbol	Condition	Max Rating	Unit
Power Supply Voltage	VDD	1.8V – 3.3V	3.6	V
Latch Up Current	LU		200	mA
Storage Temperature	T_{stg}	-	-40 to 150	^{0}C
Juntion Temperature	T_J		125	^{0}C
ESD(Human body model)	VESDHBM		2k	V
ESD(Machine model)	VESDMM		200	V

3.2 Recommended Operating Conditions

Table 6: Recommended Operating Conditions

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Digital I/O Supply Voltage	VDD	Supplied externally	1.62	1.8/ 3.3	3.6	V
Operating Temperature	T_{amb}	Extended Grade Automotive Grade	-20 -40	25 25	70 85	°C

Notes: The power ripple (AC element) has to be limited within 100mV

3.3 DC Characteristics

Table 7: DC Characteristics

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Active Power Supply Current	I_{Bypass}	In power down HW bypass modes		0.5		mA
	I_{VDD}	2-mic mode		15(1)		mA
Power Down Current	I_{VDD}	2-mic mode		10		µA
Input Leakage Current	I_{IH}	VDD = 1.8V	-1	-	1	µA
	I_{IL}	VDD = 0V	-1	-	1	µA
Digital Output Voltage High	V_{OH}	I_{OH} = 1mA	0.9*VDD	-	-	V
Digital Output Voltage Low	V_{OL}	I_{OL} = 1mA	-	-	0.1*VDD	V
Digital Input Voltage High	V_{IH}	VDD = 1.8V	0.7*VDD	-	-	
Digital Input Voltage Low	V_{IL}		-	-	0.45	V
Digital Output Leakage Current	IO		-1		1	µA
Input Capacitance	CIN			2		pF
Power Dissipation	P_{PDN}			18		µW
	P_{SYS}	T_{amb}=25°C,		27(1)		mW

Notes:
VDD=1.8V, at 25°C, Sampling Rate at 16KHz, and the FM-36 in normal operating condition, unless otherwise noted
(1) The number will be re-confirmed after CSP package is done and measured by product qualification team.

3.4 Timing Characteristics

Table 8: Timing Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit
Rise/fall time of input pins except for SCL/SDA		-	-	20	ns
Setup time from Power to master clock	Tsu_Vdd2clk		1		ms
Reset active low time	Trst_	120	-	-	µs
Setup time from master clock to rising edge of RST#	Tsu_clk2rst	80	-	-	µs
Reset to parameters programming start setup time	Tsu_rst2pp	2(1)	10	-	ms
Wake up to 2nd power down or 2nd parameters programming setup time	Tsu_wu2pp		15		ms
Parameters programming to Master clock off hold time	Th_pp2clkoff	12	-	-	ms
Power down active low time	Twpd	50	-	-	ms
Time delay from DSP ROM flag setting to the next DSP register accessing	Tsu_pp2pp	0.4	-	-	ms
1st parameter programming to bypass mode setup time	Tsu_pp2bp	100	-	-	µs
Master clock frequency	Tcyc	30.5	-	333	ns
Master clock high width	Thigh	45%	-	55%	Tcyc
Master clock low width	Tlow	45%	-	55%	Tcyc
PCM Frame Frequency	Tcyc_frame	8		48	kHz
PCM BCLK Frequency	Tcyc_bclk_chi	128		12288	kHz
PCM RX setup time	Tsu_d2c_chi	20	-	-	ns
PCM TX delay	Td_tx_chi	-	-	20	ns
IIS LRCK Frequency (2)	Tcyc_lrck	-	16	-	kHz
IIS BCLK Frequency(2)	Tcyc_bclk_IIS	128		12288	kHz
IIS RX setup time to clock edge(2)	Tsu_d2c_IIS	20	-	-	ns
IIS TX delay time(2)	Td_tx-IIS	-	-	20	ns
SCL Frequency	Tf_scl	-	100	400(3)	kHz
Hold time Start condition	Th_sta	-	4	-	µs
SDA Setup time	Tsu_dat	250	-	-	ns
SDA Hold time	Th_dat	0	-	-	
Low period of SCL	Tlow_scl	4.7	-	-	µs
High period of SCL	Thigh_scl	4.0	-	-	µs
Setup time for START	Tsu_sta	4.7	-	-	µs
Rise time of both SDA and SCL	Tr	1000	-	-	ns
Fall time of both SDA and SCL	Tf	300	-	-	ns
Setup time for STOP	Tsu_sto	4	-	-	µs
Bµs free time between STOP and Start	Tbuf	4.7	-	-	µs
PDM clock frequency	Tcyc_isam	-	1.024	4.096	MHz
PDM clock high width	Tisam_high	45%	-	55%	Tcyc_isam
PDM clock low width	Tisam_low	45%	-	55%	Tcyc_isam
PDM data setup time	Tsu_isam	50	-	-	ns
PDM data hold time	Th_isam	10	-	-	ns

Notes:

(1) Minimum timing is 2ms including HW internal reset and SW rest inside DSP based on the MCLK is 24.576MHz. Need to raise the timing if MCLK is less than 24.576MHz.
(2) Reference Figures 10 to 18 for PCM and IIS timing parameters
(3) SHI can support 1/25 MCLK rate in slave mode;maximum up to 400KHz.

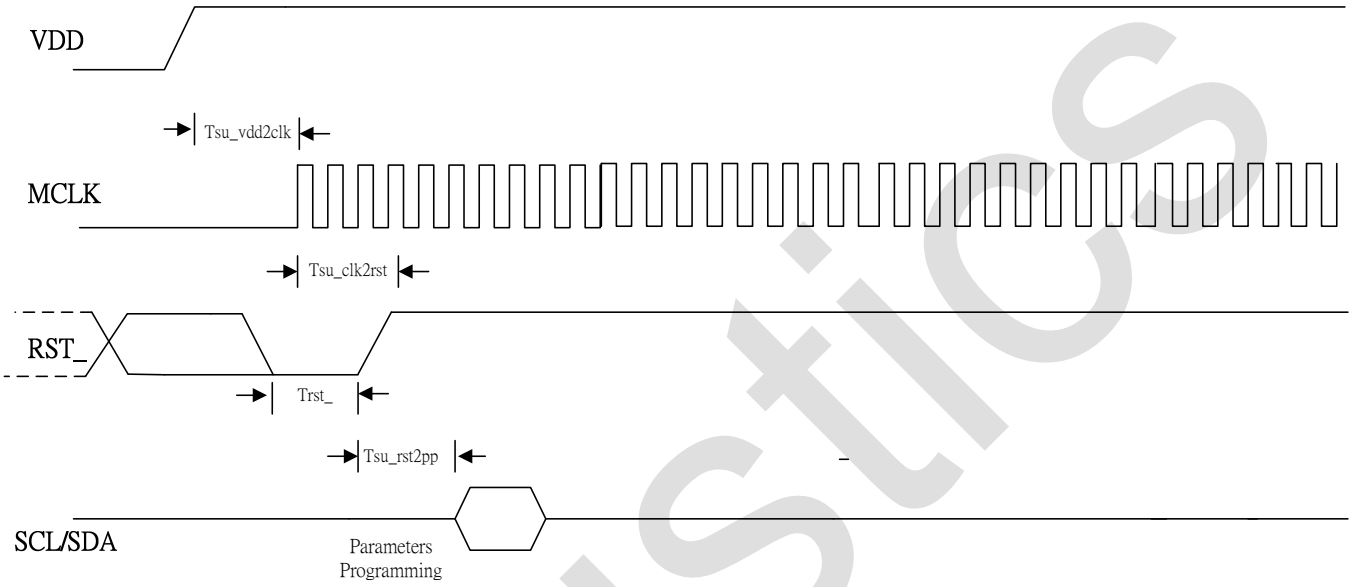


Figure 21: Power-up Initialization timing sequence

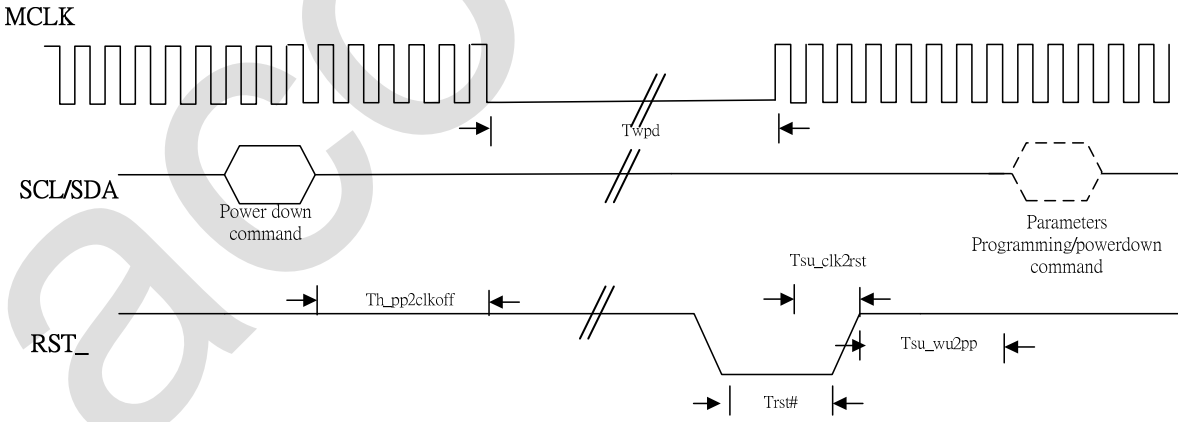


Figure 22: Power down to wake up(reset\resume) Timing

Note:

Power down **resume** mode no need to download the parameters after reset.
Power down **reset** mode need to download the parameters after reset.

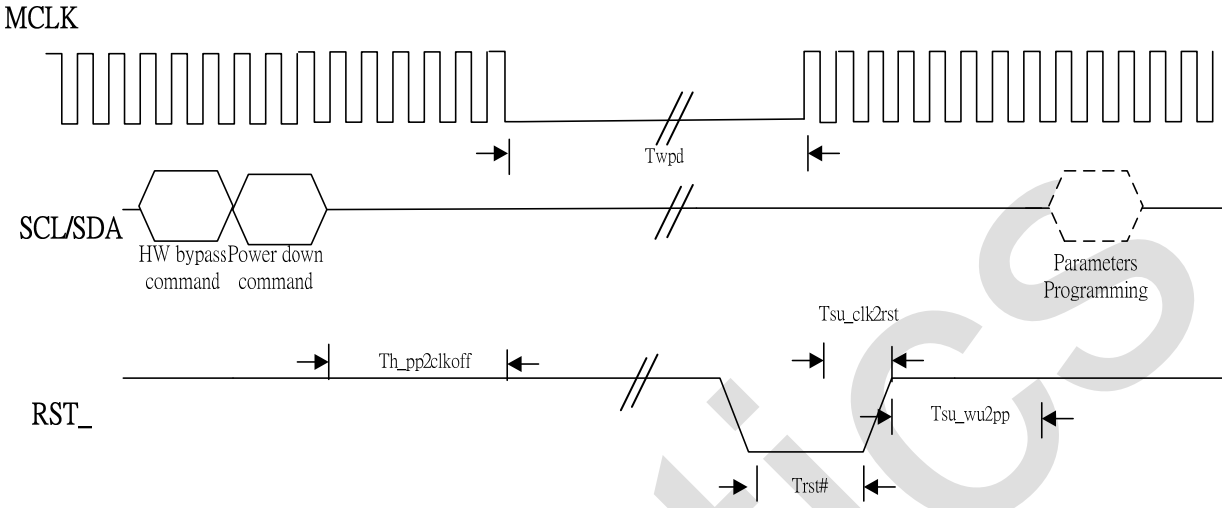


Figure 23: HW Bypass Timing

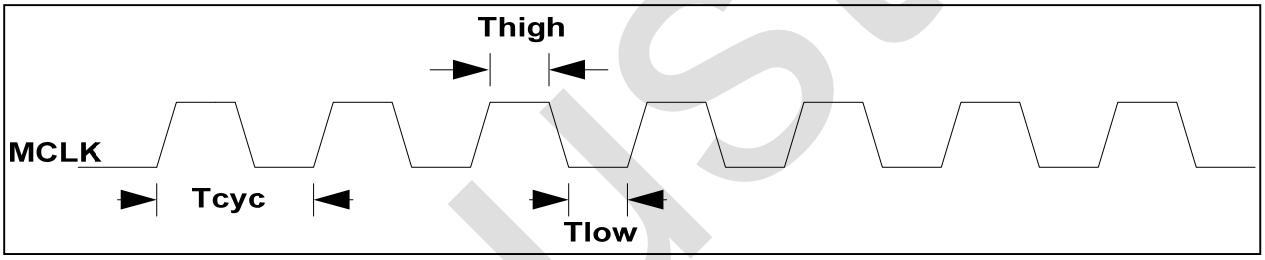


Figure 24: Master Clock (MCLK) Timing

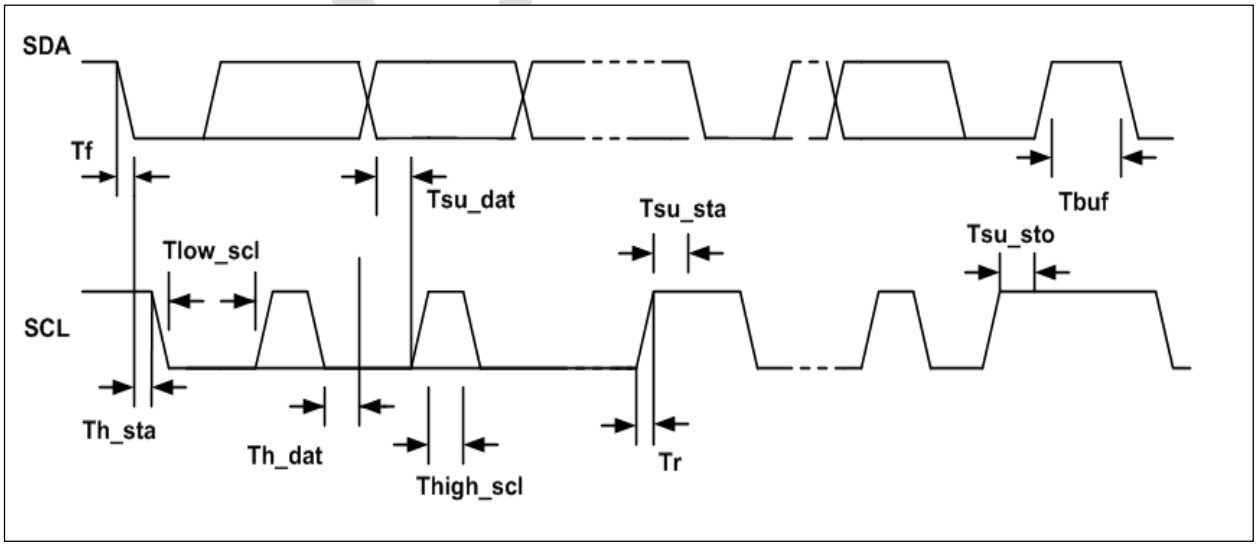


Figure 25: SHI Timing

4. Pin Definition Details

Table 9: CSP Pin Description

Pin#	Name	Type	Description	Electrical Capability
A1	I2S_DOUT0	Out	Transmit channel of serial port 0, 1, or 2. TX_0 can support up to 8 slots.	3.3V I/O tolerance, 6mA
A2	I2S_DOUT1	Out	This pin is a transmit channel of serial port. TX_1 can support up to 8 slots. The format of TX_1 can be selected among serial port 0, 1 or 2.	3.3V I/O tolerance, 6mA
A3	I2S_DIN1	In	This pin is a transmit channel of serial port. RX_1 can support up to 8 slots. The format of RX_1 can be selected among serial port 0, 1 or 2.	3.3V I/O tolerance
A4	I2S_DOUT2	Out	This pin can be configured as a transmit channel of serial port 0, 1, or 2, or PDM output channel.TX_2 can support up to 8 slots when configured as TX channel of serial port 0, 1, or 2.	3.3V I/O tolerance, 6mA
A5	DMIC_DIN0	In	PDM input data.	3.3V I/O tolerance
B1	I2S_BCLK0	In	BCLK_0 is bit clock of serial port 0.	3.3V I/O tolerance
B2	I2S_DIN0	In	Received channel of serial port 0, 1, or 2. RX_0 can support up to 8 slots.	3.3V I/O tolerance
B3	VSSD	GND	VSS for internal PLL and digital ground.	Ground
B4	DMIC_IN_CLK	Out	PDM clock of input data	3.3V I/O tolerance, 2mA
B5	MCLK	In	Master clock input. Rate of master clock can be multiple of 1MHz or 1.024MHz between 3~48Mhz. Also 3.684, 7.68, 14.4, 15.36, 16.8, 19.2, 19.68 and 44.1 MHz are also supported.	3.3V I/O tolerance
C1	I2S_LRCLK0	In	FRAME_0 is frame synchronization clock of serial port 0.	3.3V I/O tolerance
C2	VDD	Power	1.8V,2.5V, 3.3V I/O voltage supply.	1.8V recommended
C3	I2S_DIN2	In	This pin can be configured as a receive channel of serial port 0, 1, or 2, or PDM input.RX_2 can support up to 8 slots when configured as a receive channel of serial port 0, 1, or 2.	3.3V I/O tolerance

Pin#	Name	Type	Description	Electrical Capability
C4	DMIC_OUT_CLK	In/Out	PDM clock of PDM output data.	3.3V I/O tolerance, 2mA
C5	VDDC	Power	PLL and core power (double bonded with VDD) as internal LDO	Power as internal LDO(5)
D1	SDA	In/Out	SHI serial data.	3.3V I/O tolerance, Open drain, 4mA
D2	RST_	In	Master reset pin, active low. The minimum active duration is at least 1 ms.	3.3V I/O tolerance
D3	I2S_BCLK1	In	This pin can be configured as BCLK of serial port 1 or a receive channel of serial port. RX_4 only supports up to 2 slots. Format of RX_4 can be selected among serial port 0, 1, or 2.	3.3V I/O tolerance
D4	DMIC_OUT0	Out	PDM output data pin	3.3V I/O tolerance, 2mA
D5	DMIC_OUT1	In/Out	This pin can be configured as PDM data output, or general purpose IO.	3.3V I/O tolerance, 2mA
E1	SCL	In	Serial Host Interface Clock.	3.3V I/O tolerance
E2	I2S_LRCLK1	In	This pin can be configured as the FRAME SYNC input of serial Port 1 or the TX channel of serial port. TX_4 only supports up to 2 slots. Format of TX_4 can be selected among serial port 0, 1, or 2.	3.3VI/O tolerance, 6mA
E3	TEST	In	This pin is for test purpose only. Test pin is active high. Normal operation is in low state.	
E4	I2S_BCLK2	In	This pin can be configured as BCLK of serial port 2, RX channel of serial port 0, 1, or 2, or PDM input. RX_3 only support up to 2 slots when configured as a receive channel of serial port 0, 1, or 2. Or PDM data input.	3.3V I/O tolerance
E5	I2S_LRCLK2	In/Out	This pin can be configured as FRAME of serial port 2 or a transmit channel of serial port 0, 1, or 2. TX_3 can only support up to 2 slots. Format of TX_3 can be selected among serial port 0, 1, or 2. Or PDM data output.	3.3V I/O tolerance, 6mA

Notes:

(1) Legend:
IN – input pin
OUT – Output pin
IN/OUT – Input/Output bidirectional pin
PWR – Power pins as VDDs and VSSs of each digital power domain..

(2) Pad symbol is followed for reference.

(3) The unussed input pins should be connected to ground while the unused output pins should be left to unconnected. The unused I/O pins should be treated as input or output depending on its definition in system desgin.

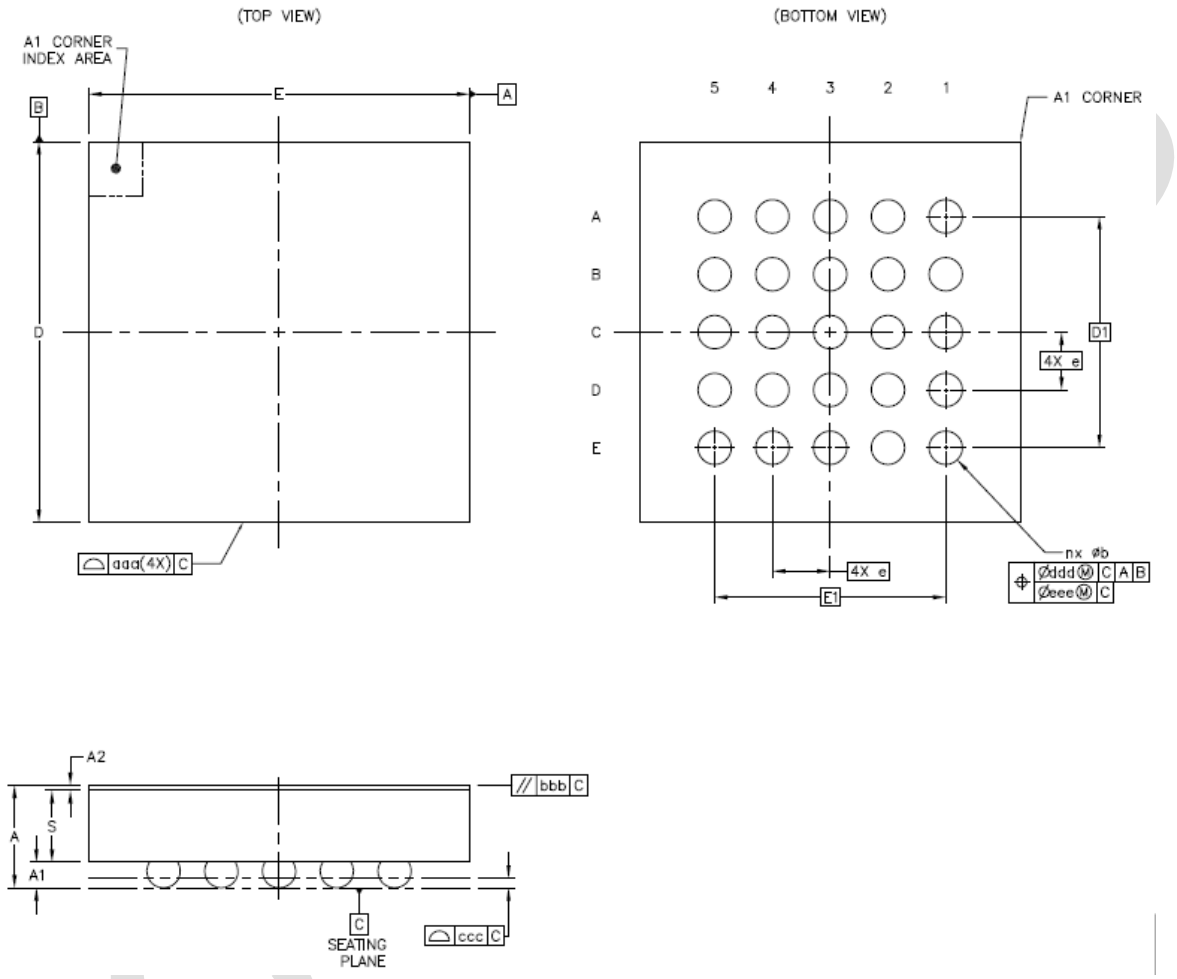
(4) It is recommended to keep all the input pins at low state during the power -off process to avoid any ESD leakage, but the random glitches are allowed.

(5) Please connect all VDDC with 0.1uF for high frequency and 2.2uF(10uF is the best) for power decoupling to ground

(6) This separate voltage source is designed to adapt to the level of the digital I/O interface voltage level; it can either be 1.8V, 2.5V, or 3.3V, depending on the interface logic level

5. Package Dimensions

NR2048 Top View, Bottom View and Side View



Description	Symbol	Dimension			unit
		Min	Nominal		
IC Length	E	2956	2966	2976	µm
IC Width	D	2956	2966	2976	µm
Pitch	e		450		µm
Edge ball center to center (X)	E1		1800		µm
Edge ball center to center (Y)	D1		1800		µm
Ball Size	b	230	260	290	µm
Height IC + Bump + Backside Coating	A	768	798	828	µm
Height IC	S	533		598	µm
Bump Height	A1	170	200	230	µm
Backside Coating	A2	15		44	µm

Figure 26: 25-ball WLCSP Package Dimensions