

## Features

- Advanced Split Gate Trench Technology
- Excellent RDS(ON) and Low Gate Charge
- Lead free product is acquired

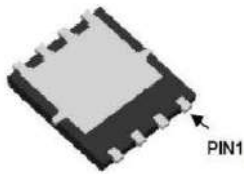
## Application

- Load Switch
- PWM Application
- Power management

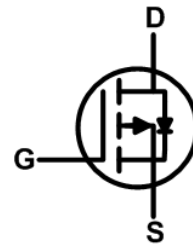
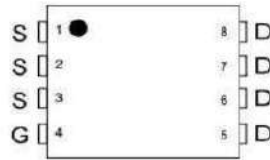
## Product Summary



$V_{DS}$	-100	V
$R_{DS(on), Typ @ V_{GS} = -10 V}$	34	mΩ
$I_D$	-40	A



DFN5\*6-8



P-Channel

## Absolute Maximum Ratings ( $T_C = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Max.	Units
$V_{DSS}$	Drain-Source Voltage	-100	V
$V_{GSS}$	Gate-Source Voltage	$\pm 20$	V
$I_D$	Continuous Drain Current	$T_C = 25^\circ\text{C}$	-40
		$T_C = 100^\circ\text{C}$	-16
$I_{DM}$	Pulsed Drain Current <sup>note1</sup>	-160	A
$E_{AS}$	Single Pulsed Avalanche Energy <sup>note2</sup>	81	mJ
$P_D$	Power Dissipation	$T_C = 25^\circ\text{C}$	54
$R_{\theta JC}$	Thermal Resistance, Junction to Case	2.3	$^\circ\text{C/W}$
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$

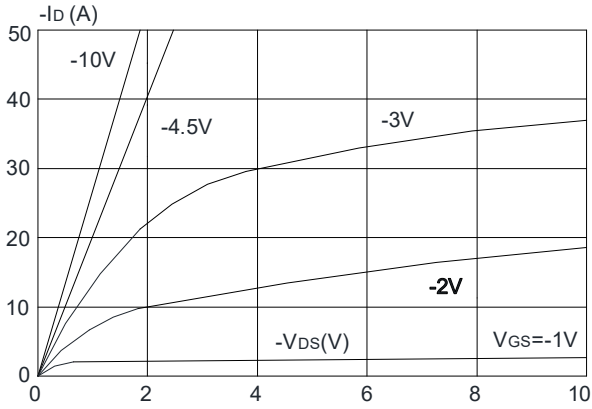
**Electrical Characteristics** ( $T_J=25^{\circ}\text{C}$  unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
<b>Off Characteristic</b>						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=-250\mu A$	-100	-	-	V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS}=-100V, V_{GS}=0V,$	-	-	-1.0	$\mu A$
$I_{GSS}$	Gate to Body Leakage Current	$V_{DS}=0V, V_{GS}=\pm 20V$	-	-	$\pm 100$	nA
<b>On Characteristics</b>						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=-250\mu A$	-1.0	-1.4	-2.5	V
$R_{DS(on)}$	Static Drain-Source on-Resistance <small>note3</small>	$V_{GS}=-10V, I_D=-20A$	-	34	52	m $\Omega$
		$V_{GS}=-4.5V, I_D=-10A$	-	38	60	
<b>Dynamic Characteristics</b>						
$C_{iss}$	Input Capacitance	$V_{DS}=-50V, V_{GS}=0V,$ $f=1.0MHz$	-	1458	-	pF
$C_{oss}$	Output Capacitance		-	133	-	pF
$C_{riss}$	Reverse Transfer Capacitance		-	8.9	-	pF
$Q_g$	Total Gate Charge	$V_{DS}=-50V, I_D=-5A,$ $V_{GS}=-10V$	-	40	-	nC
$Q_{gs}$	Gate-Source Charge		-	7.8	-	nC
$Q_{gd}$	Gate-Drain("Miller") Charge		-	8.6	-	nC
<b>Switching Characteristics</b>						
$t_{d(on)}$	Turn-on Delay Time	$V_{DD}=-50V, I_D=-5A,$ $R_G=6\Omega, V_{GS}=-10V$	-	13	-	ns
$t_r$	Turn-on Rise Time		-	39	-	ns
$t_{d(off)}$	Turn-off Delay Time		-	100.1	-	ns
$t_f$	Turn-off Fall Time		-	105.3	-	ns
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
$I_S$	Maximum Continuous Drain to Source Diode Forward Current		-	-	-40	A
$I_{SM}$	Maximum Pulsed Drain to Source Diode Forward Current		-	-	-160	A
$V_{SD}$	Drain to Source Diode Forward Voltage	$V_{GS}=0V, I_S=-25A$	-	-	-1.2	V
$t_{rr}$	Body Diode Reverse Recovery Time	$T_J=25^{\circ}\text{C},$ $I_F=-5A, di/dt=100A/\mu s$	-	104	-	ns
$Q_{rr}$	Body Diode Reverse Recovery Charge		-	280	-	nC

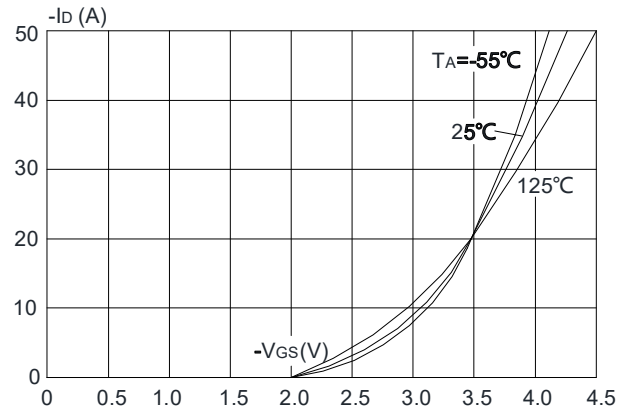
- Notes: 1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature  
 2. EAS condition:  $T_J=25^{\circ}\text{C}, V_{DD}=-50V, V_G=-10V, R_G=25\Omega, L=0.5mH, I_{AS}=-18A$   
 3. Pulse Test: Pulse Width $\leq 300\mu s$ , Duty Cycle $\leq 0.5\%$

**Typical Performance Characteristics**

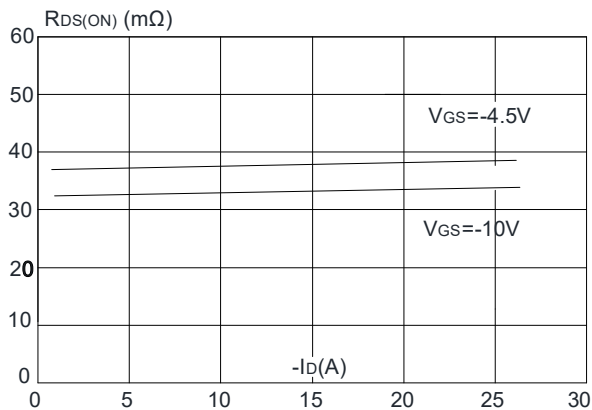
**Figure 1: Output Characteristics**



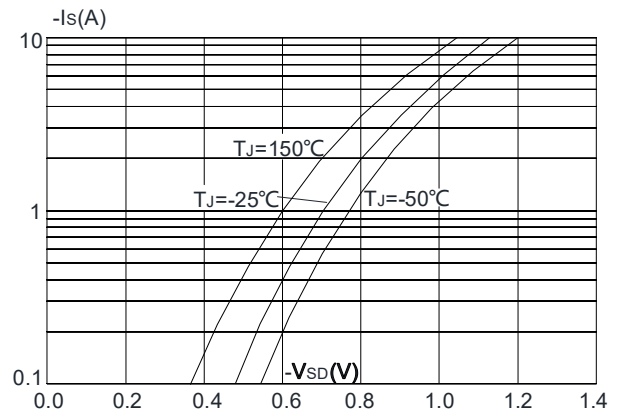
**Figure 2: Typical Transfer Characteristics**



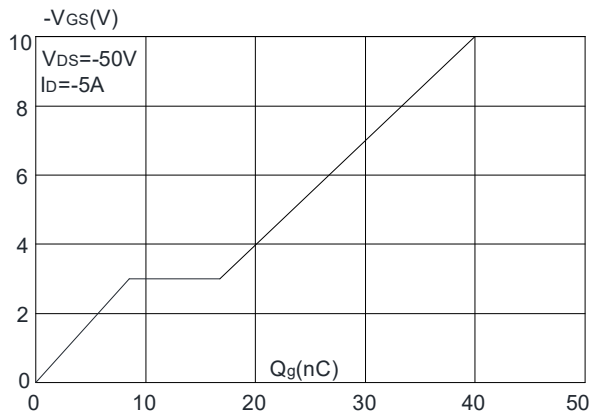
**Figure 3: On-resistance vs. Drain Current**



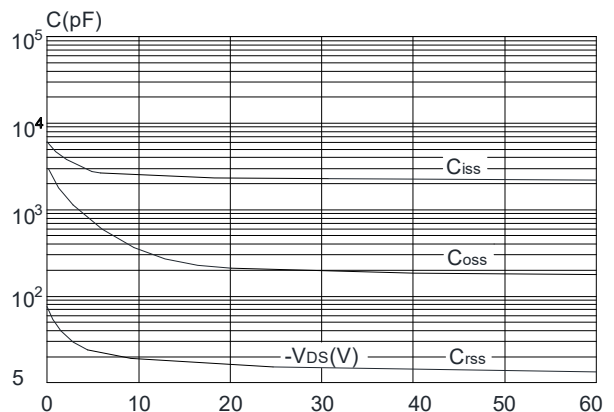
**Figure 4: Body Diode Characteristics**



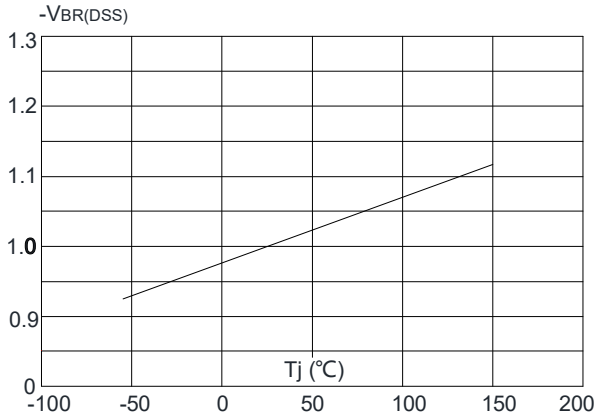
**Figure 5: Gate Charge Characteristics**



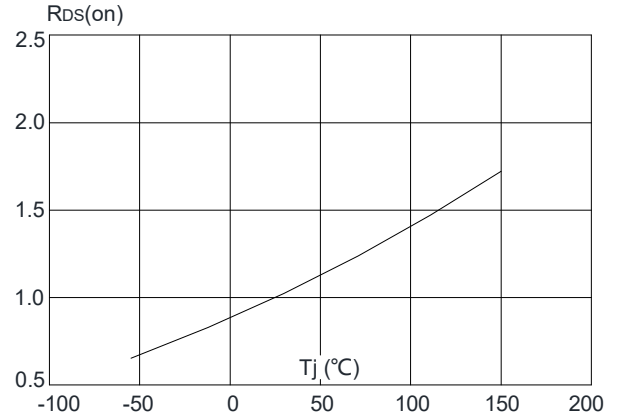
**Figure 6: Capacitance Characteristics**



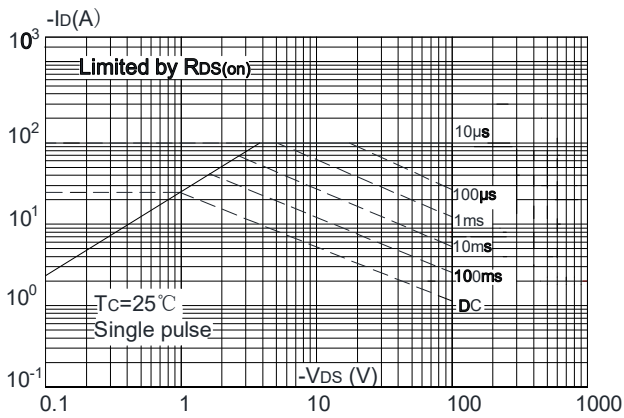
**Figure 7: Normalized Breakdown Voltage vs. Junction Temperature**



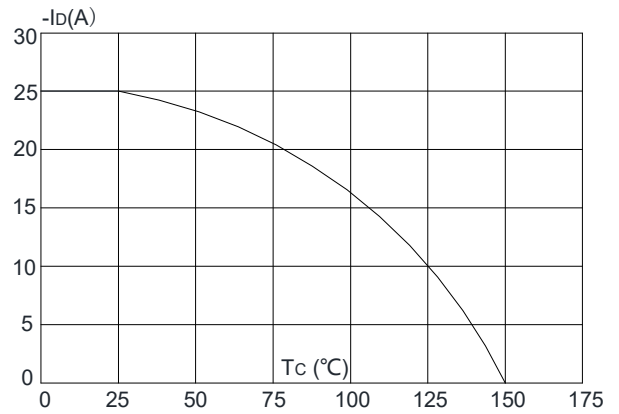
**Figure 8: Normalized on Resistance vs. Junction Temperature**



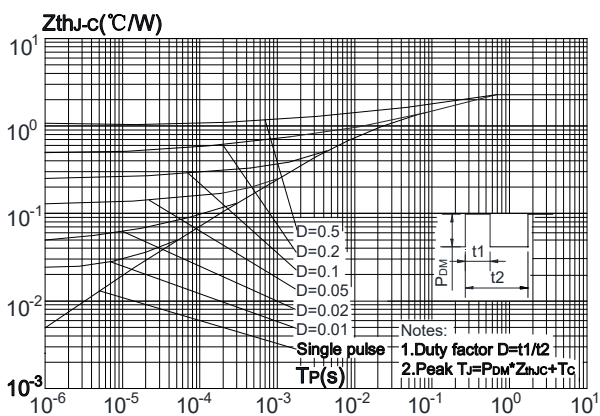
**Figure 9: Maximum Safe Operating Area**



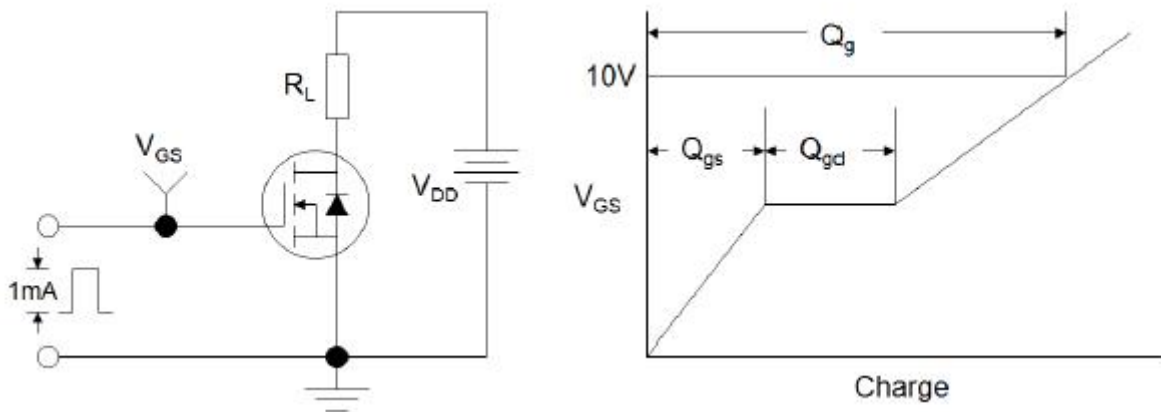
**Figure 10: Maximum Continuous Drain Current vs. Case Temperature**



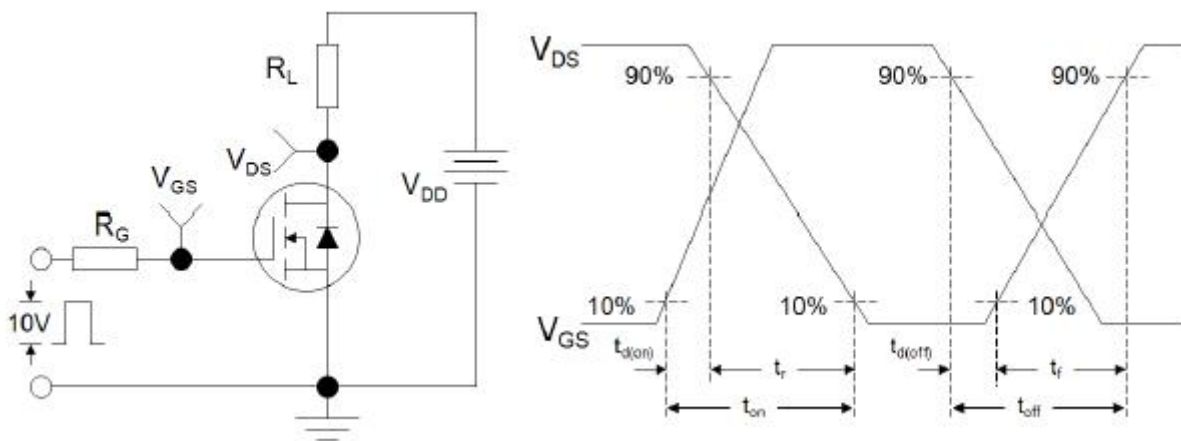
**Figure.11: Maximum Effective Transient Thermal Impedance, Junction-to-Case**



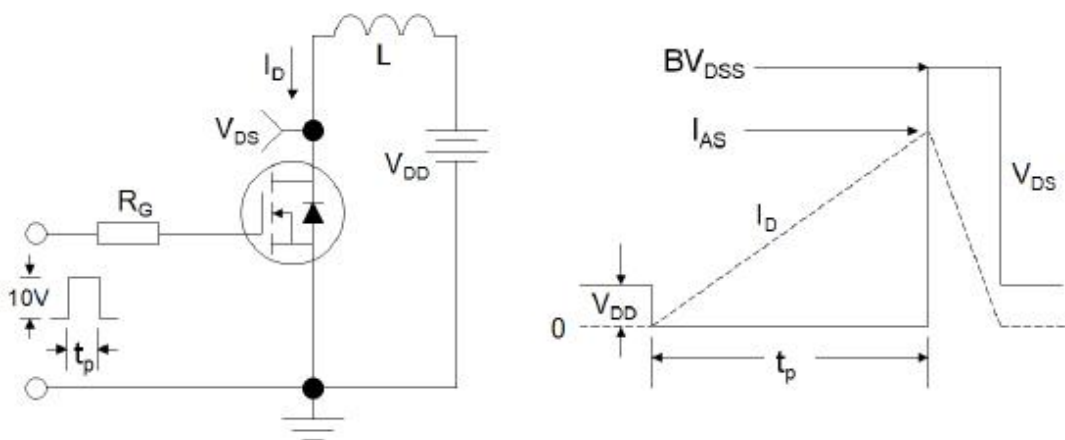
**Test Circuit**



**Figure1:Gate Charge Test Circuit & Waveform**



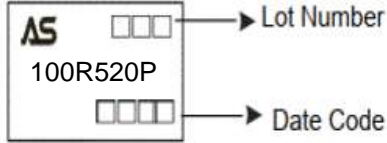
**Figure 2: Resistive Switching Test Circuit & Waveforms**

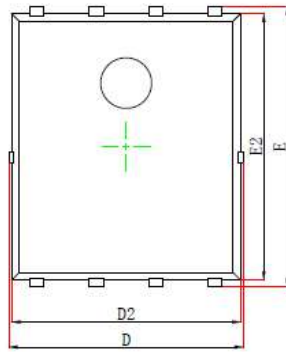
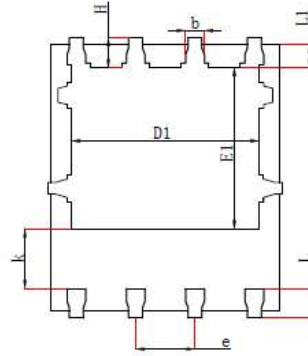
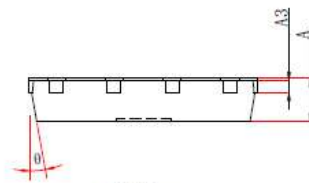


**Figure 3:Unclamped Inductive Switching Test Circuit & Waveforms**

## Ordering and Marking Information

Ordering Device No.	Marking	Package	Packing	Quantity
ASDM100R520PQ-R	100R520P	DFN5*6-8	Tape&Reel	4000/Reel

PACKAGE	MARKING
DFN5*6-8	 <p>The marking diagram shows a rectangular package with the following markings: 'AS' logo, '100R520P', and two sets of four squares. Arrows point from the top set of squares to 'Lot Number' and from the bottom set of squares to 'Date Code'.</p>

**DFN5x6\_P, 8 Leads**

**Top View**  
 [顶视图]

**Bottom View**  
 [背视图]

**Side View**  
 [侧视图]

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.000	0.035	0.039
A3	0.254REF.		0.010REF.	
D	4.944	5.096	0.195	0.201
E	5.974	6.126	0.235	0.241
D1	3.910	4.110	0.154	0.162
E1	3.375	3.575	0.133	0.141
D2	4.824	4.976	0.190	0.196
E2	5.674	5.826	0.223	0.229
k	1.190	1.390	0.047	0.055
b	0.350	0.450	0.014	0.018
e	1.270TYP.		0.050TYP.	
L	0.559	0.711	0.022	0.028
L1	0.424	0.576	0.017	0.023
H	0.574	0.726	0.023	0.029
θ	10°	12°	10°	12°

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