ASDM80R055NTD

80V N-Channel MOSFET

Features

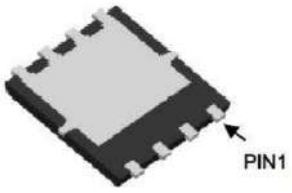
- Optimized for chargers
- 100% avalanche tested
- Superior thermal resistance
- N-channel, Logic level
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21
- Ideal for high-frequency switching

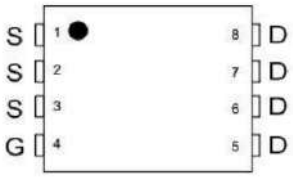
Product Summary

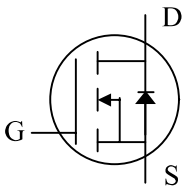
V_{DSS}	80	V
$R_{DS(ON)-Typ@VGS=10V}$	5.4	mΩ
I_D	40	A

Product validation

Qualified according to JEDEC Standard







DFN3*3-8

Maximum ratings at T_A=25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current	I_D	- - -	- - -	40 40 14	A	V_{GS}=10 V, T_C=25 °C V_{GS}=10 V, T_C=100 °C V_{GS}=10 V, T_A=25 °C, R_{thJA} =60K/W[1)]
Pulsed drain current[2)]	$I_{D,pulse}$	-	-	160	A	T_C=25 °C
Avalanche energy, single pulse[3)]	E_{AS}	-	-	38	mJ	I_D=20 A, R_{GS}=25 Ω
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	- -	- -	46 2.1	W	T_C=25 °C T_A=25 °C, R_{thJA}=60 K/W[1)]
Operating and storage temperature	T_j, T_{stg}	-55	-	150	°C	IEC climatic category; DIN IEC 68-1: 55/150/56

Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	1.6	2.7	K/W	-
Device on PCB, minimal footprint	R_{thJA}	-	-	62	K/W	-
Device on PCB, 6 cm^2 cooling area[1)]	R_{thJA}	-	-	60	K/W	-

Electrical characteristics at T_j=25 °C, unless otherwise specified

Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	80	-	-	V	V_{GS}=0 V, I_D=1 mA
Gate threshold voltage	$V_{GS(th)}$	1.1	1.7	2.3	V	V_{DS}=V_{GS}, I_D=20 µA
Zero gate voltage drain current	I_{DSS}	- -	0.1 10	1 100	µA	V_{DS}=80 V, V_{GS}=0 V, T_j=25 °C V_{DS}=80 V, V_{GS}=0 V, T_j=125 °C
Gate-source leakage current	I_{GSS}	-	10	100	nA	V_{GS}=20 V, V_{DS}=0 V
Drain-source on-state resistance	$R_{DS(on)}$	- -	5.4 7.3	6.5 9.4	mΩ	V_{GS}=10 V, I_D=20 A V_{GS}=4.5 V, I_D=10 A
Gate resistance[1)]	R_G	-	1.2	1.8	Ω	-
Transconductance	g_{fs}	25	50	-	S	$\|V_{DS}\|>2\|I_D\|R_{DS(on)max}$, I_D=20 A

Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance[1)]	C_{iss}	-	1400	1800	pF	V_{GS}=0 V, V_{DS}=40 V, f=1 MHz
Output capacitance[1)]	C_{oss}	-	300	390	pF	V_{GS}=0 V, V_{DS}=40 V, f=1 MHz
Reverse transfer capacitance[1)]	C_{rss}	-	16	28	pF	V_{GS}=0 V, V_{DS}=40 V, f=1 MHz
Turn-on delay time	$t_{d(on)}$	-	5.0	-	ns	V_{DD}=40 V, V_{GS}=10 V, I_D=20 A, $R_{G,ext}$=1.6 Ω
Rise time	t_r	-	2.9	-	ns	V_{DD}=40 V, V_{GS}=10 V, I_D=20 A, $R_{G,ext}$=1.6 Ω
Turn-off delay time	$t_{d(off)}$	-	14	-	ns	V_{DD}=40 V, V_{GS}=10 V, I_D=20 A, $R_{G,ext}$=1.6 Ω
Fall time	t_f	-	2.6	-	ns	V_{DD}=40 V, V_{GS}=10 V, I_D=20 A, $R_{G,ext}$=1.6 Ω

Gate charge characteristics[2)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	4.1	-	nC	V_{DD}=40 V, I_D=20 A, V_{GS}=0 to 4.5 V
Gate charge at threshold	$Q_{g(th)}$	-	2.3	-	nC	V_{DD}=40 V, I_D=20 A, V_{GS}=0 to 4.5 V
Gate to drain charge[1)]	Q_{gd}	-	3.3	4.9	nC	V_{DD}=40 V, I_D=20 A, V_{GS}=0 to 4.5 V
Switching charge	Q_{sw}	-	5.1	-	nC	V_{DD}=40 V, I_D=20 A, V_{GS}=0 to 4.5 V
Gate charge total[1)]	Q_g	-	10	13	nC	V_{DD}=40 V, I_D=20 A, V_{GS}=0 to 4.5 V
Gate plateau voltage	$V_{plateau}$	-	2.9	-	V	V_{DD}=40 V, I_D=20 A, V_{GS}=0 to 4.5 V
Gate charge total, sync. FET	$Q_{g(sync)}$	-	18	-	nC	V_{DS}=0.1 V, V_{GS}=0 to 10 V
Output charge[1)]	Q_{oss}	-	19	26	nC	V_{DD}=40 V, V_{GS}=0 V

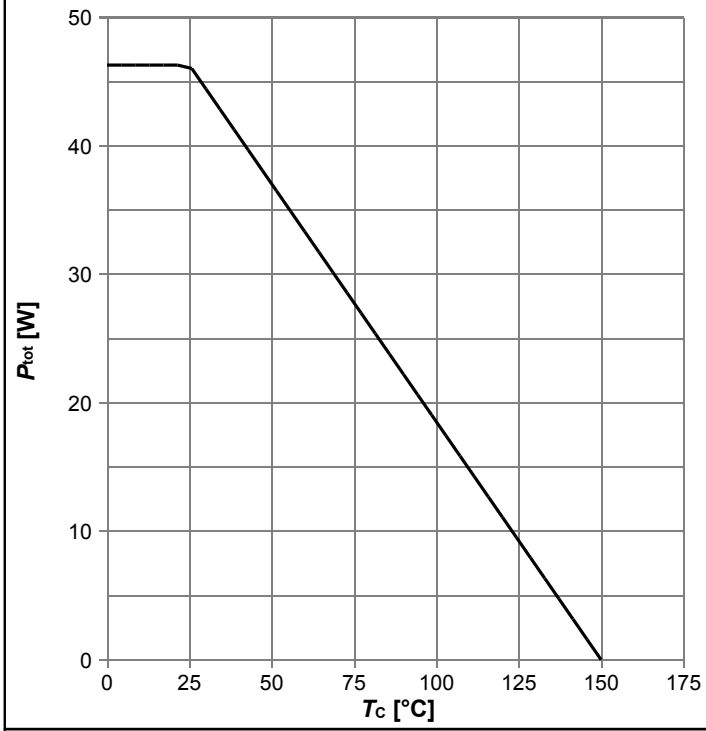
[1)] Defined by design. Not subject to production test
[2)] See ″Gate charge waveforms″ for parameter definition

Reverse diode

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	39	A	T_C=25 °C
Diode pulse current	$I_{S,pulse}$	-	-	156	A	T_C=25 °C
Diode forward voltage	V_{SD}	-	0.83	1.2	V	V_{GS}=0 V, I_F=20 A, T_j=25 °C
Reverse recovery time[1)]	t_{rr}	-	18	36	ns	V_R=40 V, I_F=20 *A*, di_F/dt=100 A/μs
Reverse recovery charge[1)]	Q_{rr}	-	7	14	nC	V_R=40 V, I_F=20 *A*, di_F/dt=100 A/μs

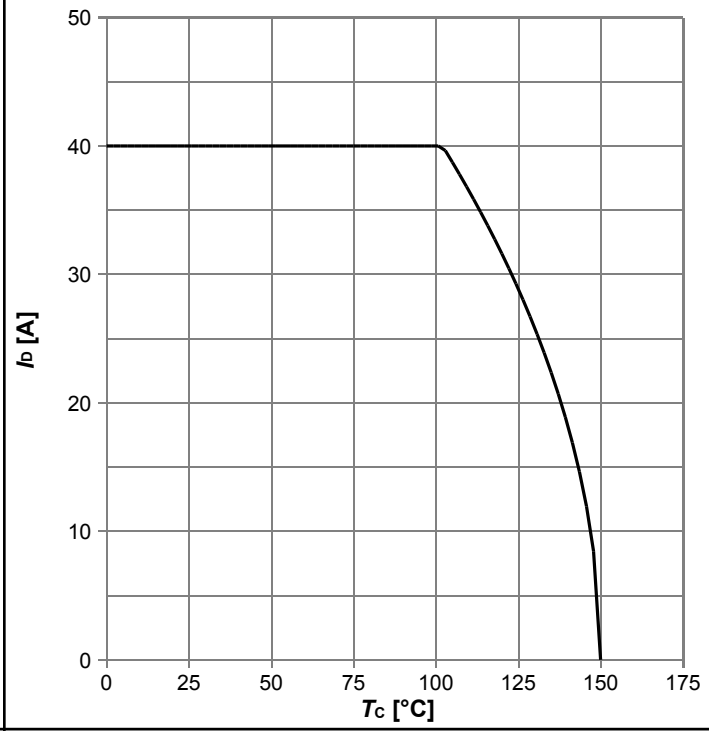
Electrical characteristics diagrams

Diagram 1: Power dissipation



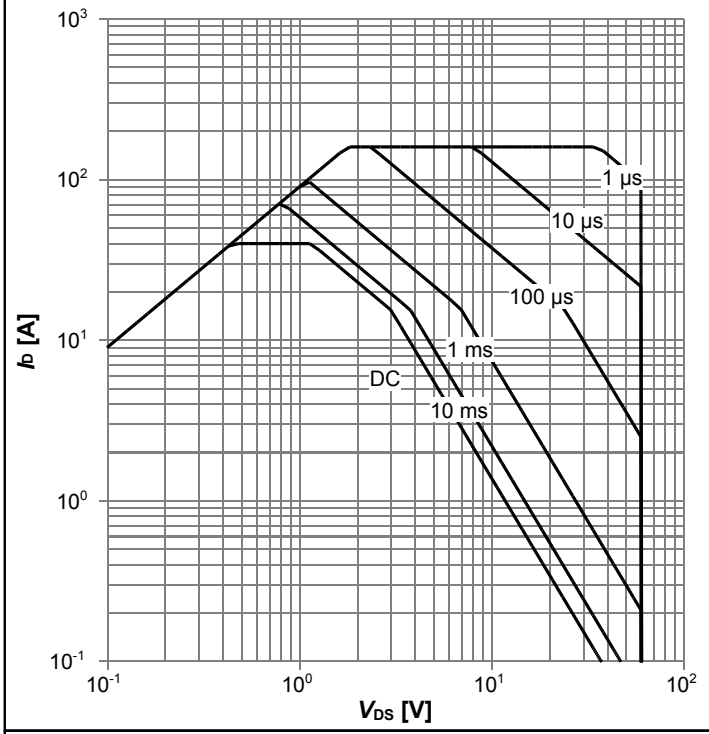
$P_{tot}=f(T_C)$

Diagram 2: Drain current



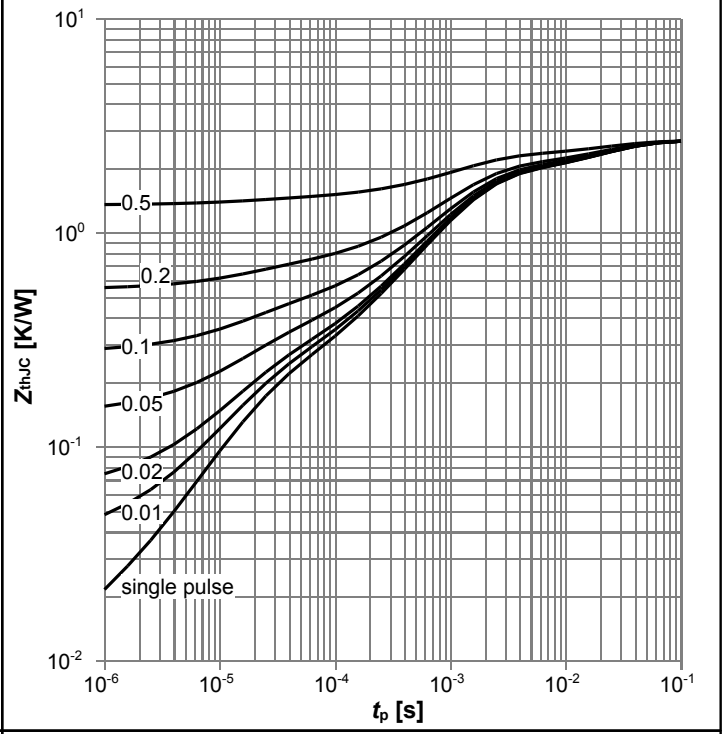
$I_D=f(T_C)$; $V_{GS}\geq 10$ V

Diagram 3: Safe operating area



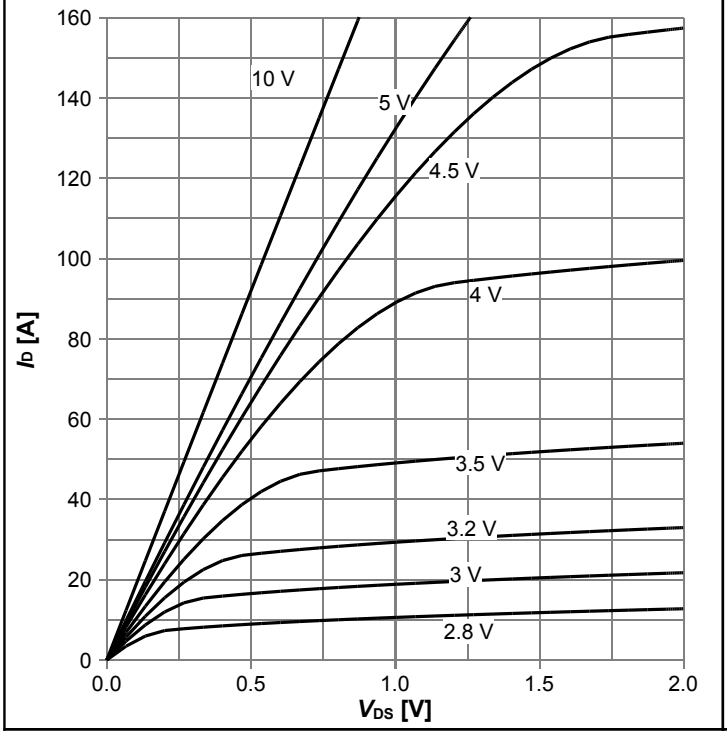
$I_D=f(V_{DS})$; $T_C=25$ °C; $D=0$; parameter: t_p

Diagram 4: Max. transient thermal impedance



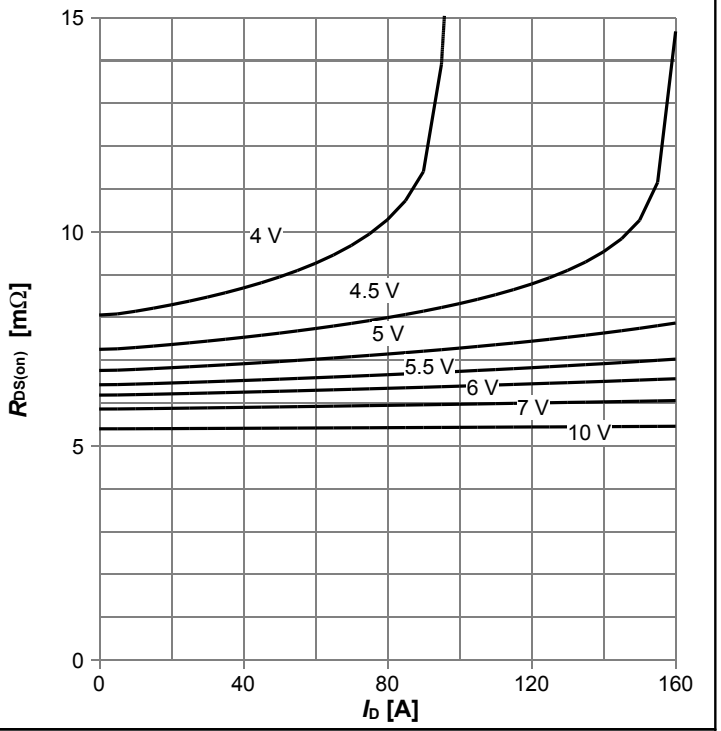
$Z_{thJC}=f(t_p)$; parameter: $D=t_p/T$

Diagram 5: Typ. output characteristics



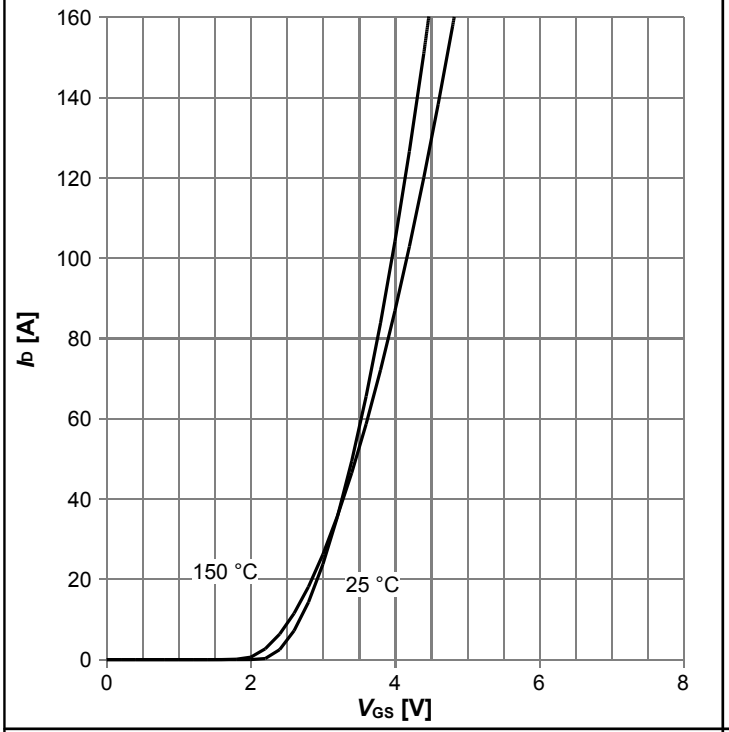
I_D=f(V_{DS}); T_j=25 °C; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



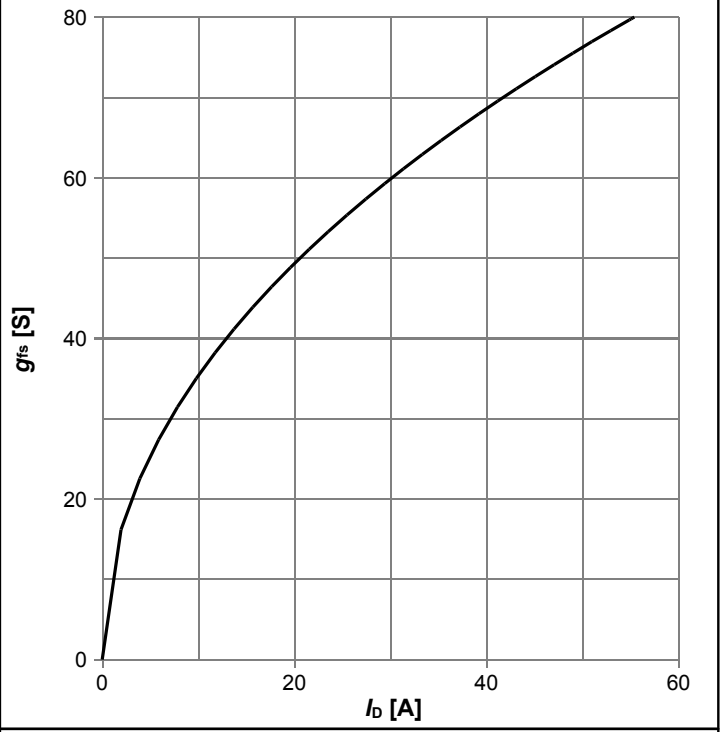
$R_{DS(on)}$=f(I_D); T_j=25 °C; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



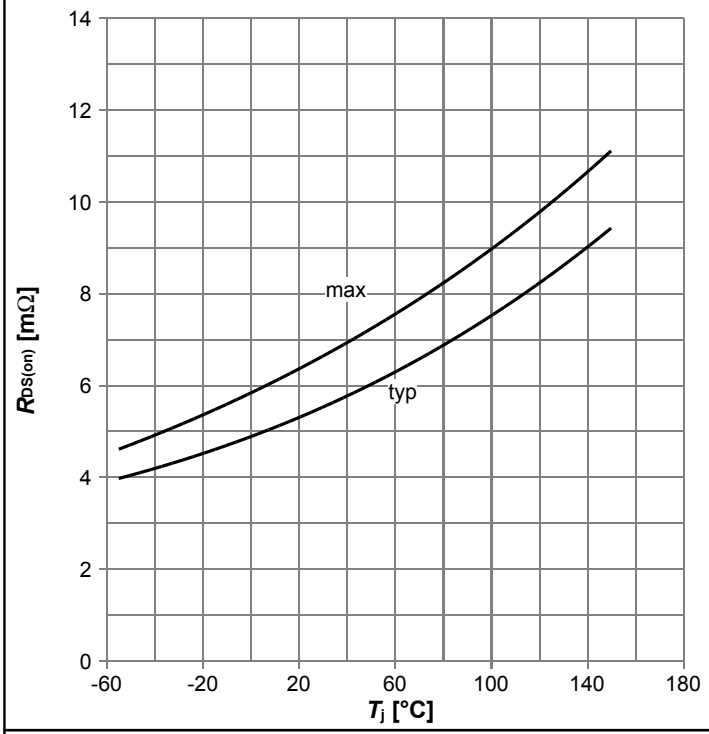
I_D=f(V_{GS}); |V_{DS}|>2|I_D|$R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. forward transconductance



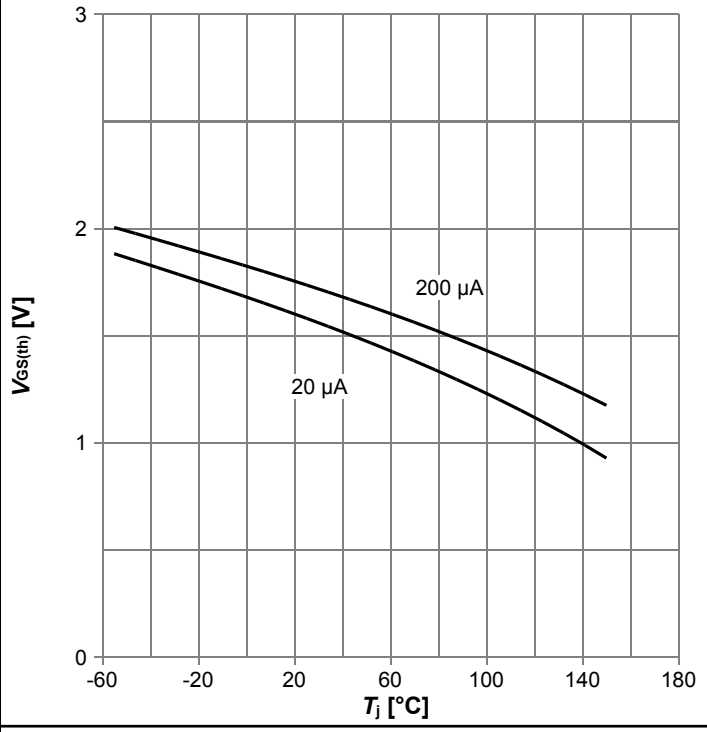
g_{fs}=f(I_D); T_j=25 °C

Diagram 9: Drain-source on-state resistance



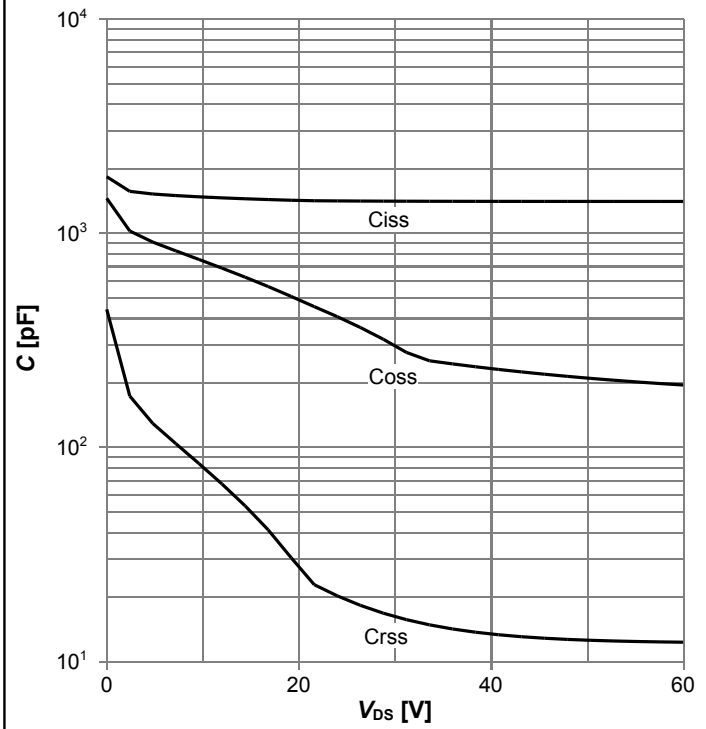
$R_{DS(on)}$=f(T_j); I_D=20 A; V_{GS}=10 V

Diagram 10: Typ. gate threshold voltage



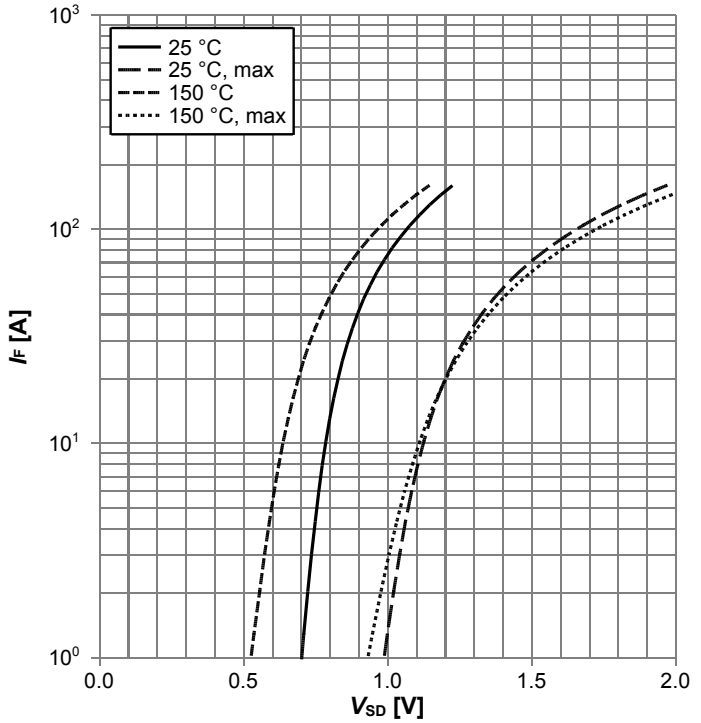
$V_{GS(th)}$=f(T_j); V_{GS}=V_{DS}

Diagram 11: Typ. capacitances



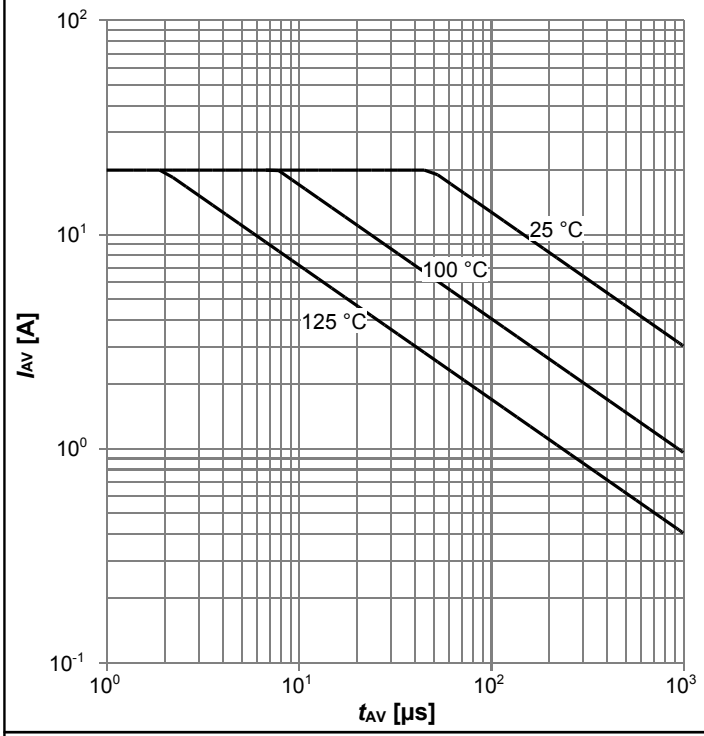
C=f(V_{DS}); V_{GS}=0 V; f=1 MHz

Diagram 12: Forward characteristics of reverse diode



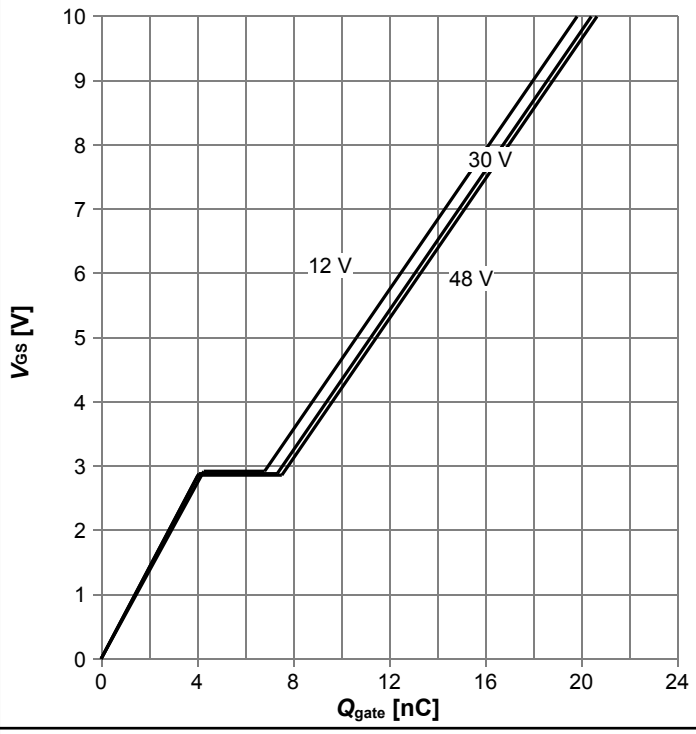
I_F=f(V_{SD}); parameter: T_j

Diagram 13: Avalanche characteristics



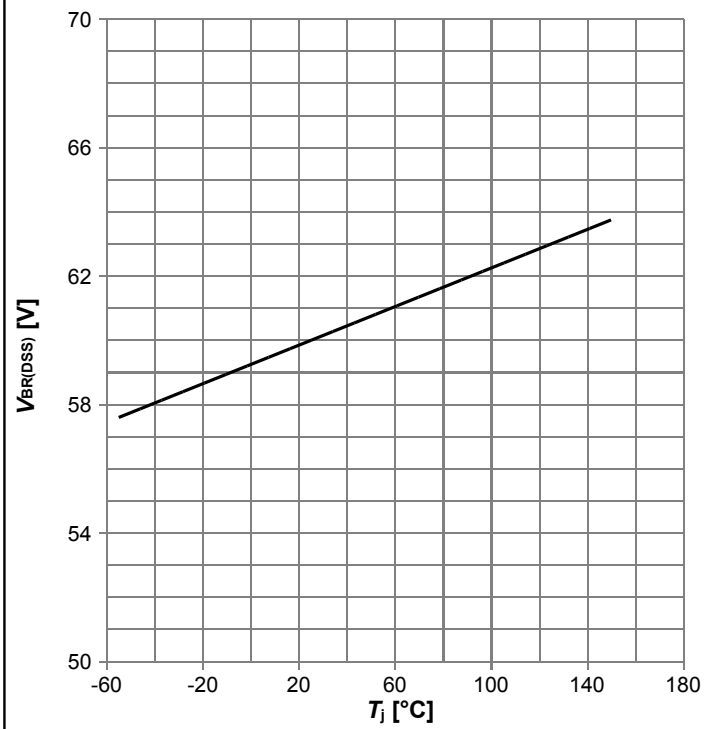
$I_{AS}=f(t_{AV})$; $R_{GS}=25\ \Omega$; parameter: $T_{j(start)}$

Diagram 14: Typ. gate charge



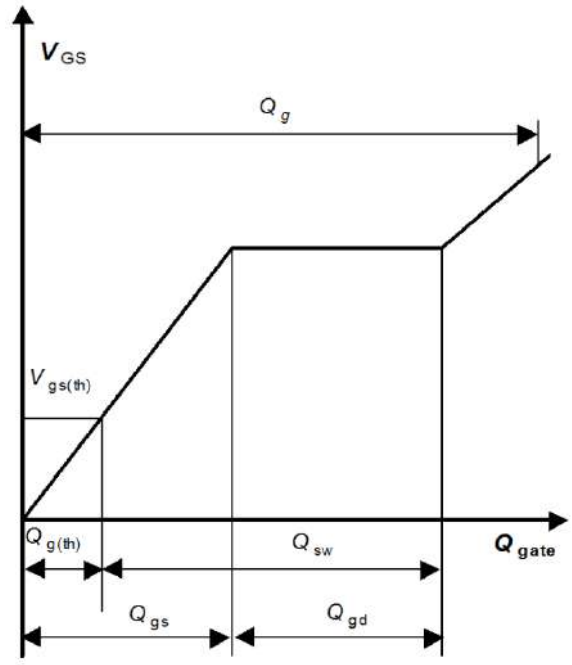
$V_{GS}=f(Q_{gate})$; $I_D=20$ A pulsed; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage



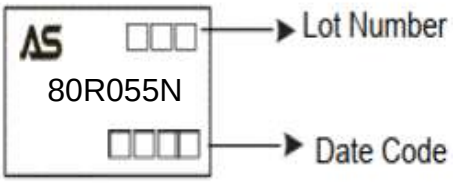
$V_{BR(DSS)}=f(T_j)$; $I_D=1$ mA

Diagram Gate charge waveforms



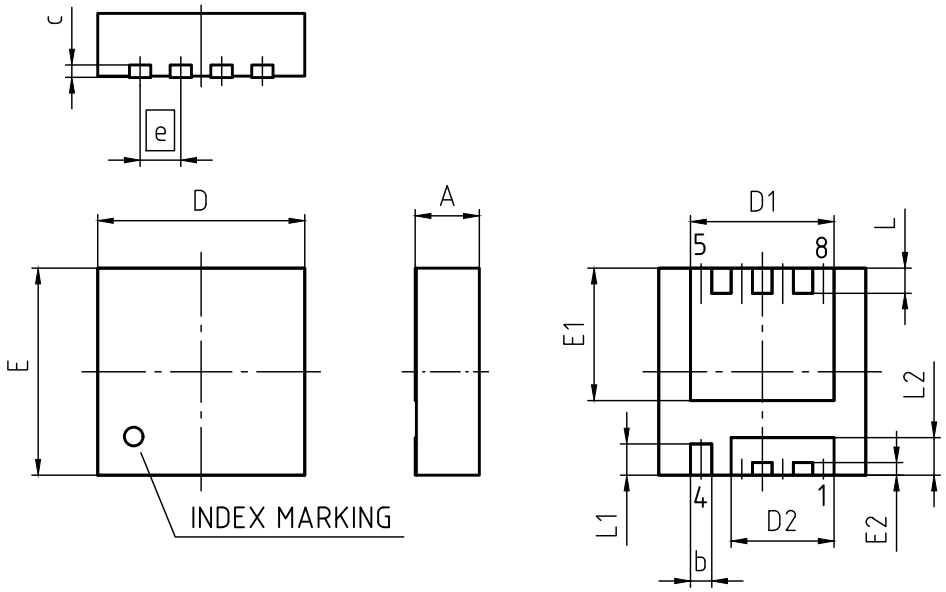
Ordering and Marking Information

Ordering Device No.	Marking	Package	Packing	Quantity
ASDM80R055NTD-R	80R055N	DFN3*3-8	Tape&Reel	5000/Reel

PACKAGE	MARKING
DFN3*3-8	

Package Outlines

DFN3*3-8



PACKAGE - GROUP NUMBER:	PG-TSDSON-8-U03	
REVISION: 03	DATE: 20.10.2020	
DIMENSIONS	**MILLIMETERS**	
	MIN.	MAX.
A	0.90	1.10
b	0.24	0.44
c	(0.20)	
D	3.20	3.40
D1	2.19	2.39
D2	1.54	1.74
E	3.20	3.40
E1	2.01	2.21
E2	0.10	0.30
e	0.65	
L	0.30	0.50
L1	0.40	0.60
L2	0.50	0.70
aaa	0.06	

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