Features

- High Efficiency
- Low Dense Cell Design
- Advanced trench process technology
- improved dv/dt capability
- Reliable and Rugged

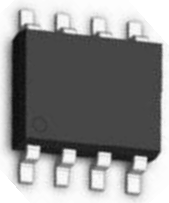
Application

- Networking, Load Swtich
- LED lighting

Product Summary

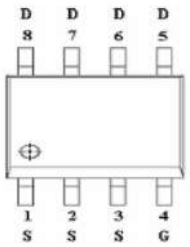
V_{DS}	30	V
$R_{DS(on),Typ}$@ V_{GS} =10 V	8.1	mΩ
I_D	13	A

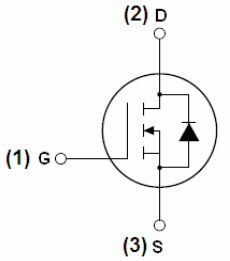
top view



SOP-8

Simplified Outline





Absolute Maximum Ratings at T_j=25℃ (unless otherwise specified)

Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current	T_A=25℃	I_D	13	A
	T_A=70℃		10.4	
Pulsed Drain Current [C]		I_{DM}	52	
Avalanche Current [C]		I_{AS}	13	A
Avalanche energy L=0.1mH [C]		E_{AS}	24	mJ
Power Dissipation [B]	T_A=25℃	P_D	3.1	W
	T_A=70℃		2	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	℃

Thermal Characteristics					
Parameter		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	31	40	℃/W
Maximum Junction-to-Ambient [A D]	Steady-State		59	75	℃/W
Maximum Junction-to-Lead	Steady-State	$R_{\theta JL}$	16	24	℃/W

Electrical Characteristics (T_J=25℃ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=250μA, V_{GS}=0V	30	--	--	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=30V, V_{GS}=0V	--	--	1	μA
		T_J=85°C	--	--	30	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}=±20V	--	--	±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS} I_D=250μA	1.0	1.4	2.0	V
$I_{D(ON)}$	On state drain current	V_{GS}=10V, V_{DS}=5V	100	--	--	A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V, I_D=12A	--	8.1	11.5	mΩ
		T_J=125℃	--	12	15	
		V_{GS}=4.5V, I_D=10A	--	12.6	14	mΩ
g_{FS}	Forward Transconductance	V_{DS}=5V, I_D=12A	--	45	--	S
V_{SD}	Diode Forward Voltage	I_S=1A,V_{GS}=0V	--	0.75	1	V
I_S	Maximum Body-Diode Continuous Current		--	--	13	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=15V, f=1MHz	610	760	910	pF
C_{oss}	Output Capacitance		88	125	160	pF
C_{rss}	Reverse Transfer Capacitance		40	70	100	pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz	0.8	1.6	2.4	Ω
SWITCHING PARAMETERS						
Q_g(10V)	Total Gate Charge	V_{GS}=10V, V_{DS}=15V, I_D=12A	11	14	17	nC
Q_g(4.5V)	Total Gate Charge		5	6.6	8	nC
Q_{gs}	Gate Source Charge		1.9	2.4	2.9	nC
Q_{gd}	Gate Drain Charge		1.8	3	4.2	nC
Q_{gs}	Gate Source Charge	V_{GS}=4.5V, V_{DS}=15V, I_D=12A	1.9	2.4	2.9	nC
Q_{gd}	**Gate Drain Charge**		**1.8**	**3**	**4.2**	**nC**
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=10V, V_{DS}=15V, R_L=1.25Ω, R_{GEN}=3Ω	--	4.4	--	ns
t_r	Turn-On Rise Time		--	9	--	ns
$t_{D(off)}$	Turn-Off DelayTime		--	17	--	ns
t_f	Turn-Off Fall Time		--	6	--	ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=12A, dI/dt=500A/μs	5.6	7	8	ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=12A, dI/dt=500A/μs	6.4	8	9.6	nC

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A =25° C. The value in any given application depends on the user's specific board design.
B. The power dissipation P_D is based on $T_{J(MAX)}$=150° C, using ≤ 10s junction-to-ambient thermal resistance.
C. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150° C. Ratings are based on low frequency and duty cycles to keep initialT_J=25° C.
D. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to lead $R_{\theta JL}$ and lead to ambient.
E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.
F. These curves are based on the junction-to-ambient thermal impedence which is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, assuming a maximum junction temperature of $T_{J(MAX)}$=150° C. The SOA curve provides a single pulse rating.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

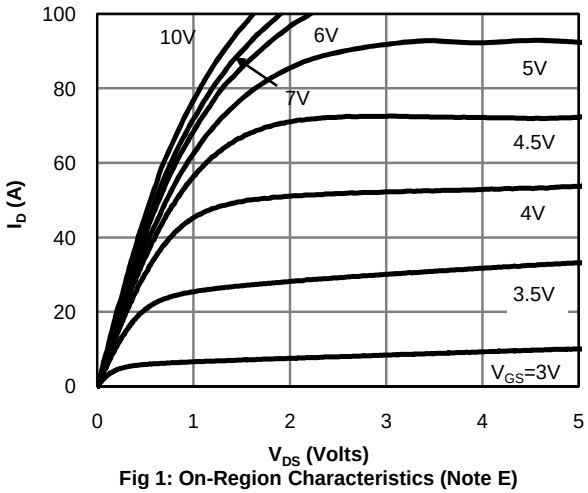


Fig 1: On-Region Characteristics (Note E)

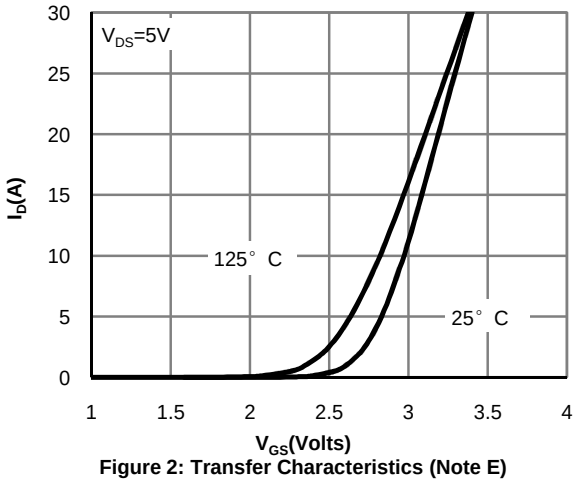


Figure 2: Transfer Characteristics (Note E)

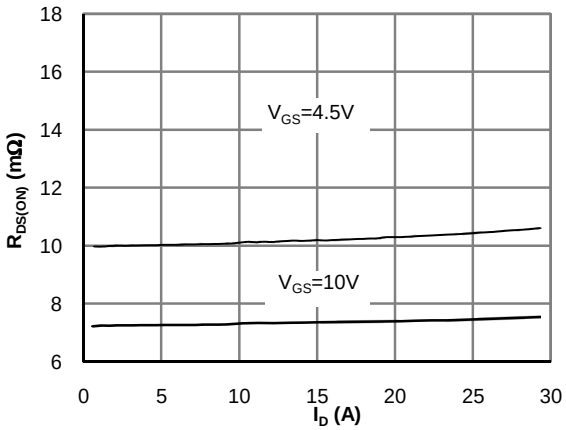


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

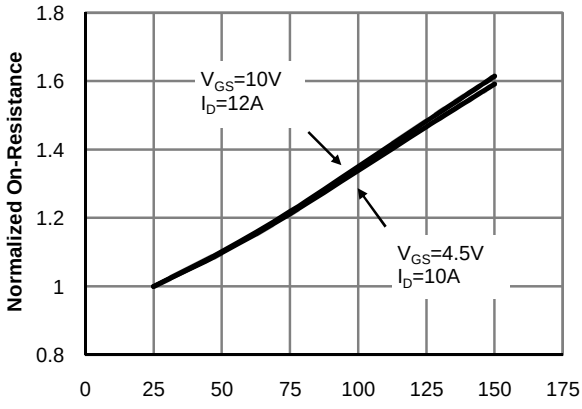


Figure 4: On-Resistance vs. Junction Temperature (Note E)

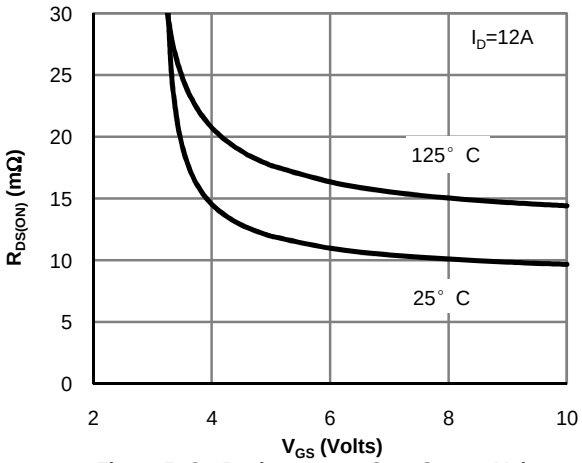


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

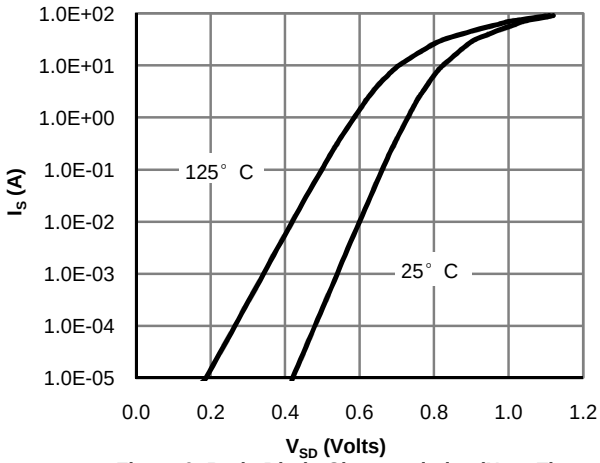


Figure 6: Body-Diode Characteristics (Note E)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

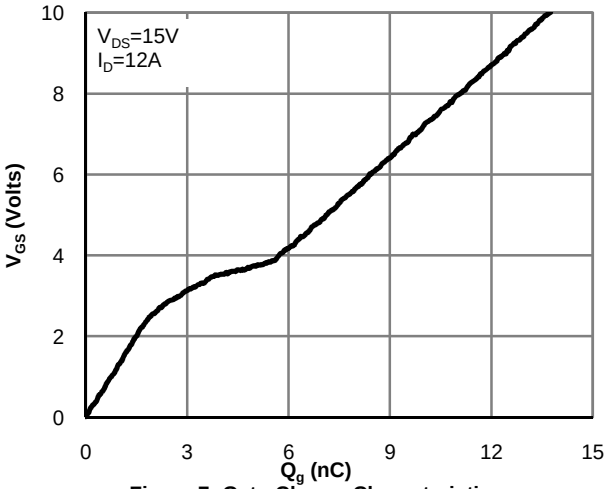


Figure 7: Gate-Charge Characteristics

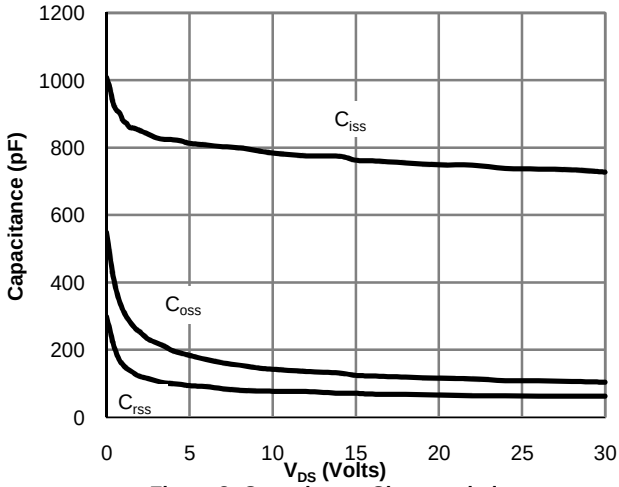


Figure 8: Capacitance Characteristics

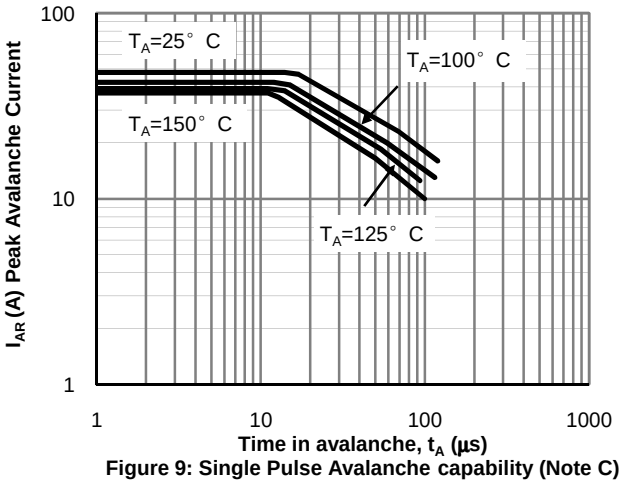


Figure 9: Single Pulse Avalanche capability (Note C)

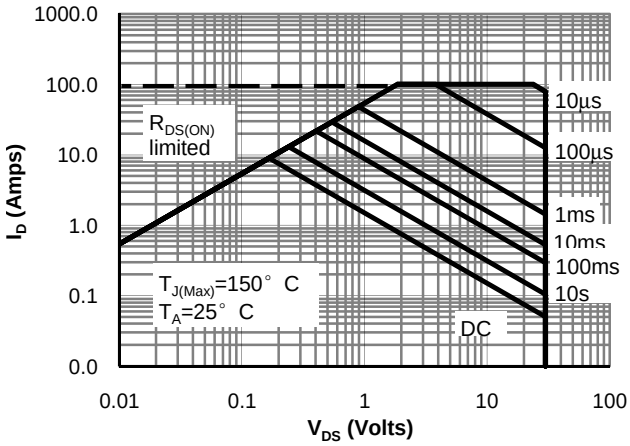


Figure 10: Maximum Forward Biased Safe Operating Area (Note F)

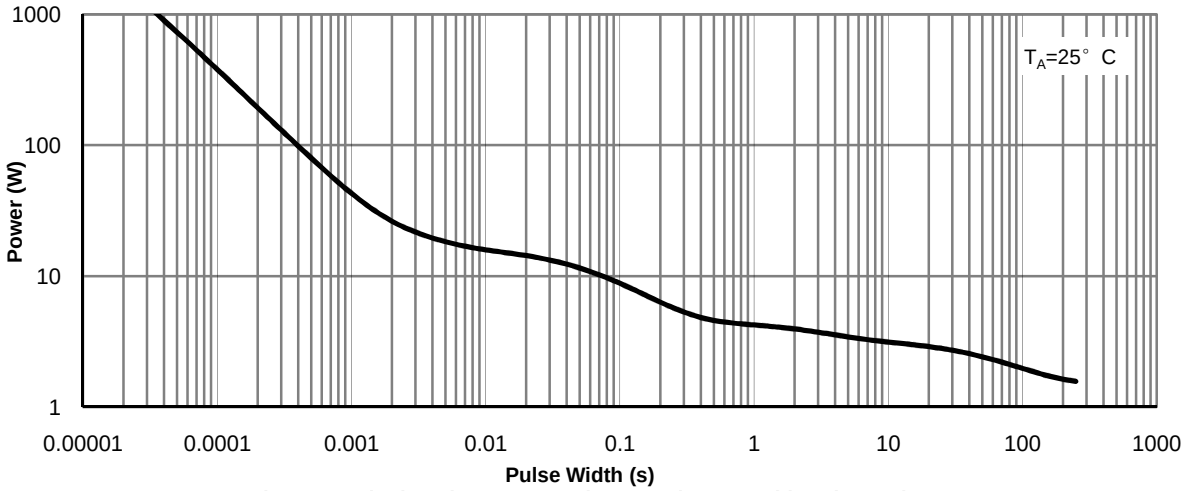


Figure 11: Single Pulse Power Rating Junction-to-Ambient (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

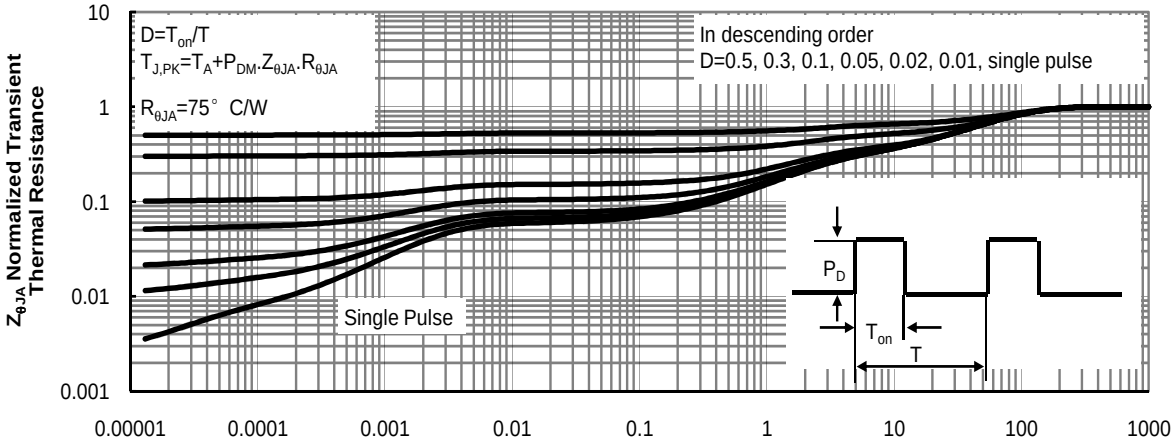
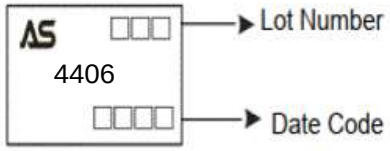


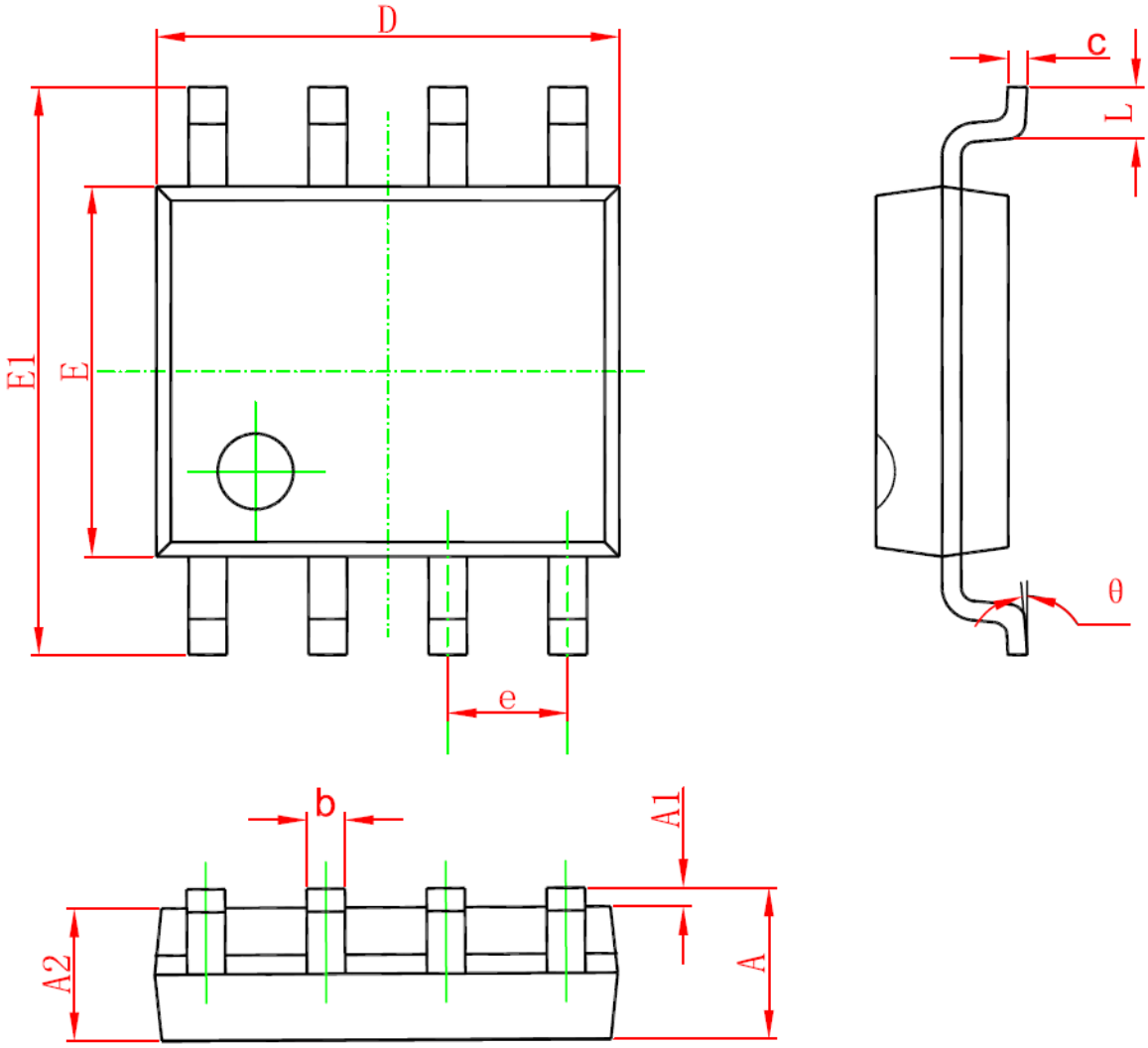
Figure 12: Normalized Maximum Transient Thermal Impedance (Note F)

Ordering and Marking Information

Ordering Device No.	Marking	Package	Packing	Quantity
ASDM4406S-R	4406	SOP-8	Tape&Reel	4000/Reel

PACKAGE	MARKING
SOP-8	

SOP-8 PACKAGE IN FORMATION



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

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