

### General Features

- High density cell design for ultra low  $R_{DS(on)}$
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high  $E_{AS}$
- Excellent package for good heat dissipation
- Special process technology for high ESD capability

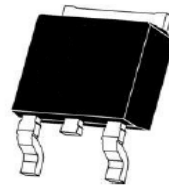
### Application

- Load switching
- Hard switched and high frequency circuits
- Uninterruptible power supply

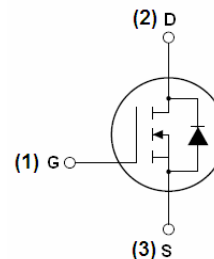
### Product Summary



$V_{DS}$	40	V
$R_{DS(on),Typ}@ V_{GS}=10V$	7.0	m $\Omega$
$I_D$	60	A



TO-252-2L top view



Schematic diagram

### Absolute Maximum Ratings ( $T_C=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	40	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current-Continuous	$I_D$	60	A
Drain Current-Continuous( $T_C=100^\circ\text{C}$ )	$I_D(100^\circ\text{C})$	42	A
Pulsed Drain Current	$I_{DM}$	240	A
Maximum Power Dissipation	$P_D$	65	W
Derating factor		0.43	W/ $^\circ\text{C}$
Single pulse avalanche energy <sup>(Note 5)</sup>	$E_{AS}$	400	mJ
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 To 175	$^\circ\text{C}$

### Thermal Characteristic

Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	62	$^\circ\text{C/W}$
Thermal Resistance, Junction-to-Case <sup>(Note 2)</sup>	$R_{\theta JC}$	2.8	$^\circ\text{C/W}$

**Electrical Characteristics ( $T_C=25^{\circ}\text{C}$  unless otherwise noted)**

Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS}=0V, I_D=250\mu A$	40	-	-	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=40V, V_{GS}=0V$	-	-	1	$\mu A$
Gate-Body Leakage Current	$I_{GSS}$	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	$\pm 100$	nA
<b>On Characteristics (Note 3)</b>						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1.2	1.6	2.5	V
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=20A$	-	7.0	7.5	m $\Omega$
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=4.5V, I_D=20A$	-	10.5	12	m $\Omega$
Forward Transconductance	$g_{FS}$	$V_{DS}=10V, I_D=20A$	15	-	-	S
<b>Dynamic Characteristics (Note 4)</b>						
Input Capacitance	$C_{iss}$	$V_{DS}=20V, V_{GS}=0V,$ $F=1.0\text{MHz}$	-	1520	-	PF
Output Capacitance	$C_{oss}$		-	236	-	PF
Reverse Transfer Capacitance	$C_{rss}$		-	160	-	PF
<b>Switching Characteristics (Note 4)</b>						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=20V, I_D=2A, R_L=1\Omega$ $V_{GS}=10V, R_G=3\Omega$	-	6.4	-	nS
Turn-on Rise Time	$t_r$		-	17.2	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	29.6	-	nS
Turn-Off Fall Time	$t_f$		-	16.8	-	nS
Total Gate Charge	$Q_g$	$V_{DS}=20V, I_D=20A,$ $V_{GS}=10V$	-	29	-	nC
Gate-Source Charge	$Q_{gs}$		-	4.5	-	nC
Gate-Drain Charge	$Q_{gd}$		-	6.4	-	nC
<b>Drain-Source Diode Characteristics</b>						
Diode Forward Voltage (Note 3)	$V_{SD}$	$V_{GS}=0V, I_S=10A$	-	-	1.2	V
Diode Forward Current (Note 2)	$I_S$		-	-	60	A
Reverse Recovery Time	$t_{rr}$	$T_J = 25^{\circ}\text{C}, I_F = 20A$ $di/dt = 100A/\mu s$ (Note 3)	-	29	-	nS
Reverse Recovery Charge	$Q_{rr}$		-	26	-	nC
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

**Notes:**

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board,  $t \leq 10$  sec.
3. Pulse Test: Pulse Width  $\leq 300\mu s$ , Duty Cycle  $\leq 2\%$ .
4. Guaranteed by design, not subject to production
5.  $E_{AS}$  condition :  $T_J=25^{\circ}\text{C}, V_{DD}=20V, V_G=10V, L=1\text{mH}, R_g=25\Omega,$

Typical Electrical and Thermal Characteristics (Curves)

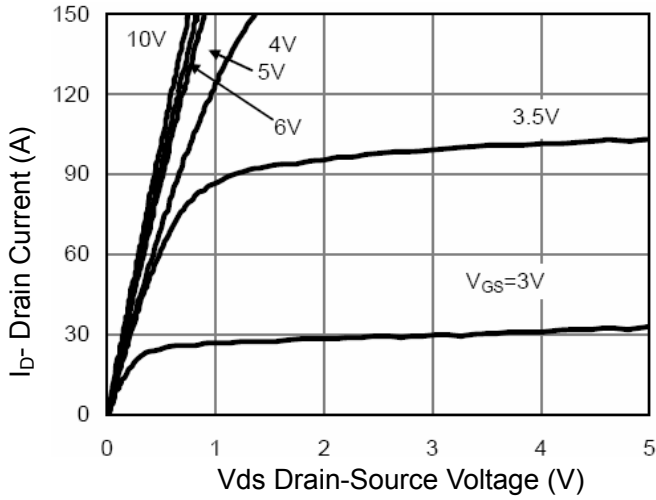


Figure 1 Output Characteristics

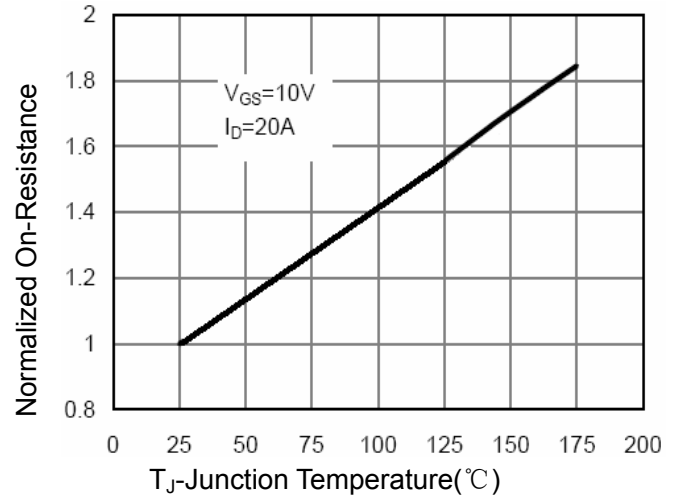


Figure 4  $R_{dson}$ -Junction Temperature

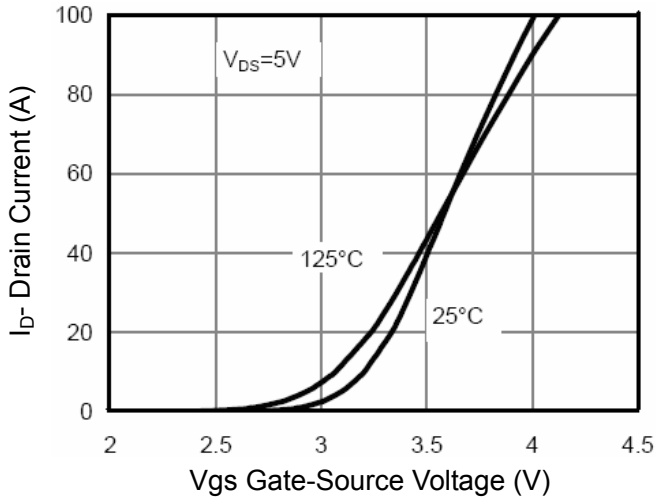


Figure 2 Transfer Characteristics

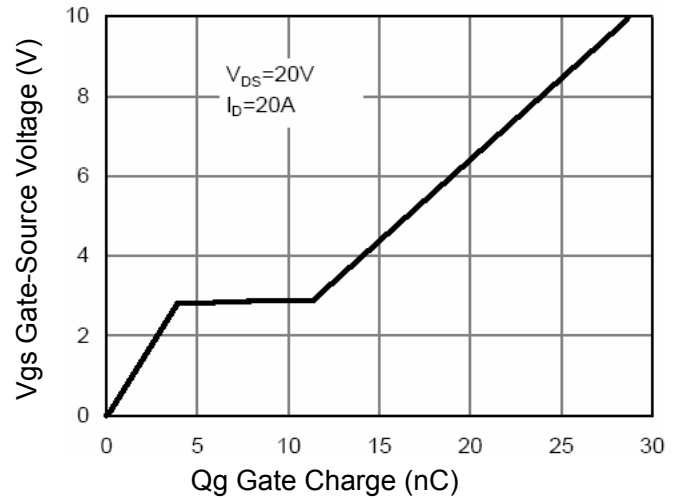


Figure 5 Gate Charge

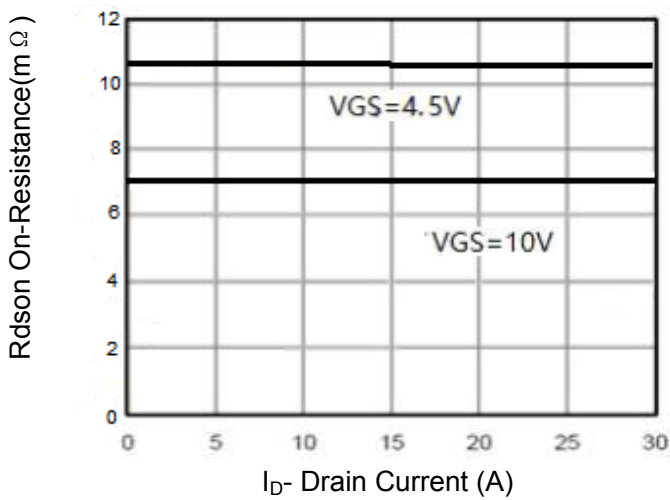


Figure 3  $R_{dson}$ - Drain Current

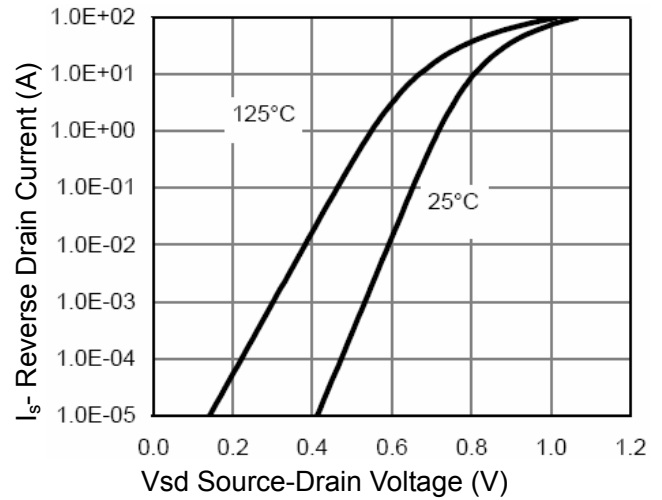
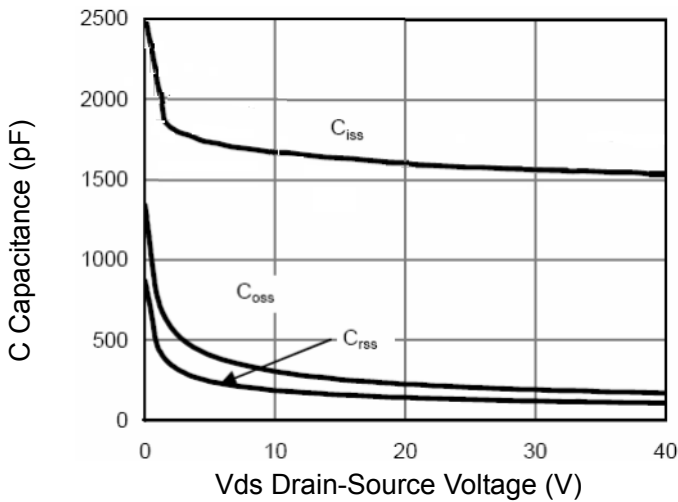
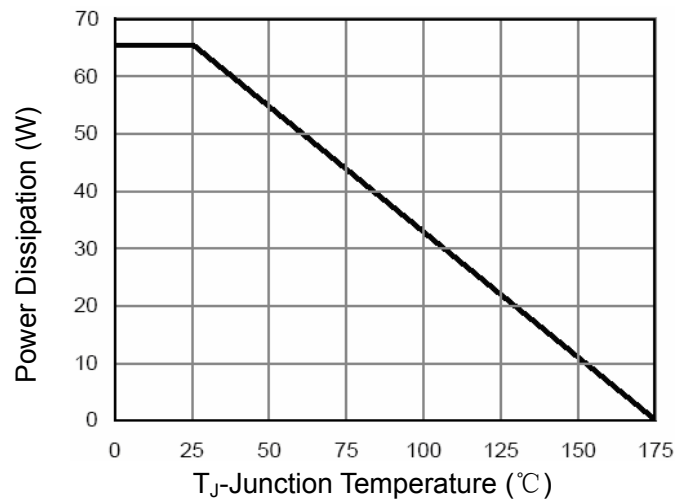


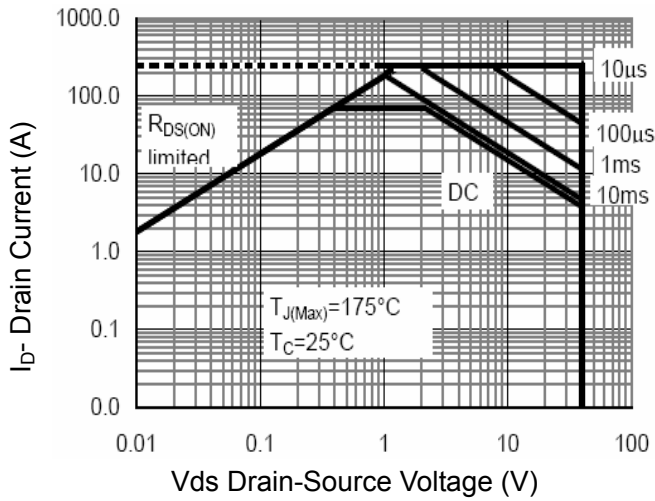
Figure 6 Source- Drain Diode Forward



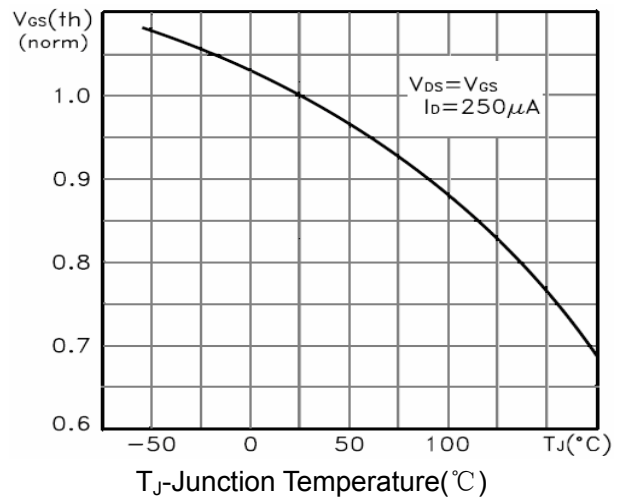
**Figure 7 Capacitance vs Vds**



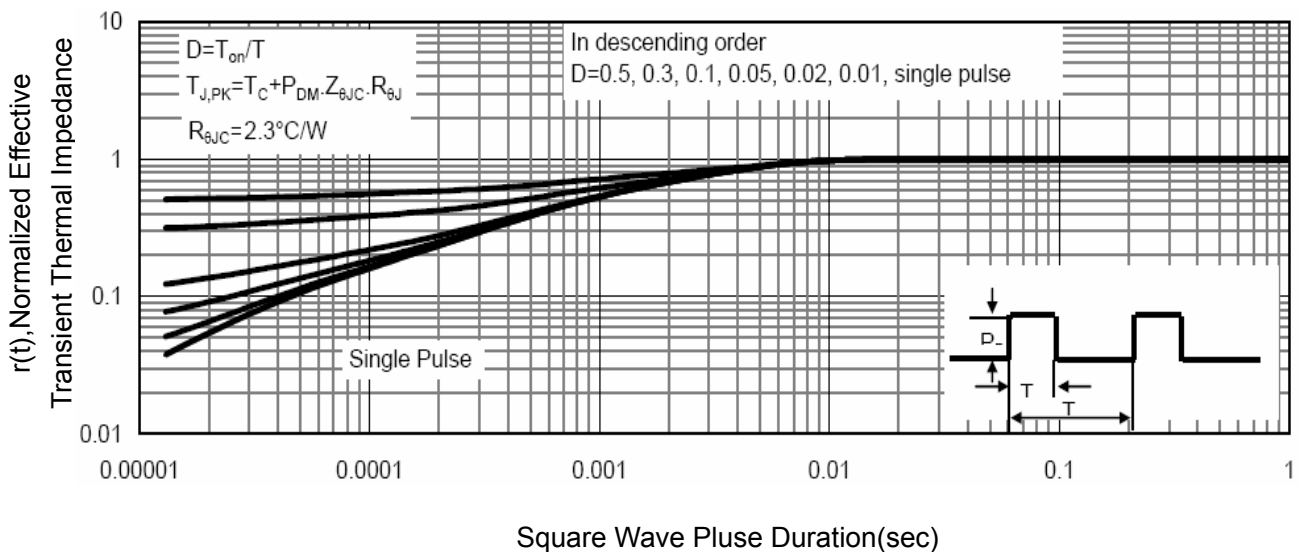
**Figure 9 Power De-rating**



**Figure 8 Safe Operation Area**



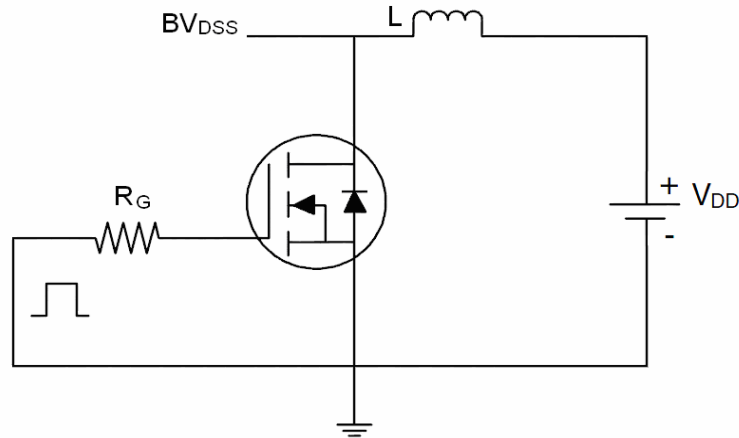
**Figure 10 VGS(th) vs Junction Temperature**



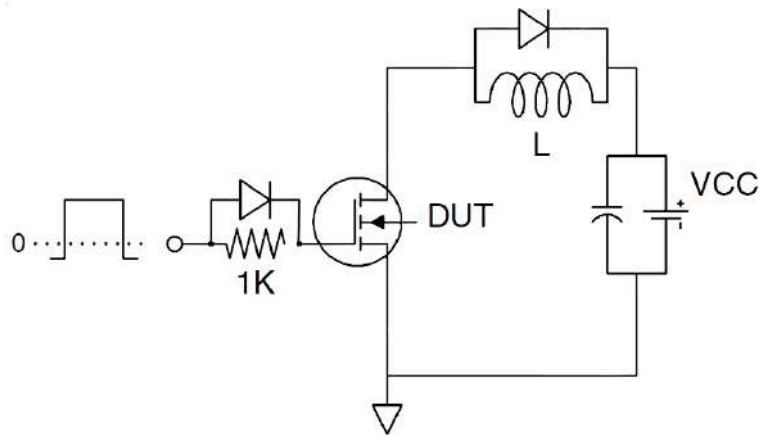
**Figure 11 Normalized Maximum Transient Thermal Impedance**

**Test circuit**

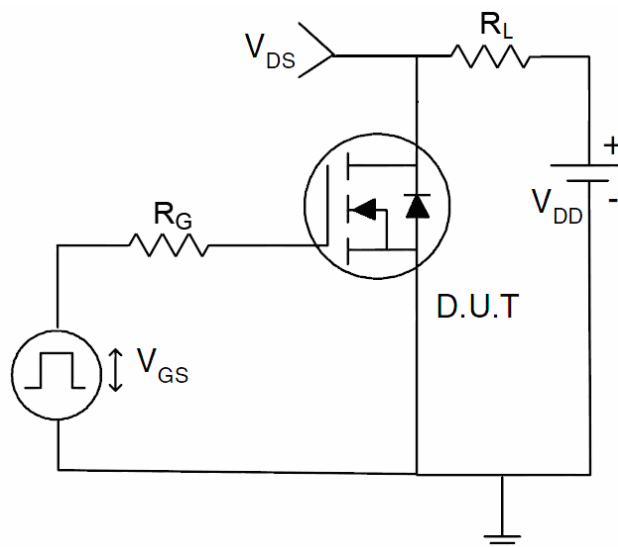
**1)  $E_{AS}$  Test Circuit**



**2) Gate Charge Test Circuit**

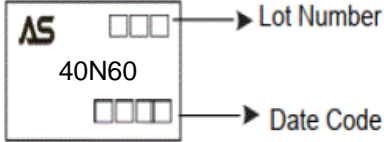


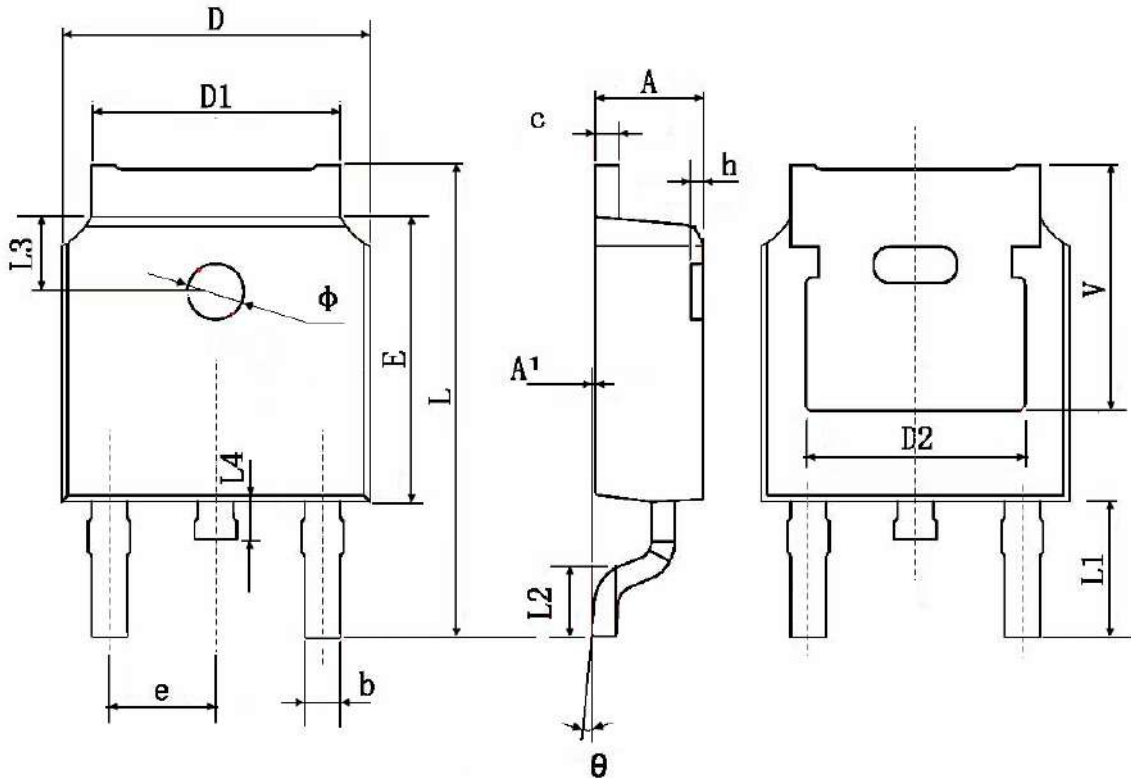
**3) Switch Time Test Circuit**



### Ordering and Marking Information

Ordering Device No.	Marking	Package	Packing	Quantity
ASDM40N60KQ-R	40N60	TO-252	Tape&Reel	2500/Reel

PACKAGE	MARKING
TO-252	

**TO-252 Package Information**


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
b	0.660	0.860	0.026	0.034
c	0.460	0.580	0.018	0.023
D	6.500	6.700	0.256	0.264
D1	5.100	5.460	0.201	0.215
D2	4.830 TYP.		0.190 TYP.	
E	6.000	6.200	0.236	0.244
e	2.186	2.386	0.086	0.094
L	9.800	10.400	0.386	0.409
L1	2.900 TYP.		0.114 TYP.	
L2	1.400	1.700	0.055	0.067
L3	1.600 TYP.		0.063 TYP.	
L4	0.600	1.000	0.024	0.039
φ	1.100	1.300	0.043	0.051
θ	0°	8°	0°	8°
h	0.000	0.300	0.000	0.012
V	5.350 TYP.		0.211 TYP.	

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