

MIPI 进展、测试挑战及解决方案

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May 2023



Agenda

- MIPI Technology Overview
- MIPI C-PHY Update and Solution
- MIPI D-PHY Update and Solution
- MIPI M-PHY Update and Solution
- MIPI A-PHY Update and Solution



5G



Automotive

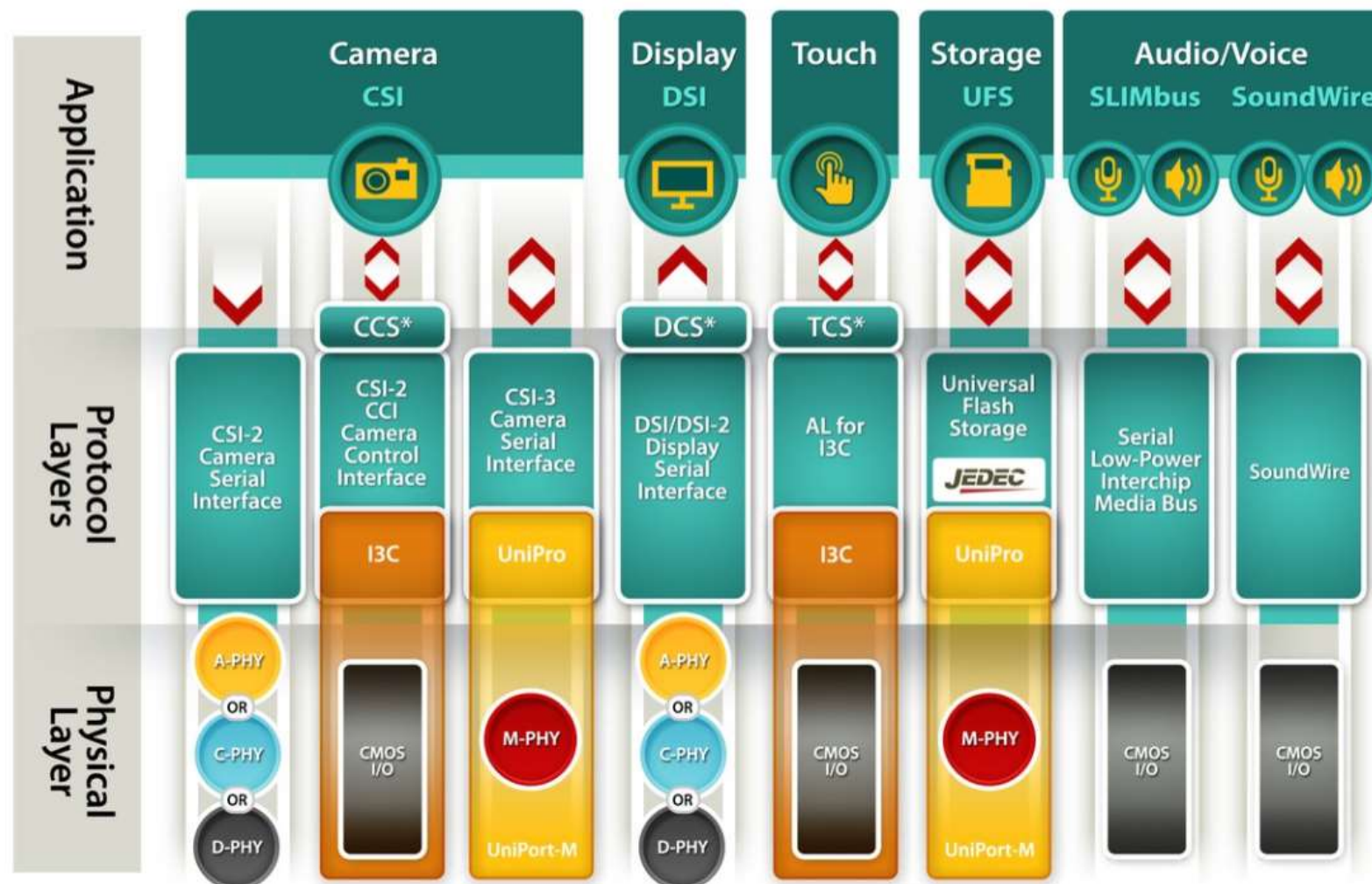


Internet of Things



Mobile

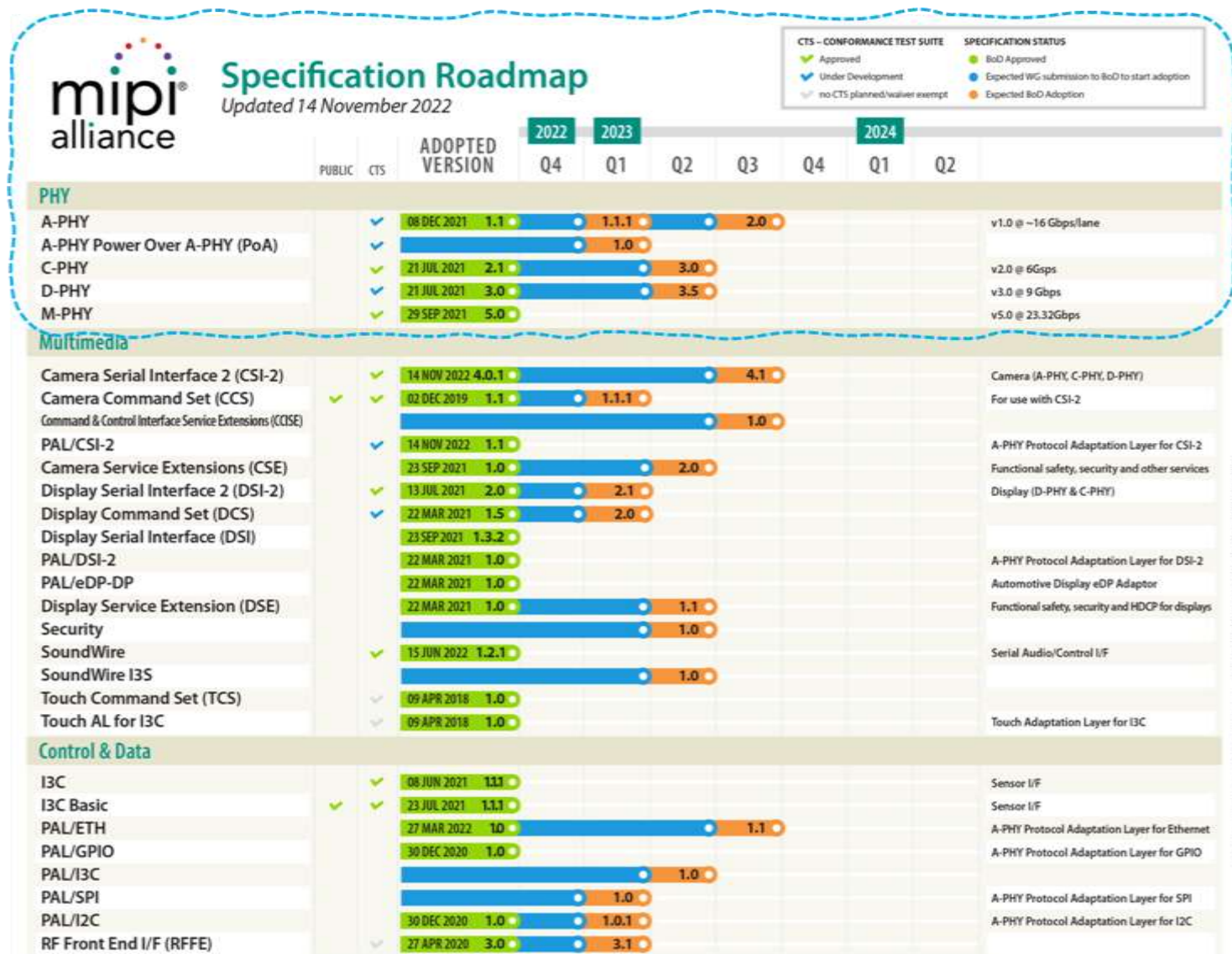
MIPI Overview: Multimedia Specifications



*Indicates an available Command Set.

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MIPI PHY Roadmap



MIPI PHY Feature Roadmap

A-PHY Feature Roadmap

Category	Feature	v1.0	v1.1 ^[1]	V2.0	Next
	Board Adoption	Q3 20	Q4 21	Q2 23	24-25
Channels	Coax Channel 15 meter – 4-inline connectors	✓	✓	TBD	TBD
	STP / SPP Channel 10 meter – 4 inline connectors	✓	✓	TBD	TBD
	STQ 10 meter – 4 inline connectors (2 differential pairs)	-	✓	TBD	TBD
Max Downlink Data Rate	Single Lane Downlink	16Gbps	16Gbps	32Gbps	>48Gbps
	Dual Lane Downlink	-	32Gbps	64Gbps	~100Gbps
Max Uplink Data Rate	Uplink	100Mbps	200Mbps	1.6Gbps	TBD

D-PHY Feature Roadmap

Category	Feature	v3.0	v3.5 FC	v3.5 EC (Optional)	v4.0 EC (Tentative)
	Board Adoption	3Q 21			
Symbol Rate (Gbps/Lane)	Standard Channel	9	9	9 Bands B1, B2, B3, B4	TBD
	Short Channel	11	11	Same as above	TBD
	Basic De-emphasis	✓	✓	✓	✓
Increased Symbol Rate	Calibration	✓	✓	✓	✓
	Additional UI Jitter (RCLK jitter) specs	✓	✓	✓	✓
	Rx Equalization	✓	✓	✓	✓

C-PHY Feature Roadmap

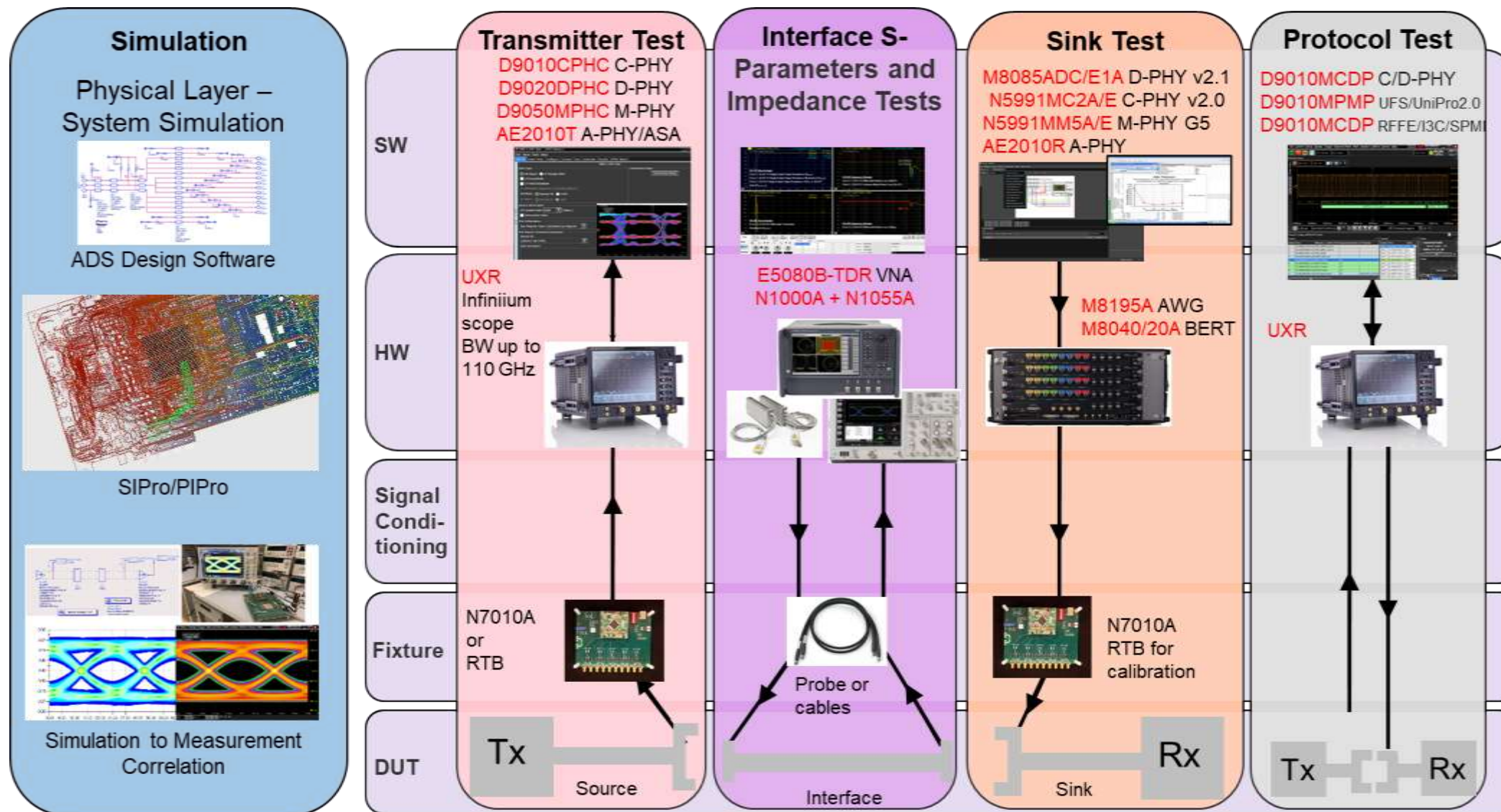
Category	Feature	v1.0	v1.1	v1.2	v2.0	v2.1	v3.0
	Board Adoption	4Q 14	1Q 16	1Q 17	3Q 19	3Q 21	~1Q 23
Symbol Rate (Gbps/Lane)	Standard Channel, Gbps (Gbps)	-	2.8 (6.4)	3.5 (8.0)	6 (13.7)	6 (13.7)	~5 (17.8)
	Short Channel, Gbps (Gbps)	-	3.0 (6.9)	4.5 (10.3)	8 (18.3)	8 (18.3)	~7 (24.9)
Increased Symbol Rate	Basic Pre-emphasis		✓	✓	✓	✓	✓
	Advanced TxEQ, Calibration			✓	✓	✓	✓
	Additional UI (RCLK) Jitter specs			✓	✓	✓	✓
	Rx Equalization				✓	✓	✓
	Multi-phase 18-state coding (3,556 coding factor)						✓

M-PHY Feature Roadmap

Category	Feature	v2.0	v3.1	v4.1	v5.0	v6.0
	Board Adoption	Q2 12	Q2 14	Q1 17	~Q4 21	~2025
Data rate	Max data rate per lane (Rate B Gbps)	~3	~6	~12	~24	TBD
	Mobile Long Channel (CH2, channel length in inches)	~13	~13	~13	-	-
Channel support	Mobile Standard Channel (CH1, channel length in inches)	~6	~6	~6	~6	~6
	Automotive Channel					TBD
Equalization	Tx De-emphasis		✓	✓	✓	✓
	Rx Equalization			✓	✓	✓
	Advanced Tx and RX equalization					✓
Power Reduction	Unterminated Mode	✓	✓	✓	-	-
	Burst mode transmission	✓	✓	✓	✓	✓

What's New and Coming Up on the MIPI PHY Roadmap
Sep 2022

Keysight MIPI Solution Overview

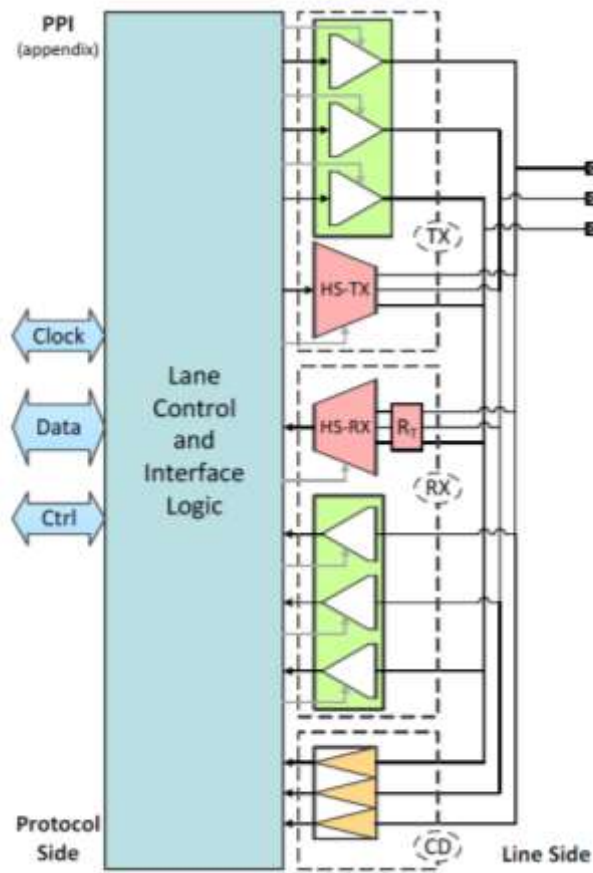


Agenda

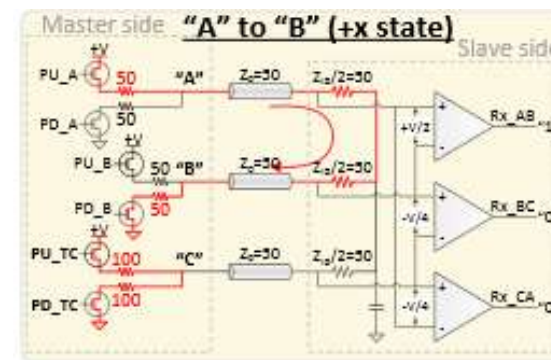
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- **MIPI C-PHY Update and Solution**
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- MIPI A-PHY Update and Solution



C-PHY物理层架构



- Lane consisting of 3 wires, A, B, C
- TXs and RXs: Bidirectional
- Contention detection (LP only)
- Two set's of TXs / RXs (HS & LP)
- LP-mode:
 - Large amplitude ($\sim 1V$), unterminated
 - Data format: "RZ"
 - Signaling: non-differential
- HS-mode:
 - Small amplitude ($\sim 200mV, pp$)
 - Termination $50\ \Omega$ – "star-type" (encircled)
 - Data format: 3-phase / 3-level
 - Signaling: 3 single ended wires forming a HS-lane,
 - Encoding: 16 bits to 7 symbols with 5 values (0,1,2,3,4) $\Rightarrow$ coding gain 2.28



C-PHY 规范及CTS更新



C-PHY 1.2 : Approved Mar 28, 2016



C-PHY 2.0 : Approved Sep 9, 2019

C-PHY 2.1: Aopted 21 Jul, 2021

- Speed up to 6Gsps~8Gsps
- RX Equalizer (1st order CTLE)
- Fast bus turn around



CTS 1.1 : Approved May 21, 2019



C-PHY 2.1 : Approved Oct 23, 2021

- Oscilloscope bandwidth updates
- Direct connect test for VOHHS and VCPTX
- Reduced amplitude LVHS(Test 1.2.7, 1.2.10)
- LVLP operation(Test 1.1.1)
- Removed DeltaUI(Test 1.2.20)
- Eye diagram test with Adv RX EQ(Test 1.2.21) – rev 02
- UI Jitter Peak(Test 1.2.22) – rev 02
- Calibration Preamble sequence (Group 1.5.x) (informative) – rev 03

C-PHY v2.1 互连特性

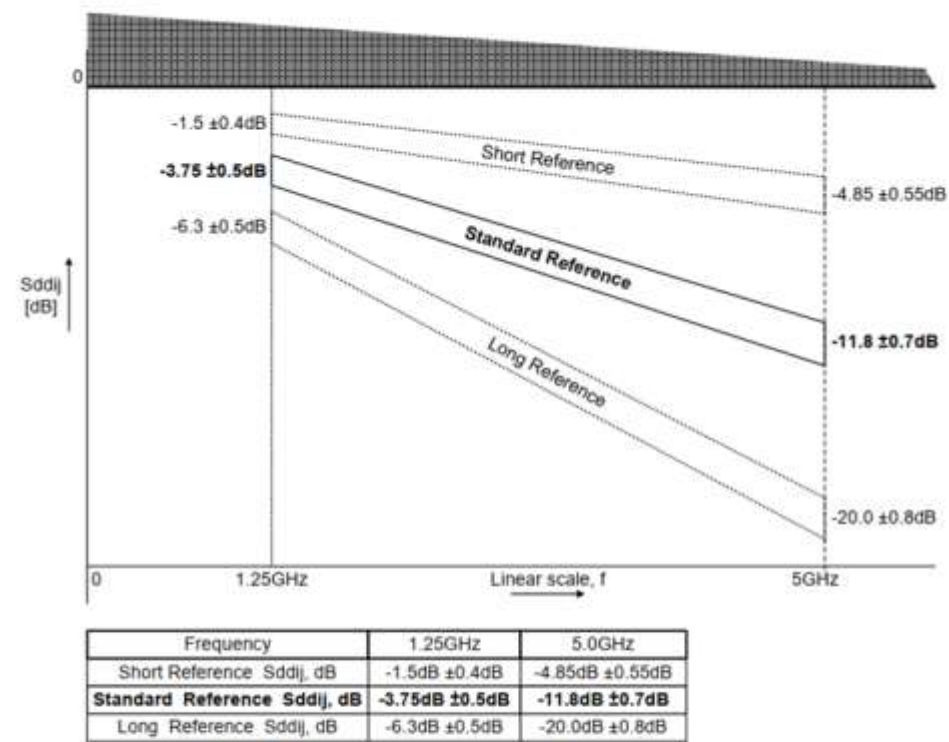


Figure 52 Template for Differential Insertion Losses

Table 65 C-PHY System Capability, High-Speed Mode

Channel	TxEQ Option disabled	TxEQ Option enabled	RxEQ Option enabled ²
Short Reference Channel (Section 8) ¹	2.5 Gsps	4.5 Gsps	8 Gsps
Standard Reference Channel (Section 8)	1.7 Gsps	3.5 Gsps	6 Gsps
Long Reference Channel (Section 8)	1.3 Gsps	2.3 Gsps	4 Gsps

Table 51 Maximum Symbol Rates Without CTLE

Description	Reference Channel			Units	Notes
	Short	Standard	Long		
When operating above these Symbol Rates, it is necessary to use a CTLE.	4.5	3.5	2.3	Gsps	—

$$H(s) = \frac{A_{DC}\omega_{P1}\omega_{P2}}{\omega_Z} \cdot \frac{s+\omega_Z}{(s+\omega_{P1})(s+\omega_{P2})}$$
 [Equation 1]

A_{DC} is the DC gain,
 $\omega_{P1} = 2\pi f_{P1}$ f_{P1} is the first pole frequency
 $\omega_{P2} = 2\pi f_{P2}$ f_{P2} is the second pole frequency
 $\omega_Z = 2\pi f_Z$ f_Z is the zero frequency

$$f_{P1} = f_Z \cdot 10^{((A_{AC}-A_{DC})/20)}$$

$$A_{AC} = 20 \cdot \log\left(\frac{f_{P1}}{f_Z}\right) + A_{DC}$$

Table 53 CTLE Reference Parameter Values, Standard Channel, 6 Gsps (Informative)

f _Z (GHz)	f _{P1} (GHz)	f _{P1} / f _Z	f _{P2} (GHz)	A _{DC} (dB)
1.0	2.0	2.0	10	0
1.0	2.2	2.2	10	0
1.0	2.4	2.4	10	0
1.0	2.6	2.6	10	0
1.0	2.8	2.8	10	0
1.0	3.0	3.0	10	0

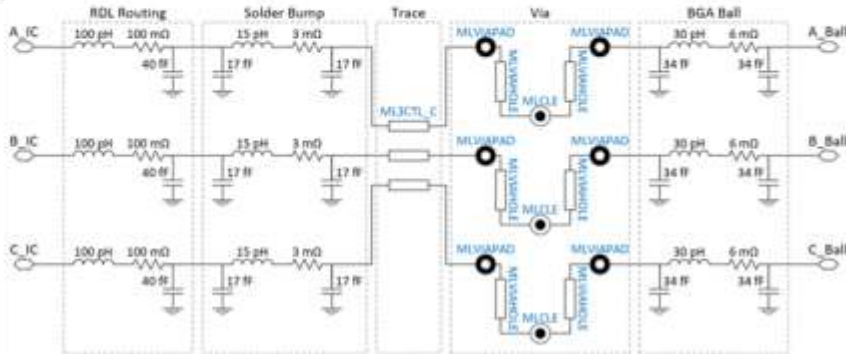
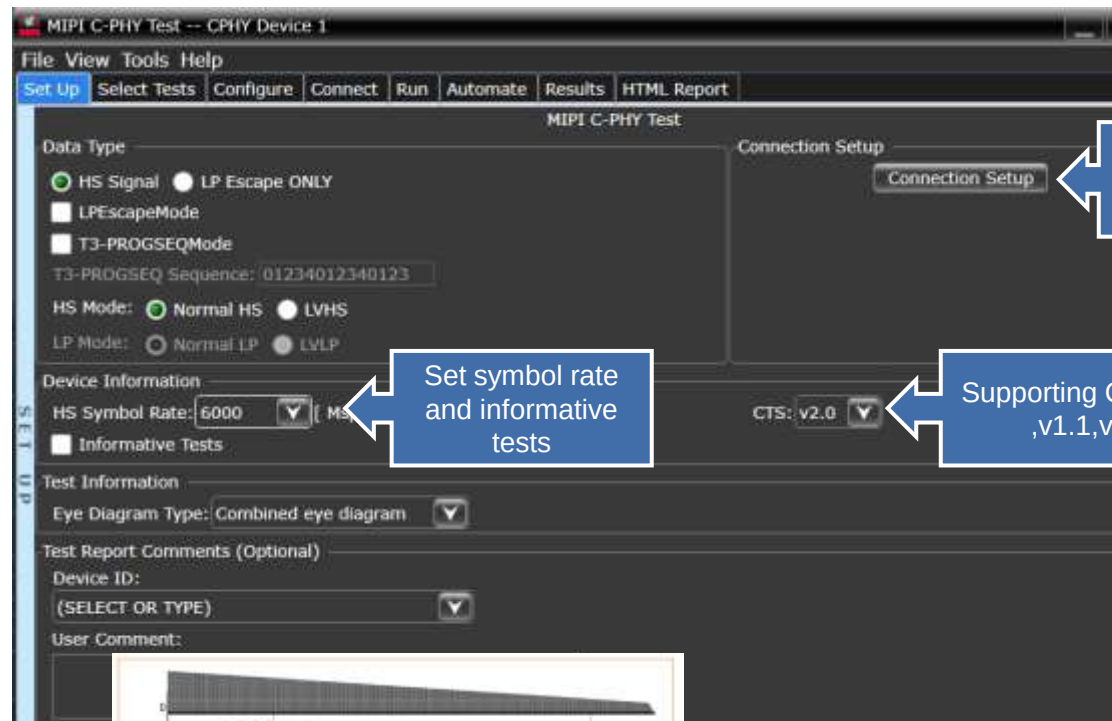


Figure 138 Reference Package Model Circuit Diagram

Keysight D9010CPHC C-PHY Tx 测试软件



Continuous and Burst mode support by Active probe connection and direct connection

Set symbol rate and informative tests

Supporting CTS v1.0, v1.1, v2.0

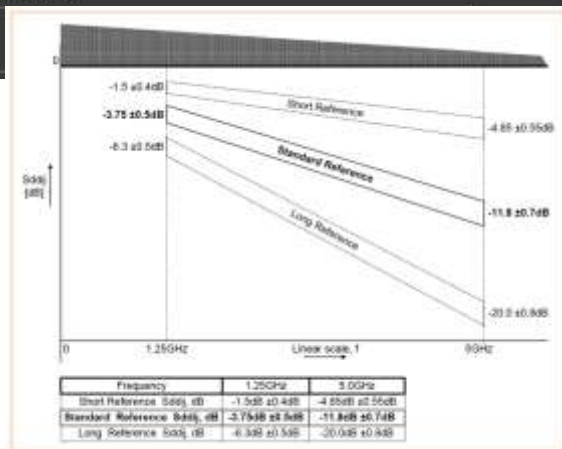
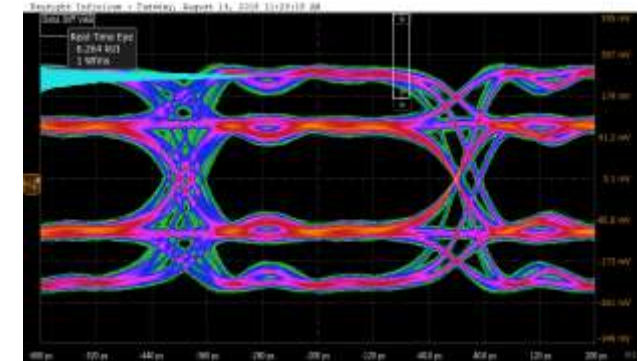
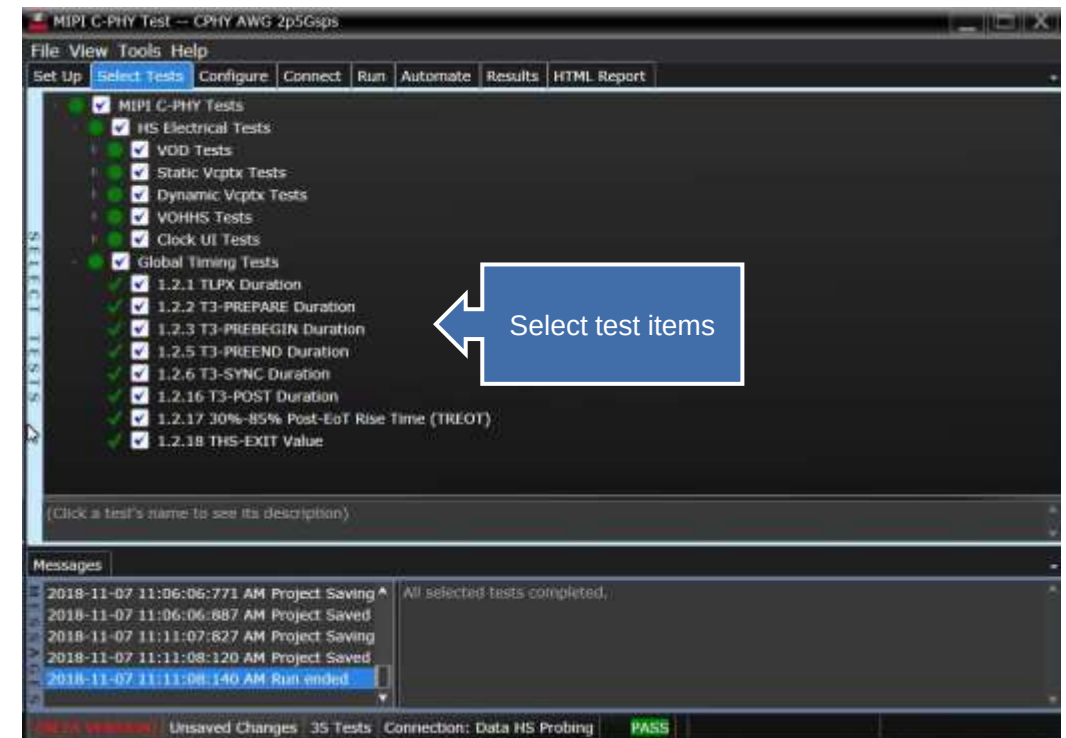
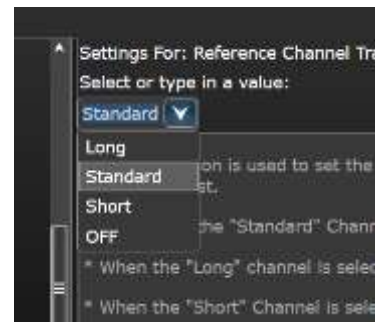


Figure 1.2.21-4: C-PHY Reference Channels



Select test items

CPHY的时钟恢复和眼图测试

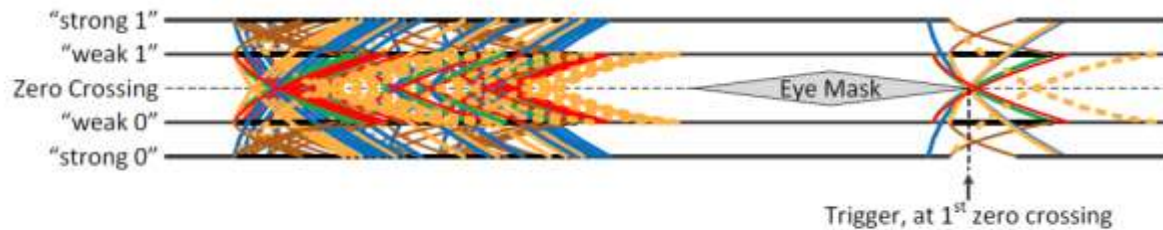


Figure 63 C-PHY Eye Pattern Example, Triggered Eye

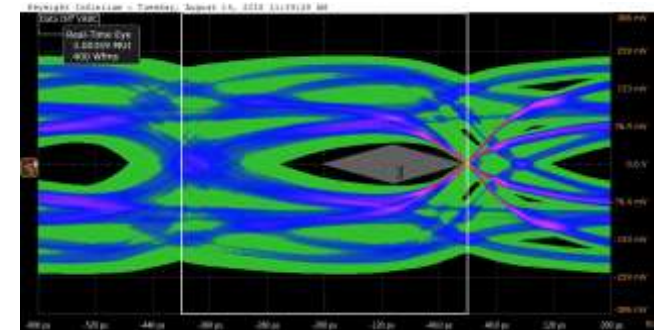
Clock is recovered from the earliest edge of a symbol transition.



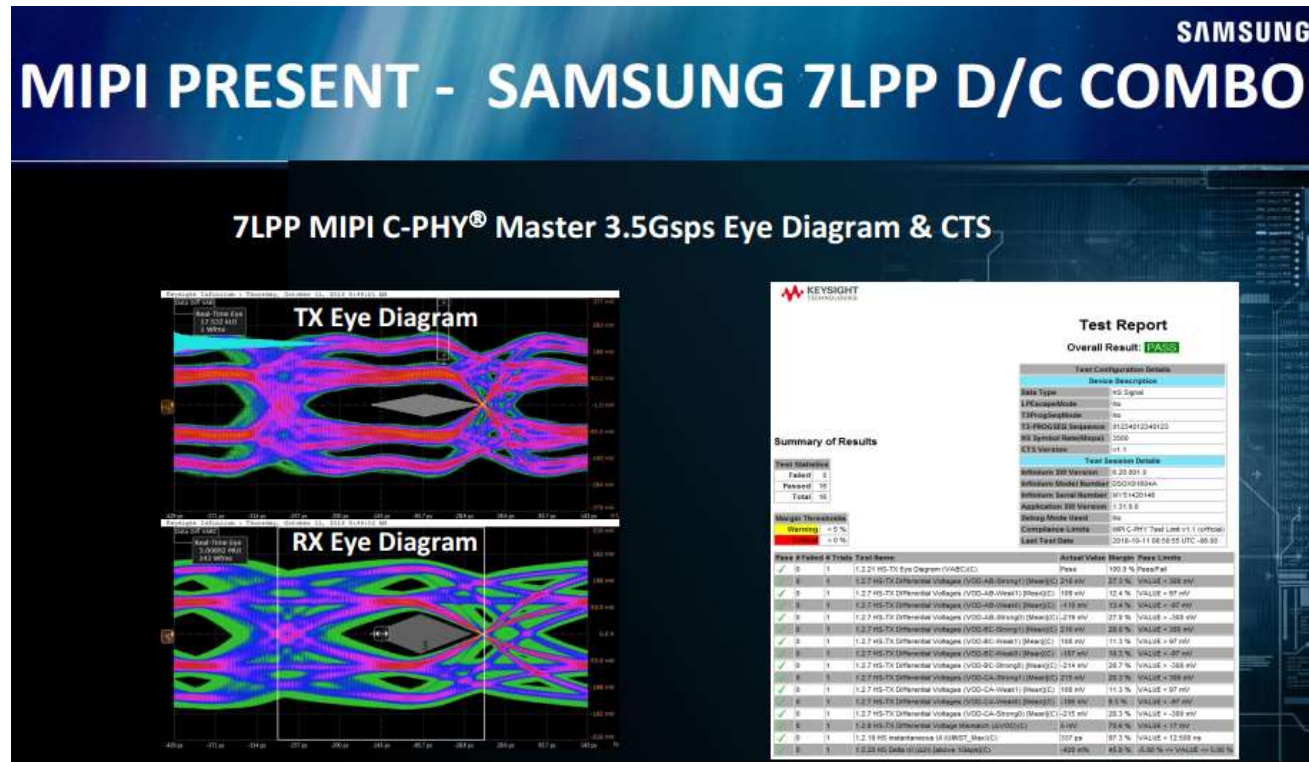
2. Using function make VAB, VAC, VBC (Symbol transition)

3. Among VAB, VAC, VBC, find each first arrival edge on acquired signal and build clock recovery

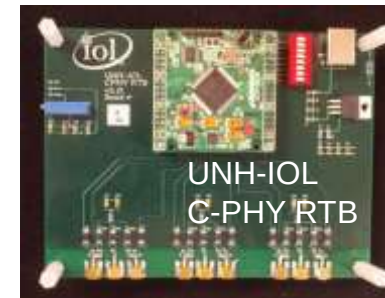
1. Acquire VA, VB, VC at once



Keysight D9010CPHC C-PHY Tx 测试实例



摘自2018年11月 MIPI DevCon Keynote
《MOBILE TECHNOLOGY FOR THE SMART WORLD》



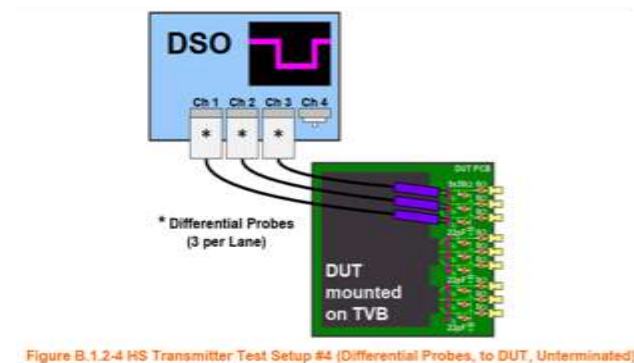
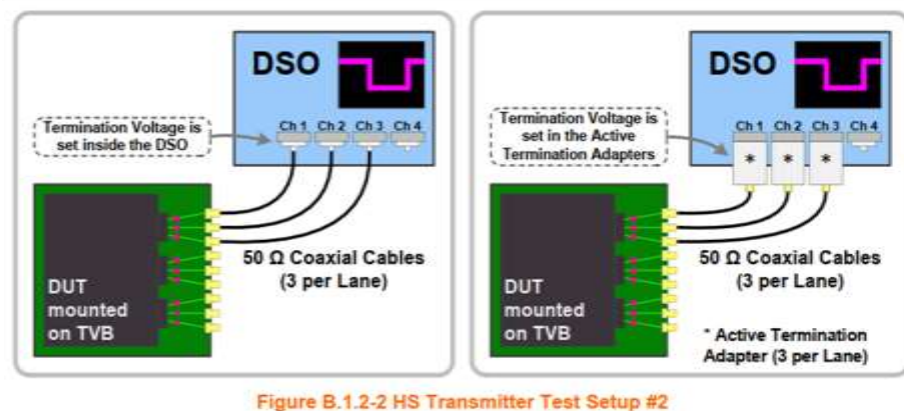
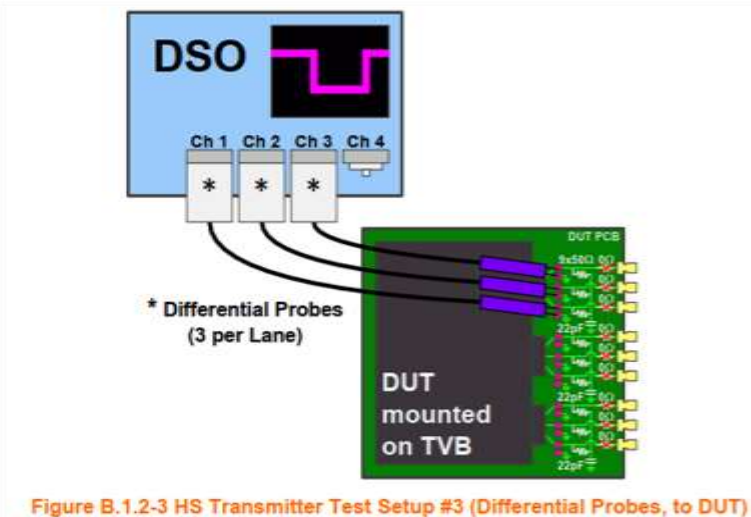
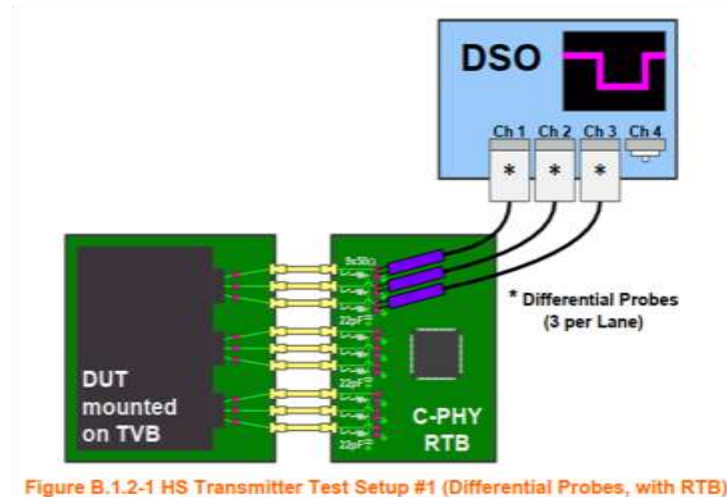
- The DUT should be configured to transmit a continuous stream of HS data, because this test setup is suitable for measurements only in the HS mode of operation.

C-PHY v1.1新增1.2.21眼图测试项为了达到更好测试效果，CTS要求使用连续模式

C-PHY Tx 测试组网(C-PHY CTS v2.0)

Table B.1.2-1 Applicability of Test Setups for Transmit Tests

CTS Test	B.1.1	Test Setup #, B.1.2-n Figure			
		1	2	3	4
1.2.1 t_{LPX} Duration		✓			
1.2.2 t_{PREPARE} Duration		✓			
1.2.3 t_{PREBEGIN} Duration		✓			
1.2.4 t_{PROGSEQ} Duration		✓			
1.2.5 t_{PREEND} Duration		✓			
1.2.6 t_{SYNC} Duration		✓			
1.2.7 HS-TX Differential Voltages ($V_{\text{DD_AB}}, V_{\text{DD_BC}}, V_{\text{DD_CA}}$)			✓	✓	
1.2.9 HS-TX Single-Ended Output High Voltages ($V_{\text{OHHS(UT)A}}, V_{\text{OHHS(UT)B}}, V_{\text{OHHS(UT)C}}$)			✓	✓	
1.2.10 HS-TX Static Common-Point Voltages (V_{CPTX})			✓	✓	
1.2.12 HS-TX Dynamic Common-Point Variations Between 50-450 MHz ($\Delta V_{\text{CPTX(LF)}}$)			✓	✓	
1.2.13 HS-TX Dynamic Common-Point Variations Above 450 MHz ($\Delta V_{\text{CPTX(HF)}}$)			✓	✓	
1.2.14 HS-TX Rise Time (t_{r})			✓		
1.2.15 HS-TX Fall Time (t_{f})			✓		
1.2.16 $t_{\text{30-85\%}}$ Duration		✓			
1.2.17 30%-85% Post-EoT Rise Time (t_{REOT})		✓			
1.2.18 $t_{\text{HS-EXIT}}$ Value		✓			
1.2.19 HS Clock Instantaneous UI (UI_{INST})			✓	✓	
1.2.20 HS Clock Delta UI (ΔUI) (Obsolete)			✓	✓	
1.2.21 HS-TX Eye Diagram			✓		
1.2.22 HS-TX UI Jitter ($UI_{\text{JITTERPEAK_TX}}$)			✓		
1.3.1 INIT: LP-TX Initialization Period ($t_{\text{INIT_PRIMARY}}$) [can use B.1.1 or B.1.2]	✓	✓			
1.3.2 ULPS Exit: Transmitted t_{WAKEUP} Interval	✓	✓			
1.4.1 HS-TX Differential Voltages Unterminated ($V_{\text{OD(UT)AB}}, V_{\text{OD(UT)BC}}, V_{\text{OD(UT)CA}}$) [Test is similar to Test 1.2.7]		✓			✓
1.4.3 HS-TX Single-Ended Output High Voltages Unterminated ($V_{\text{OHHS(UT)A}}, V_{\text{OHHS(UT)B}}, V_{\text{OHHS(UT)C}}$) [Test is similar to Test 1.2.9]		✓			✓
1.4.4 HS-TX Static Common-Point Voltages Unterminated ($V_{\text{CPTX(UT)}}$) [Test is similar to Test 1.2.10]		✓			✓
2.4.1 HS-RX t_{TERMIN} Duration		✓			



C-PHY Rx 测试方案组网

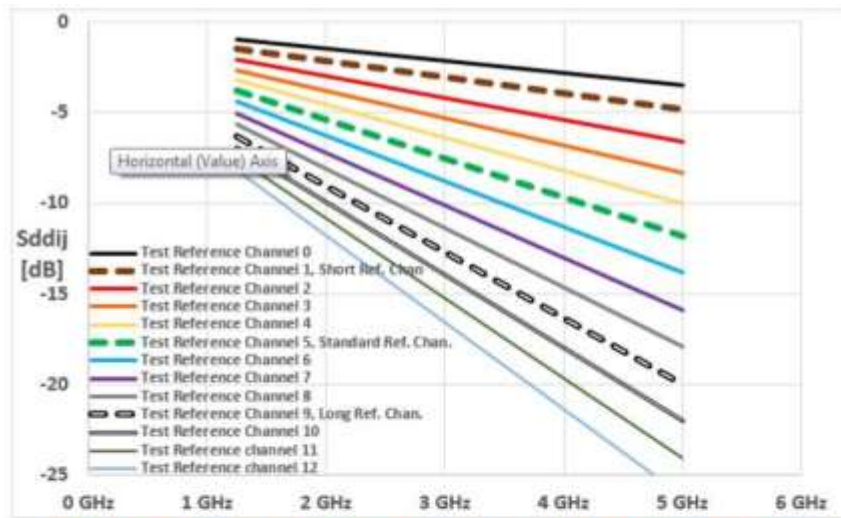
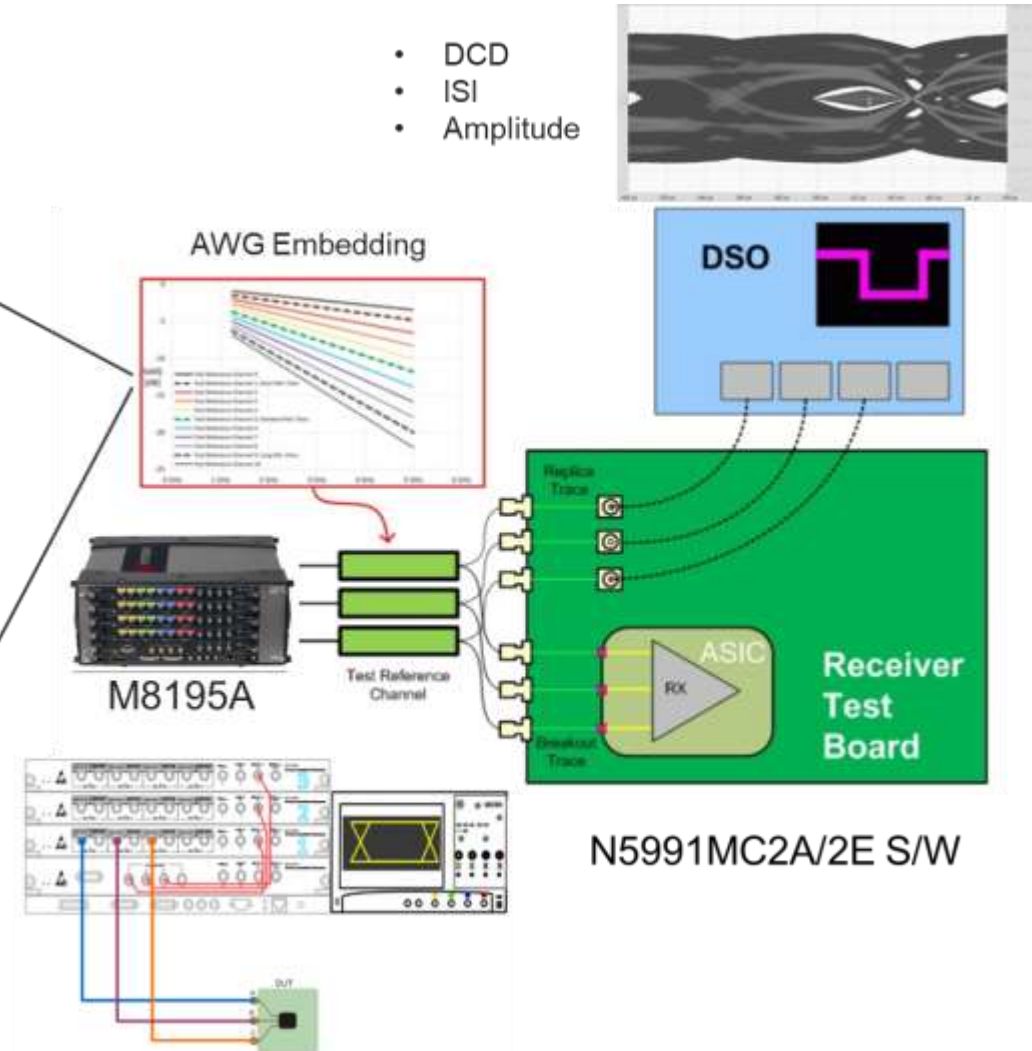


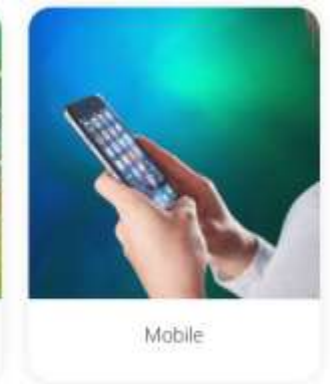
Figure 2.3.3-4: Template for Differential Insertion Losses – Test Reference Channels

	1.25 GHz	5 GHz	Physical Length
Test Reference Channel 0	-0.9375	-3.475	5 cm
Test Reference Channel 1, Short Ref. Chan	-1.5	-4.85	10 cm
Test Reference Channel 2	-2.0625	-6.5875	15 cm
Test Reference Channel 3	-2.625	-8.325	20 cm
Test Reference Channel 4	-3.1875	-10.0625	25 cm
Test Reference Channel 5, Standard Ref. Chan.	-3.75	-11.8	30 cm
Test Reference Channel 6	-4.3875	-13.85	35 cm
Test Reference Channel 7	-5.025	-15.9	40 cm
Test Reference Channel 8	-5.6625	-17.95	45 cm
Test Reference Channel 9, Long Ref. Chan.	-6.3	-20	50 cm
Test Reference Channel 10	-6.9375	-22.05	55 cm
Test Reference channel 11	-7.5756	-24.1	60cm
Test Reference channel 12	-8.2125	-26.15	65cm



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D-PHY 规范及CTS更新



D-PHY 2.0 : Approved Mar 8, 2016



D-PHY 2.1 : Approved Mar 28, 2017

D-PHY 3.0 : Adopted on Jul 2021

- Up to 11000Mbps with Short reference channel
- RxEQ CTLE
- Lower LP voltage level from 1.2V to 1V
- HS-Idle (lower latency)
- Programmable Preamble(RX PVT calibration due to LP signal)



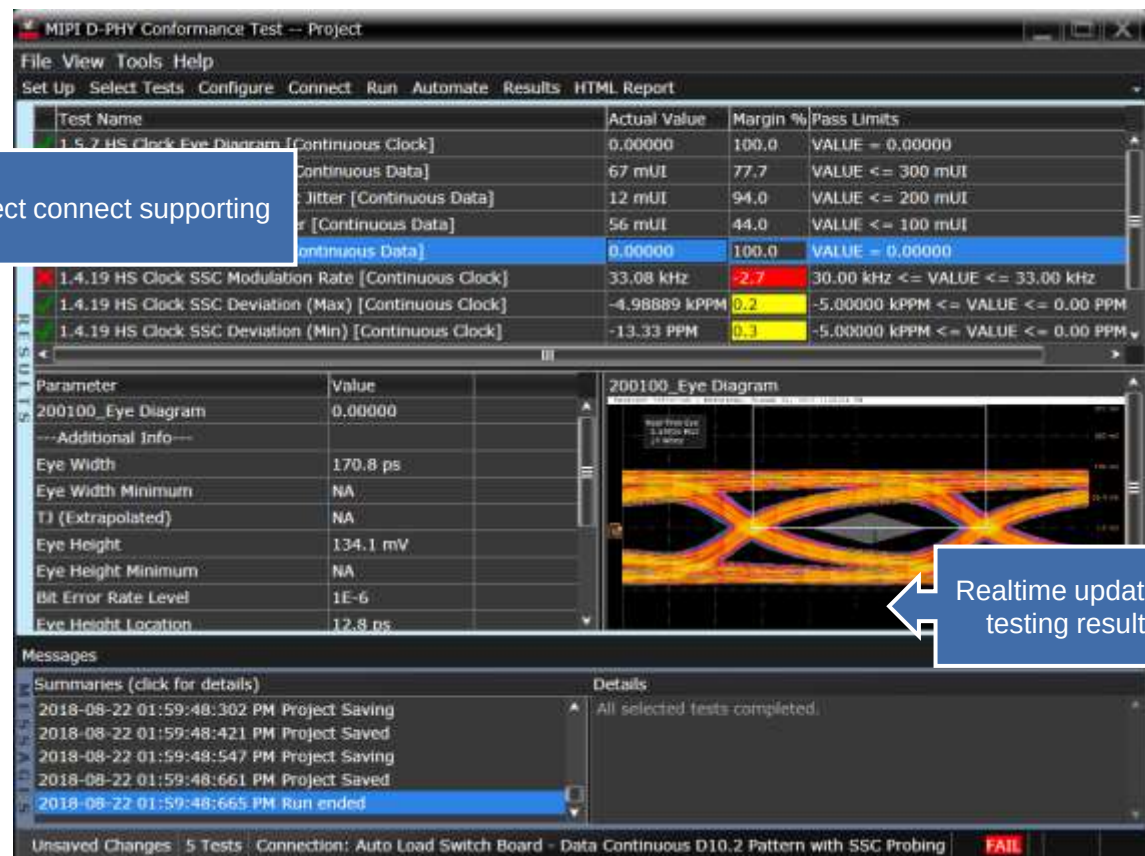
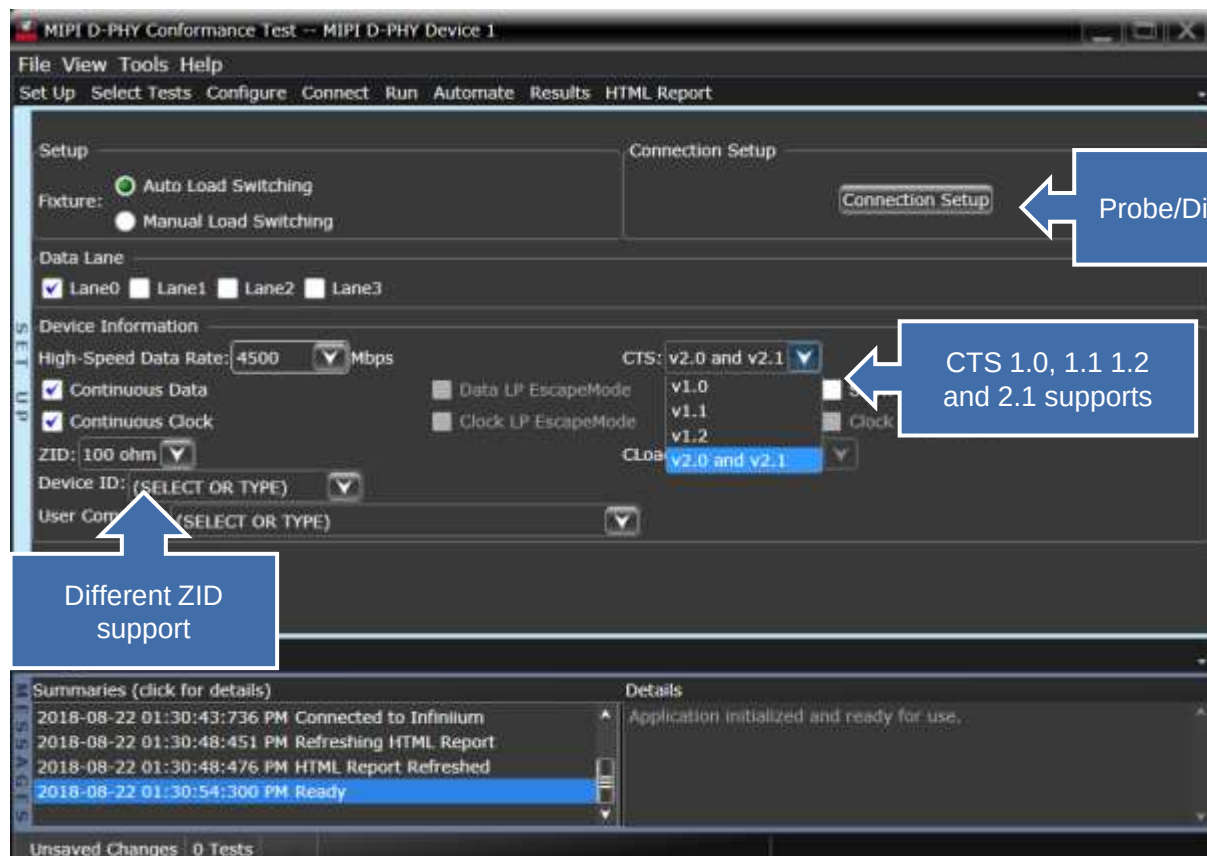
CTS 1.2 : April 24, 2017



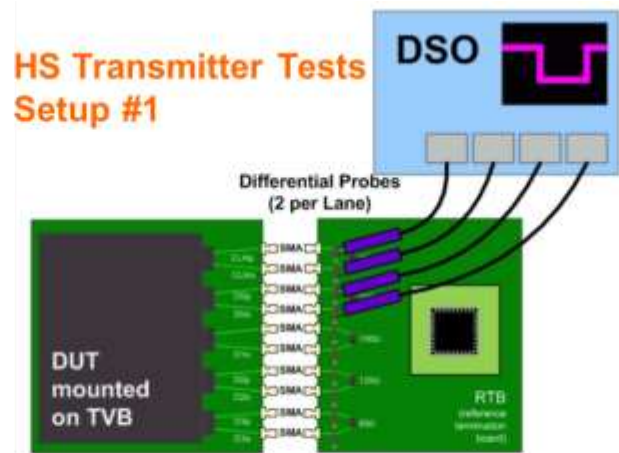
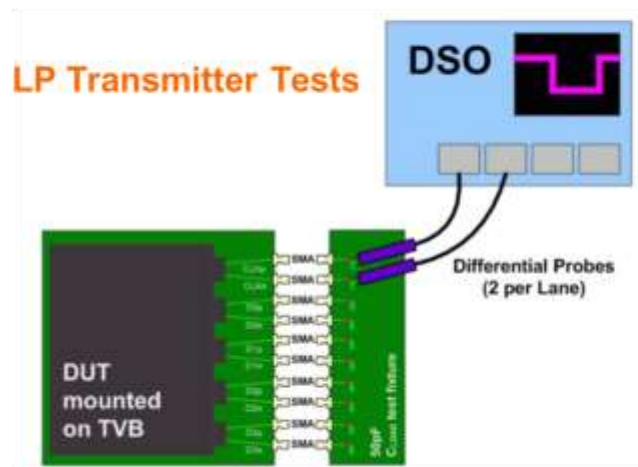
CTS 2.1 : Oct 2018

- Test 1.5.7 – HS-TX Data and Clock Eye Diagram
- Test 1.4.19 – TX Spread Spectrum Clocking(SSC) Requirement
- Test 1.4.18 - Clock Lane HS Clock Delta UI(new method)
- Test 1.4.20 - Clock lane HS Clock Period Jitter
- Test 1.5.9 - Alternate Calibration Sequence
- Test 1.5.10 - Preamble Sequence

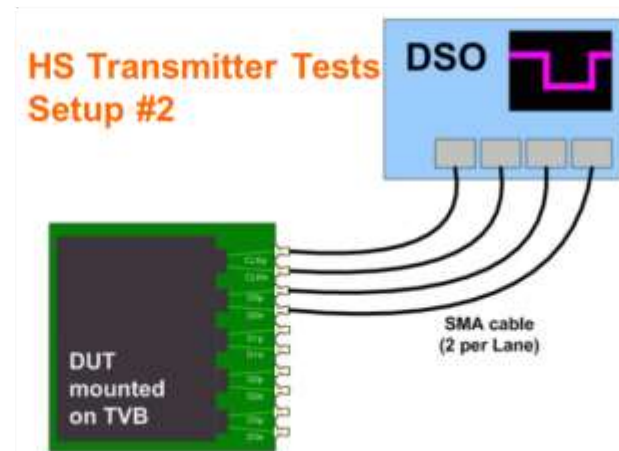
Keysight D9020DPHC D-PHY Tx 测试软件



D-PHY Tx 测试组网图(D-PHY CTS v2.1)和要求



Continuous stream of HS bursts



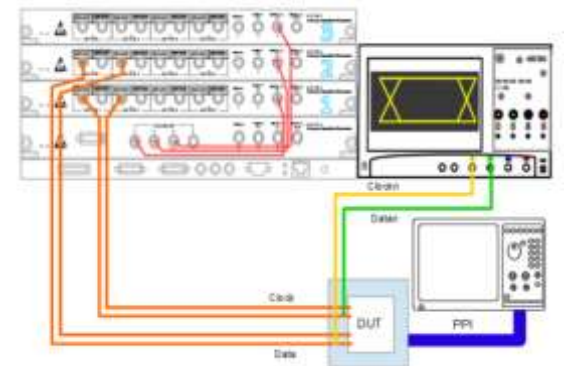
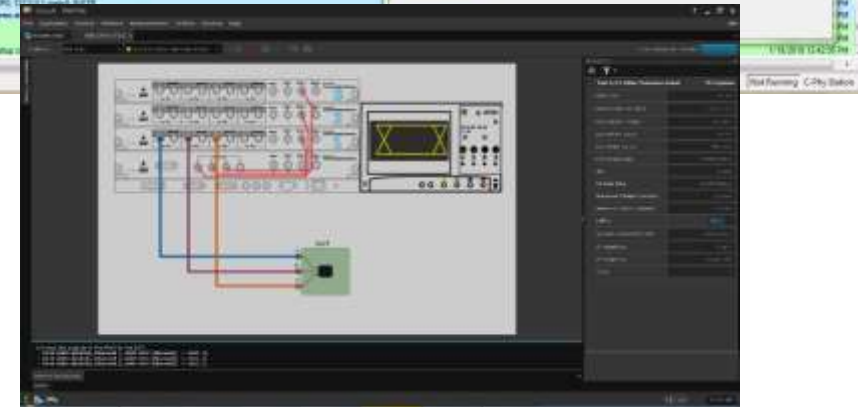
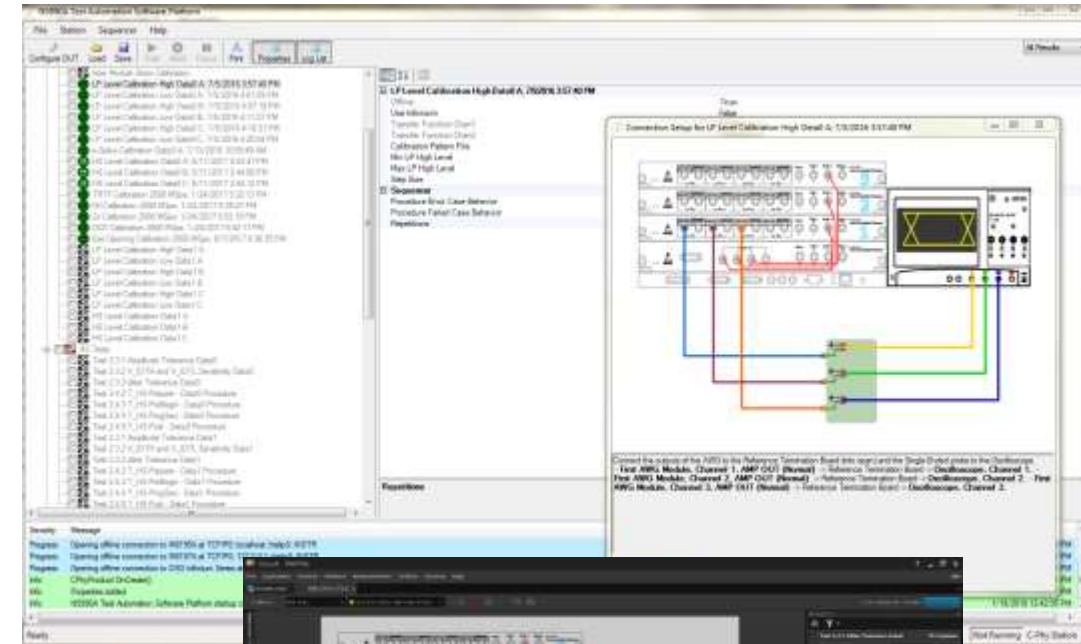
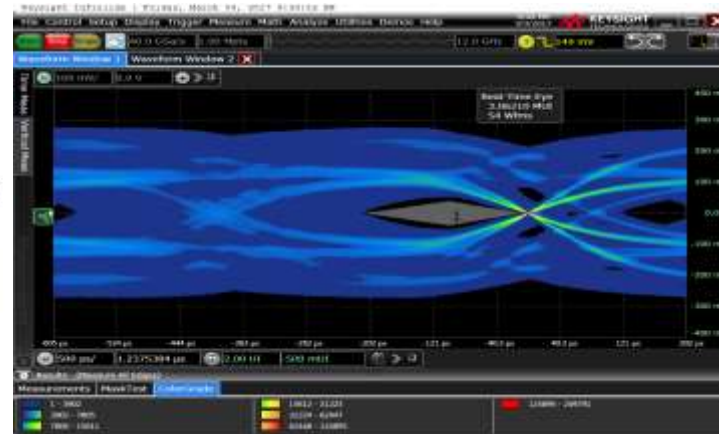
Continuous stream of HS data only

- ✓ D-PHY v2.1 CTS supporting
 - HS-TX clock/data Eye Diagram
 - TX Spread Spectrum Clocking(SSC)
 - HS Clock Delta UI
 - HS Clock Period Jitter
 - Alternate calibration sequence
 - Preamble sequence
- ✓ And more
 - Jitter test

D-PHY v2.0 或以上测试需要Burst模式和连续模式，眼图测试需要使用连续模式

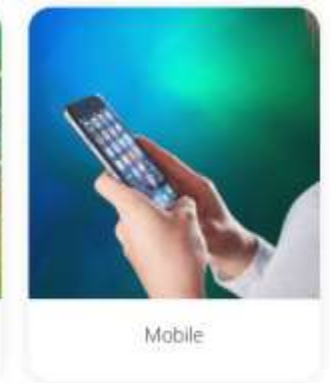
MIPI C/D PHY Rx testing solution

- 基于M8195A AWG平台
- 单模块或多模块支持C-PHY v2.0, D-PHY v2.1

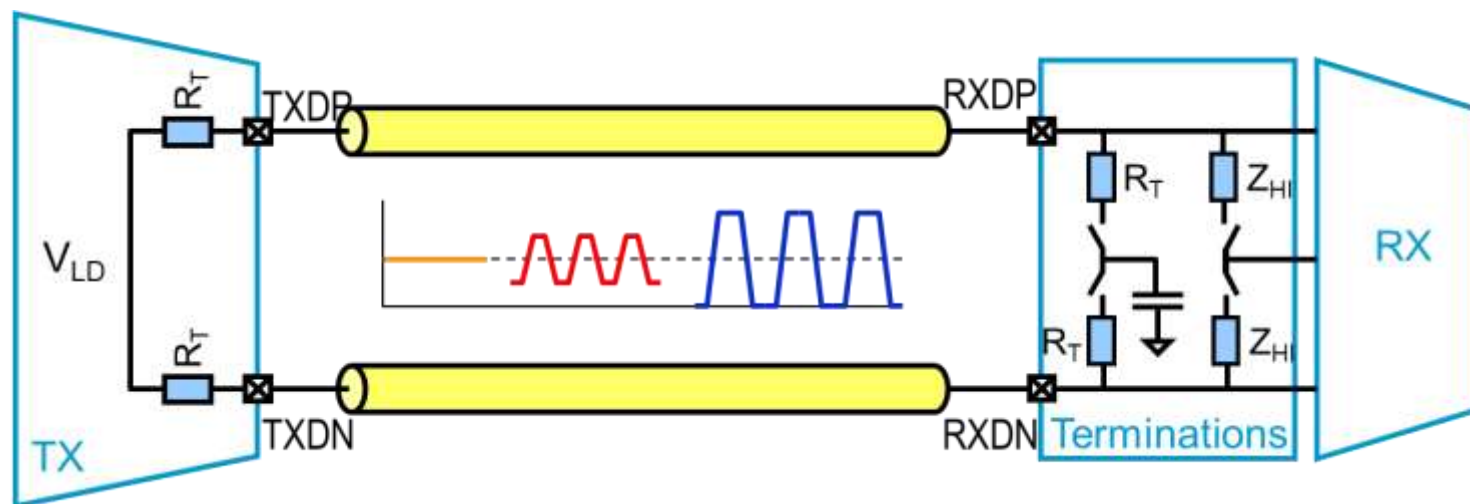


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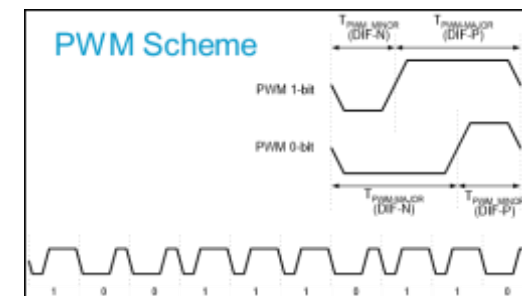
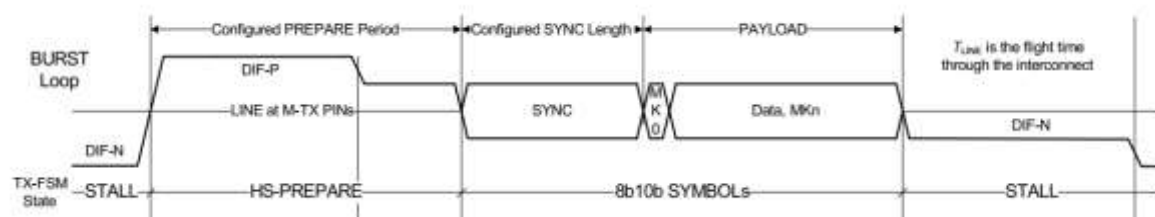
M-PHY 物理层架构



HS_Gear	data rate [Gb/s]		termination	
	A	B	default	optional
4	1984	11960	RT	NT
3	4992	5830	RT	NT
2	2496	2915	RT	NT
1	1248	1458	RT	NT

M-PHY-Type-I Module (PWM)				M-PHY-Type-II Module (NRZ)			
Type-I Baseline Module			termination		Type-II Baseline Module		
LP Gear	data rate [Mb/s]		default	optional	data rate = f _{sys} [Mb/s]		
0	0.01 - 3		NT	RT	f _{sys} = f _{ref}		
1	3 - 9		NT	RT	NT RT		
2	6 - 18		NT	RT	f _{ref} = 19.2, 26, 38.4 or 52 MHz		
3	12 - 36		NT	RT	NT = Not terminated		
4	24 - 72		NT	RT	RT = Resistively terminated		
5	48 - 144		NT	RT			
6	96 - 288		NT	RT			
7	192 - 576		NT	RT			

- Unidirectional
- DC Coupled
- High Speed NRZ (HS) and Lower Speed (LS) modes
 - Common LS mode: Pulse Width Modulation (PWM)
- Always differential and 8b/10b coded
- High and low voltage swing operations
- Terminated (100 ohm) or not terminated operation



M-PHY Specification and CTS Update: v4.1 to v5.0



Spec v4.1 : Approved Mar 28, 2017
v4.1 Errata : Approved May 17, 2018



Spec v5.0 : Approved Sept 29, 2021

- Doubling of data rate (23.32Gbps)
- CH1 mandatory, CH2 optional for G5
- New pkg model and ref EQ for G5
- Removed PWM G0, G2-G7
- Removed HS Unterminated mode
- Removed OMC support



CTS v4.1 (v1.1) : Approved Apr 14, 2020

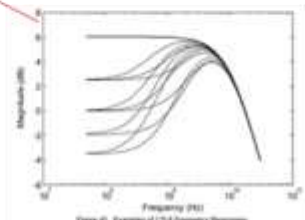
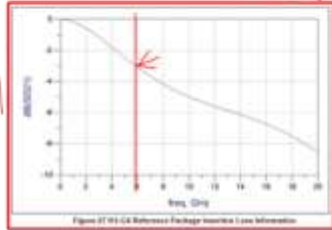
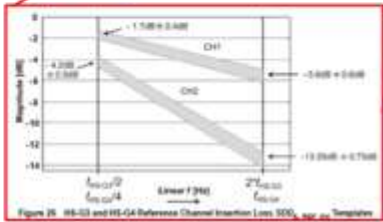
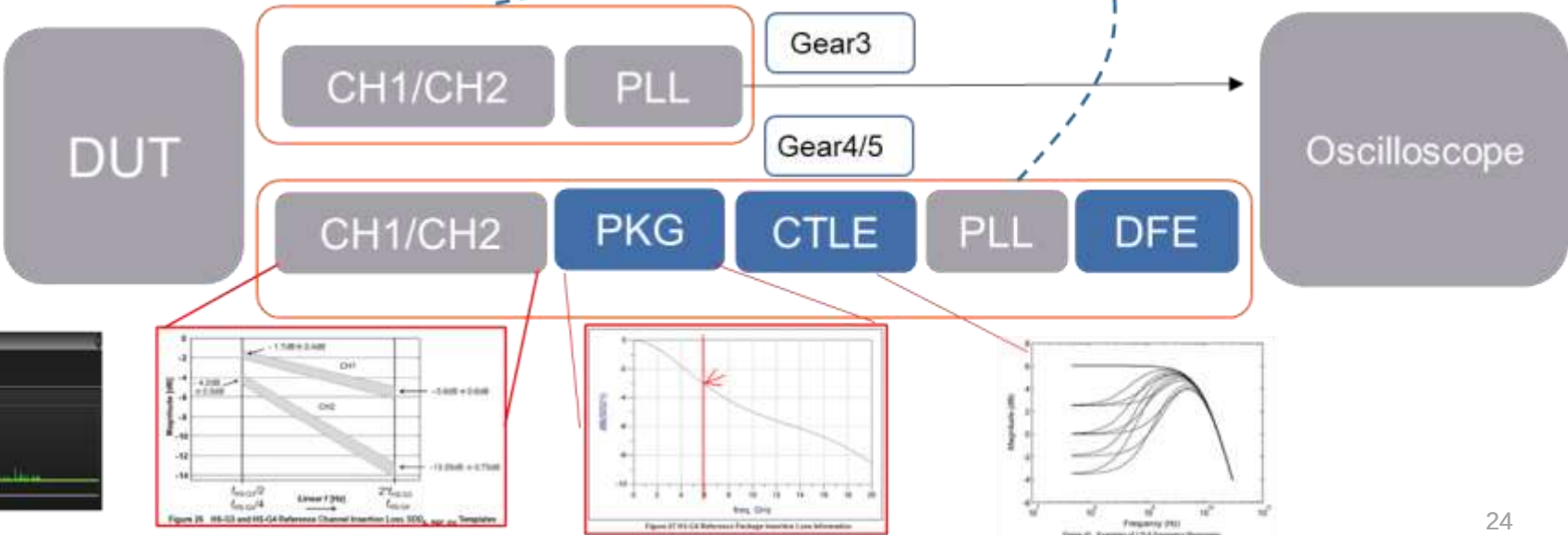
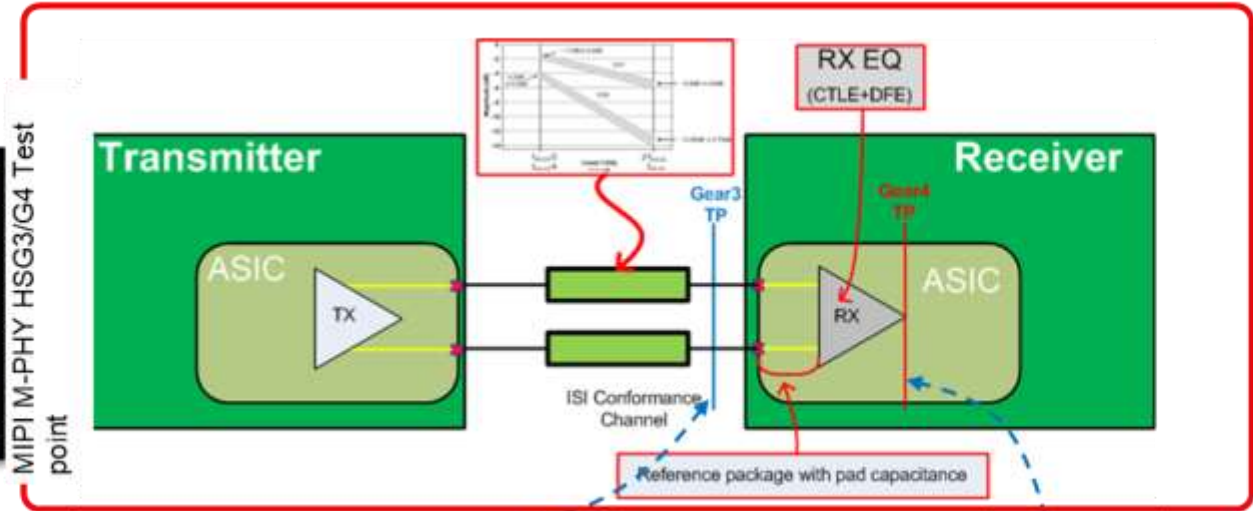
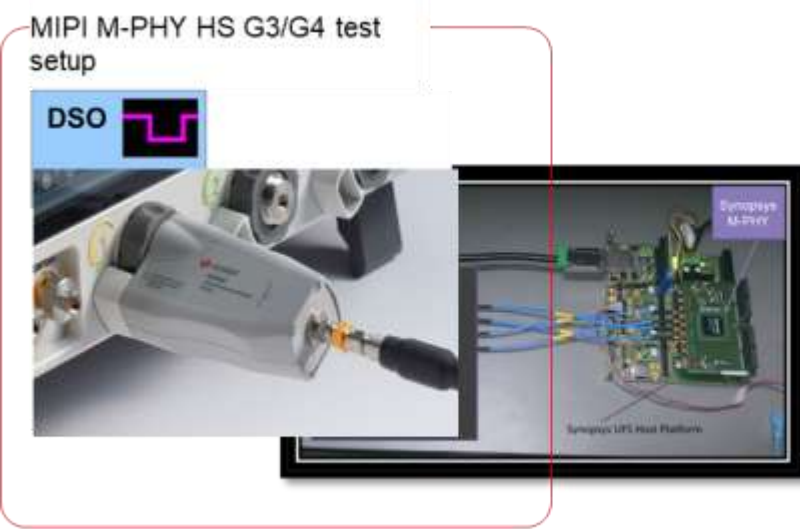


CTS v5.0 : Approved June 2, 2022

- Added HS-GEAR5 requirements
- Updates to TX/RX Eye Tests (New pkg model and ref CTLE)
- Updates to TX/RX Vcm, Vdiff, and Freq tests
- PWM tests are now PWM-G1 only

MIPI M-PHY 测试组网架构的变化

	ISI Channel Embedding	Ref Pkg Embedding	CTLE/DFE
GEAR1	No	No	No
GEAR2	No	No	No
GEAR3	Yes	No	No
GEAR4	Yes	G4 Pkg Model	G4 CTLE
GEAR5	Yes	G5 Pkg Model	G5 CTLE



M-PHY G5 参考通道和接收均衡

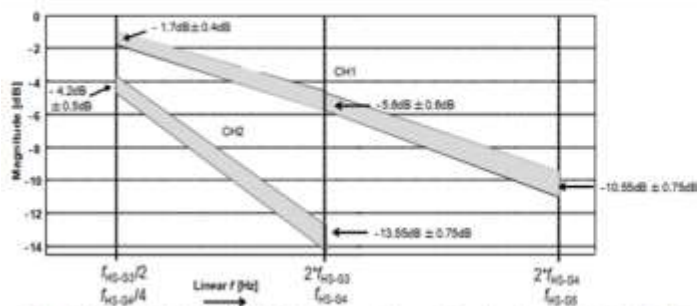


Figure 21 HS-G3, HS-G4, and HS-G5 Reference Channel Insertion Loss SDDIL_REF_CH Templates

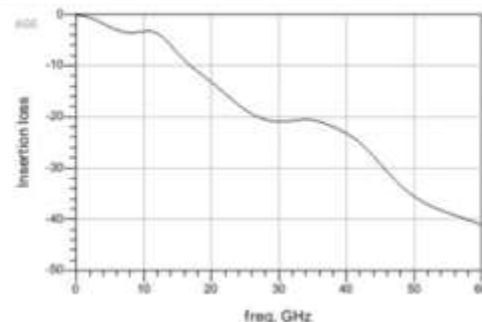
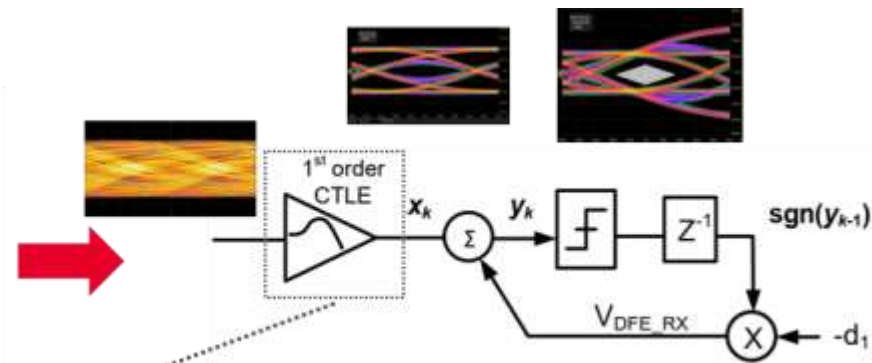


Figure 29 HS-G5 Reference Package plus Effective Pad Capacitance Insertion Loss



$$H(s) = \frac{A_{DC} w_{P1} w_{P2}}{w_z} \frac{s + w_z}{(s + w_{P1})(s + w_{P2})}$$

HS-RX Reference Equalizer for HS-G5					
A_{AC}	-	-	12	dB	CTLE AC gain
A_{DC}	-6	-	6	dB	CTLE DC gain
f_z	0.4	-	2.5	GHz	CTLE zero frequency
f_{P2}	-	-	20	GHz	CTLE second pole frequency
V_{DFE_RX}	-60	-	60	mV	DFE feedback voltage signal

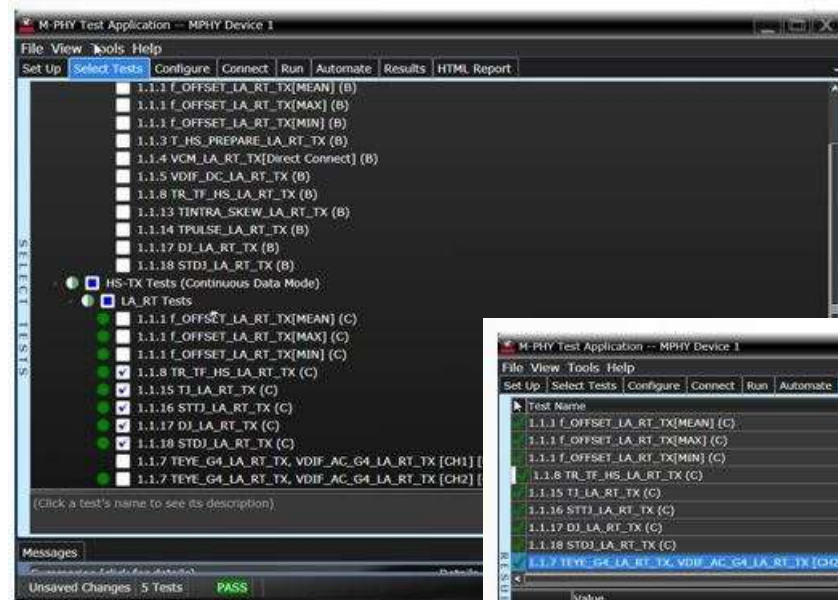
Note:

- f_{P1} is determined by other parameters: $f_{P1} = f_z * 10^{(A_{AC} - A_{DC})/20}$

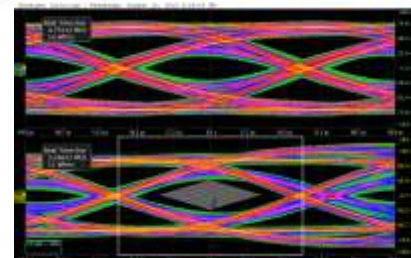
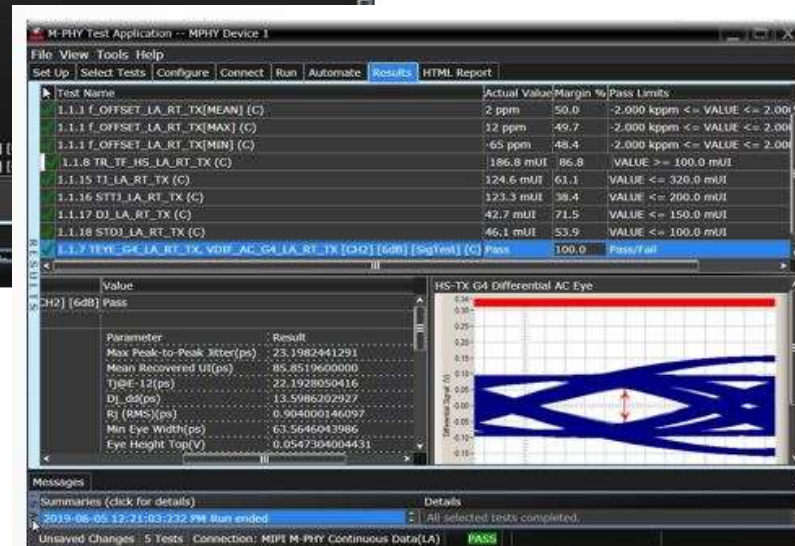
Table 11 Recommended HS-G5 CTLE Parameter Summary (for Large Amplitude with CH1)

CTLE Filter	AC Gain (A_{AC})	DC Gain (A_{DC})	Zero Pole (F_{Pz})	First Pole (F_{P1})	Second Pole (F_{P2})
1	11.75 dB	1.46 dB	2.01 GHz	6.58 GHz	20 GHz
2	11.86 dB	1.75 dB	2.06 GHz	6.59 GHz	20 GHz
3	11.74 dB	2.03 dB	2.03 GHz	6.21 GHz	20 GHz
4	11.55 dB	2.99 dB	1.80 GHz	4.84 GHz	20 GHz

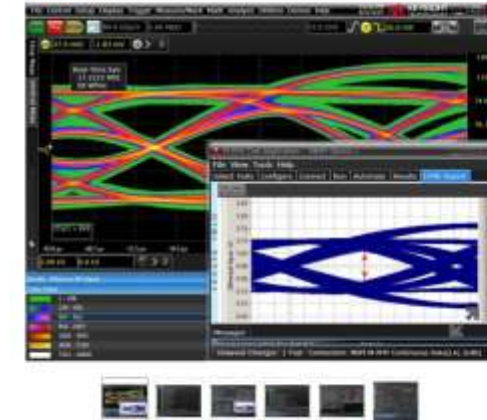
Keysight M-PHY G5 Tx 一致性测试方案



D9050MPHC



SW00MIPI MIPI Validation License Suite



The MIPI Validation License Suite is part of the subscription based Oscilloscope Compliance Test Software Suites. This suite covers Tx Validation licenses for MIPI with coverage across the MIPI technologies M-Phy, D-Phy and C-Phy. Together with the subscription model, this enables the support and coverage continuity as the MIPI technology progresses through revisions.

Get a configured quote

Get Quote

- Sold by Keysight Direct Sales - Call for availability
- Sold by Authorized Sales Partners - Check availability
- See Buy or Rent Options
- View Options and Upgrades

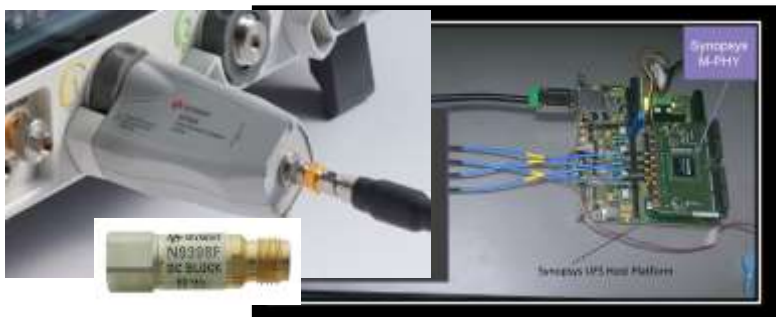
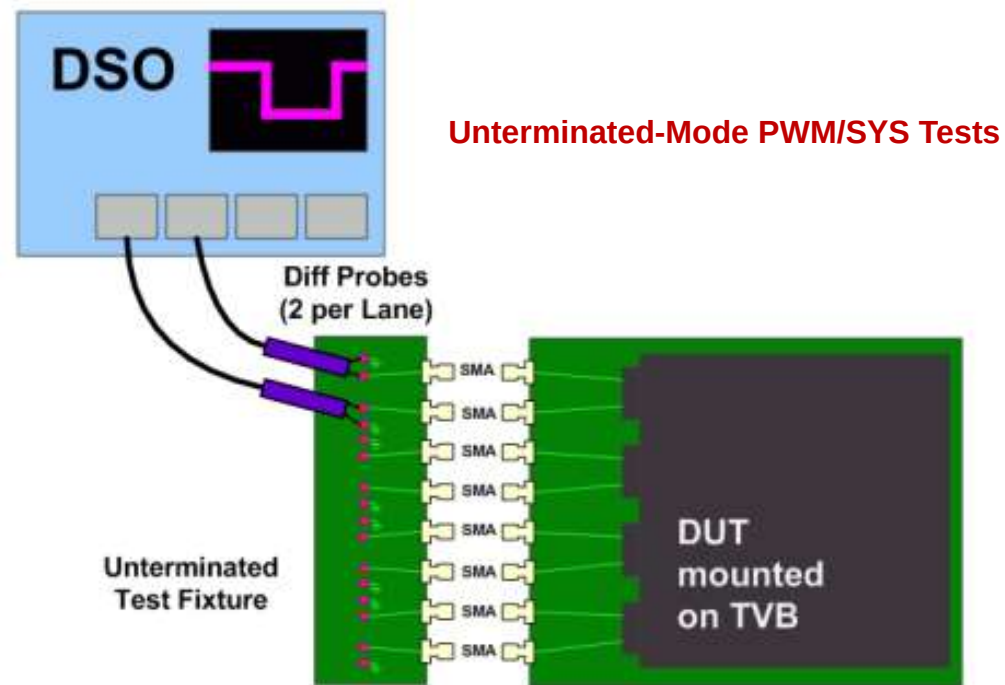
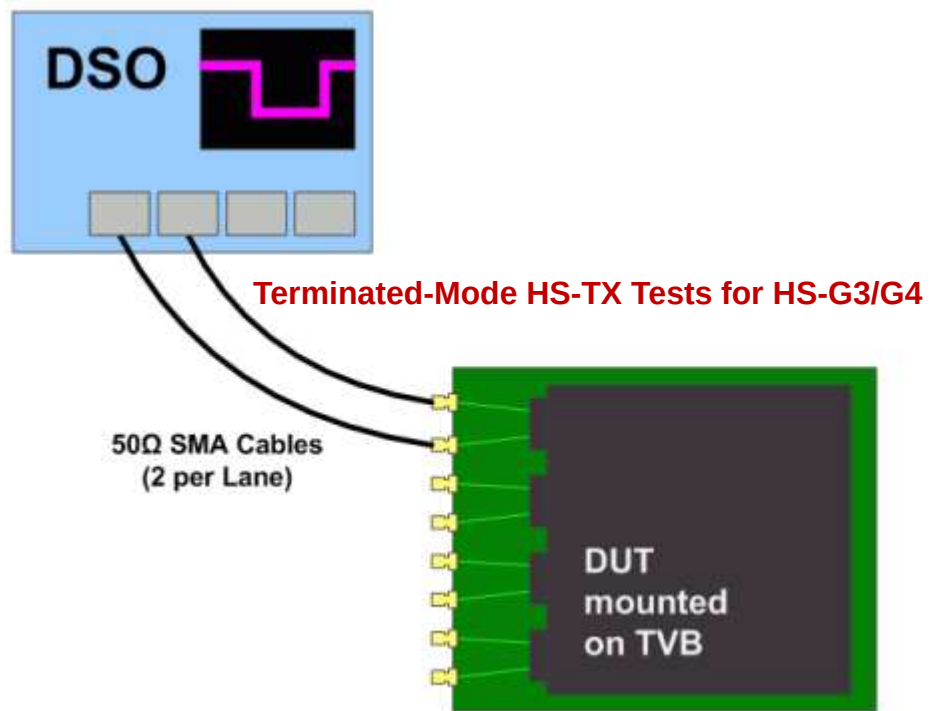
SW00MIPI = All TX conformance apps for C/D/M-PHY
SW02MIPI = SW00MIPI + all MIPI protocol apps

JEDEC Universal Flash Storage (UFS) v3.0 specification
*需D9020JITA选件

UFS reference clock (Informative)¹⁾

- Reference clock output high voltage (VOH)(informative)
- Reference clock output low voltage (VOL)(informative)
- Reference clock output rise time (TORISE)
- Reference clock output fall time (TOFALL)
- Reference clock frequency error (FERROR)
- Reference clock duty cycle (TDC)
- Reference clock phase noise (N)
- Reference clock noise floor density (NDENSITY)

M-PHY G5 Tx 一致性测试组网



M-PHY G5 示波器带宽要求

Keysight 提议，CTS变更通过

Andy Baldman 2022-10-21 19:10:57 UTC Comment 2 [reply] [-]

Formal text content (taken from presentation attached above, copied here for convenience):

Proposed new text for CTS Annex A.1.1, item (2):

2. 1 x Four-Channel Real-Time Digital Storage Oscilloscope (DSO), 5/10/20/25 minimum bandwidth for HS-G1/G2/G3/G4 measurements, respectively. Note that these values may be subject to modification, however the values above are conservative estimates based on the Bandwidth = 0.35/Risetime rule of thumb, and the fact that the minimum TX risetime spec limit is 0.1UI, which for HS-G3B (5.8Gbps) = $0.35 / 17.2\text{ps} = 20.3\text{GHz}$.

Also, because the G4 measurements are made through a reference channel, the bandwidth is limited to 25GHz.

For G5, a minimum bandwidth of 33GHz may be used to demonstrate conformance for the required (i.e., normative) TX tests. If the informative TX jitter tests 1.1.15-18) are to be performed, a minimum of 40GHz is required. Also, a minimum of 40GHz is required for performing the jitter calibration measurements for the purpose of RX testing.

Also, add the following statement to A.2.1 (as new list item 3, after item 2, "An ISI Compliance Channel..."):

3. 1 x Four-Channel Real-Time Digital Storage Oscilloscope (DSO), with 5/10/20/25/40 GHz minimum bandwidth for HS-G1/G2/G3/G4/G5, respectively.

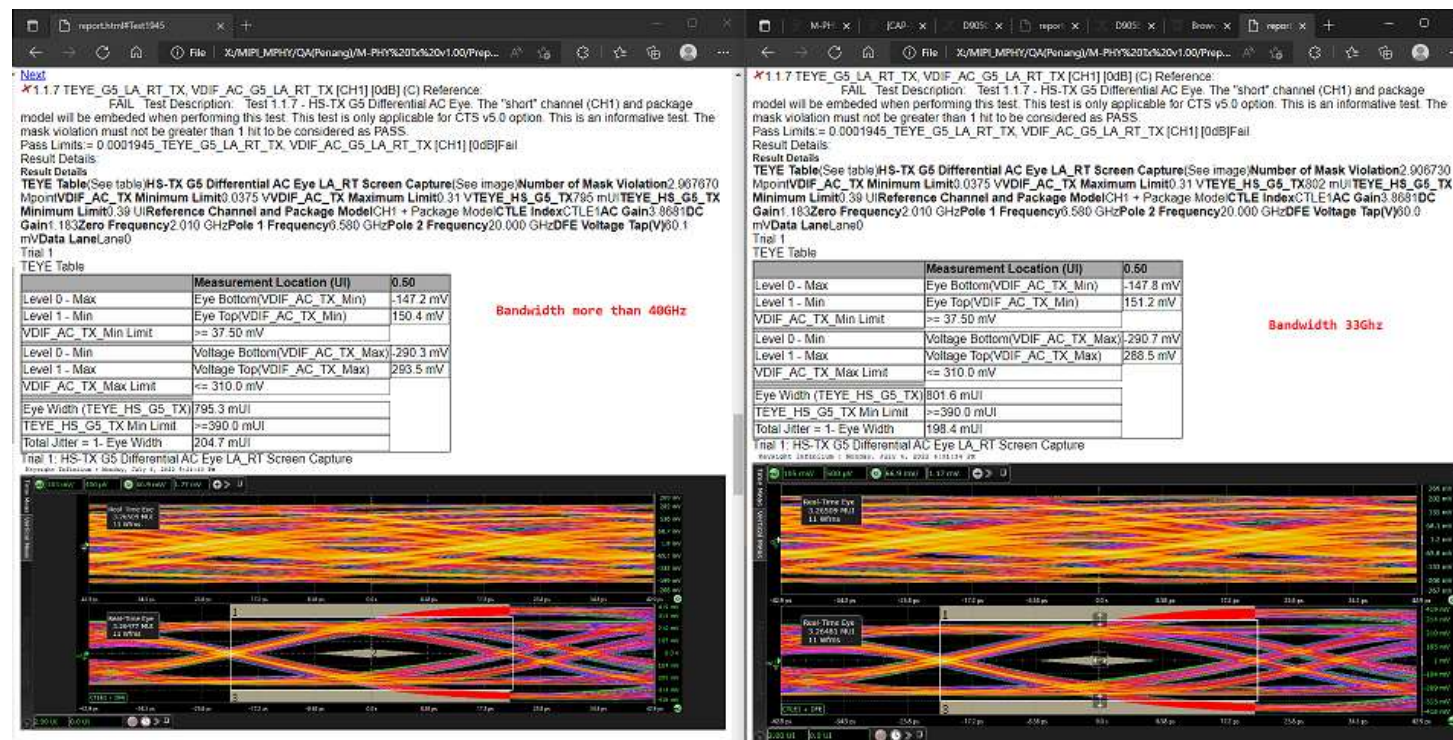
Also, add the following to the Possible Problems sections of Tests 1.1.15-18:

"If this informative test is to be performed, a minimum oscilloscope bandwidth of 40GHz is required. See Annex A.1.1."

Kirill Dimitrov 2022-11-07 15:30:49 UTC Comment 3 [reply] [-]

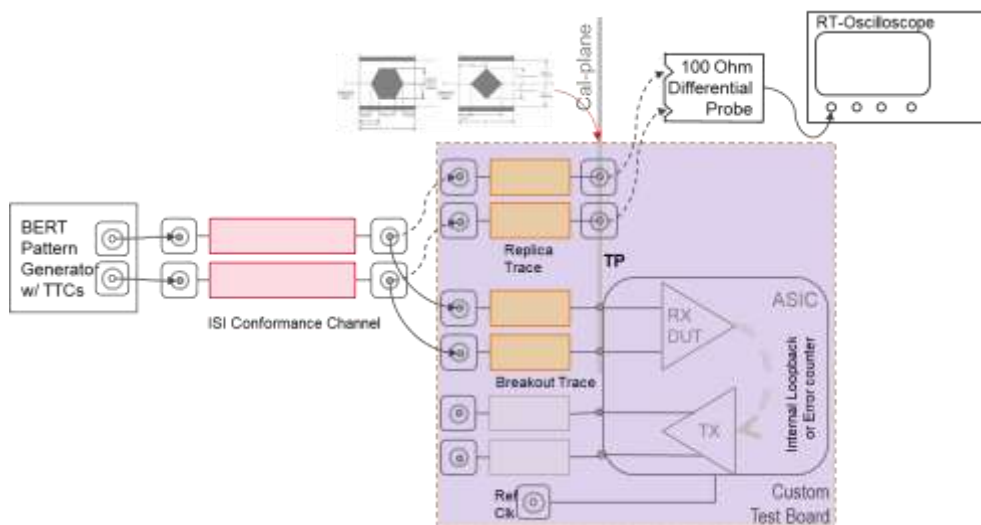
Per WG discussion modify the CTS according to the proposal in comment #2 from 21-10-2022

- Modify CTS to allow using 33GHz for Normative TX tests
- Add notes to say 40GHz is required for Informative TX jitter tests (1.1.15-18)
- Require 40GHz for RX eye calibration

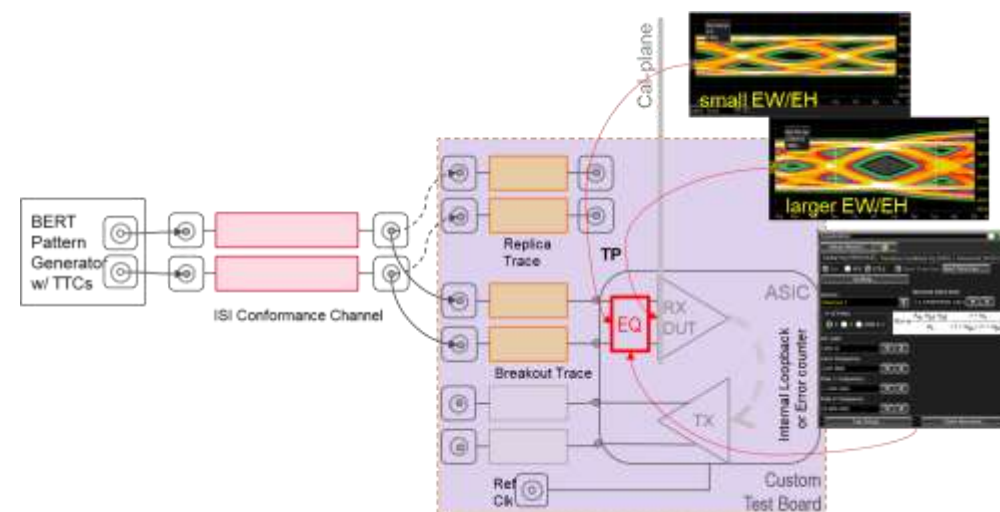


M-PHY Rx 校准及测试组网

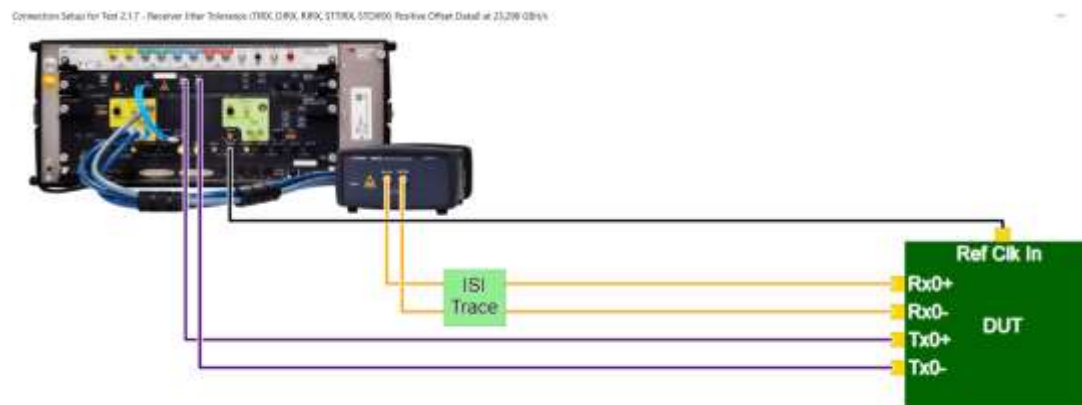
Rx Calibration HS-GEAR1 to GEAR3



Rx Calibration HS-GEAR4 to GEAR5



Rx Test HS-GEAR1 to GEAR5



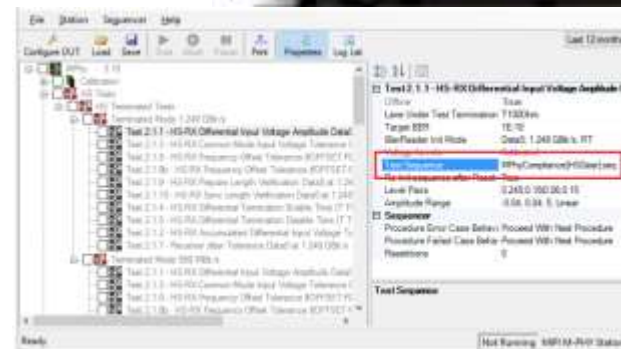
M-PHY G5 Tx Rx Solution

D9050MPHC
MIPI M-PHY Conformance Test Software
for Infiniium Oscilloscopes



- HS-G1 through G5
- CTS v5.0
- Newer solution

Rx Solution M8040A



- HS-G1 through G5
- N5991A Software
 - N5991MM5A
 - N5991MM5E

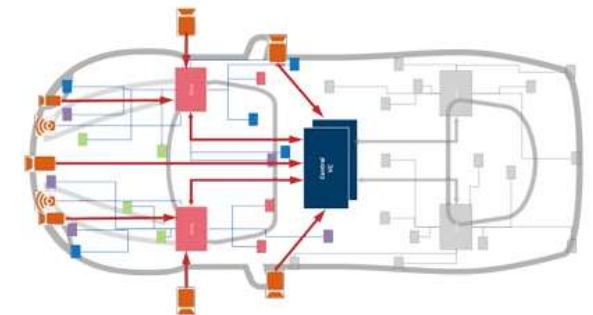
Agenda

- MIPI Technology Overview
- MIPI C-PHY Update and Solution
- MIPI D-PHY Update and Solution
- MIPI M-PHY Update and Solution
- **MIPI A-PHY Update and Solution**



A-PHY-Based Zonal Architecture

- Simplification of zonal ECU
 - Low computing overhead
 - Lower protocol overhead – Maintain native protocols for MIPI CSI-2 (e.g., camera) or Ethernet (e.g., lidar)
 - Designed for ultra-low PER at high noise environment for the entire lifespan of the vehicle
- Future-looking design and easy migration path
 - Scalable downlink speed from 2Gbps to 64Gbps over a single cable
 - Flexible and rich protocol support
 - Layered security scheme supporting variety of use cases
 - Embedded functional safety
- Guaranteed interoperability and backward/forward compatibility



Standardized Automotive SerDes

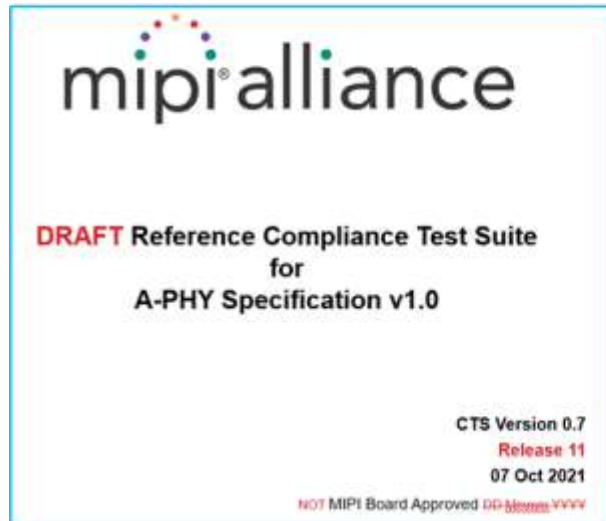
MIPI a-phy, automotive serdes alliance

- How to enable next-gen applications?
- A new standard in collaboration: OEM, Tier 1, Silicon, Test
- Definition and adoption of test methods relevant to automotive



MIPI A-PHY v1.0 CTS v0.7

Transmitter Items



Group 1 PMD Transmitter Electrical Specification Tests for Source Devices

- Test 2.1.1 TX Power Spectral Density Mask
- Test 2.1.2 TX Maximum Output Droop
- Test 2.1.3 TX Timing Jitter
- Test 2.1.4 TX Symbol Rate Accuracy
- Test 2.1.5 NRZ Downlink TX Eye Opening
- Test 2.1.6 PAM-X Transmitter Linearity
- Test 2.1.7 Downlink TX Return Loss

Group 3 PMD Transmitter Electrical Specification Tests for Sink Devices

- Test 2.3.1 TX Power Spectral Density Mask
- Test 2.3.2 TX Maximum Output Droop
- Test 2.3.3 TX Timing Jitter
- Test 2.3.4 TX Symbol Rate Accuracy
- Test 2.3.5 Uplink TX Return Loss

Receiver Items

Group 2 PMD Receiver Electrical Specification Tests for Source Devices

- Test 2.2.1 Uplink RX Bit Error Rate
- Test 2.2.2 RX Symbol Rate Frequency Tolerance

Group 4 PMD Receiver Electrical Specification Tests for Sink Devices

- Test 2.4.1 Downlink RX Bit Error Rate
- Test 2.4.2 RX Symbol Rate Frequency Tolerance

AE2010T A-PHY/ASA Transmitter Test Solution

Device Under Test

SerDes Standard: MIPI A-Phy Ver1.0 MIPI A-Phy Ver1.0 ASA Beta Ver1.0

Link Direction:

Baud Rate / Gear / Speed Grade:

SG1	SG2	SG3	SG4	SG5
☒	☒	☒	☒	☒
2G	4G	8G	12G	16G

(NRZ-8B/10B) (NRZ-8B/10B) (PAM4) (PAM8) (PAM16)

Spectral Settings

Spectral Analysis: ☒ Oscilloscope ☐ Spectrum Analyzer

Connection

DUT Connection Type: ☒ Twisted Pair (Two Channels) ☐ Twisted Pair (One Differential Probe) ☐ Coaxial (single-ended)

Vector Network Analyzer

☒ Manual Calibration Configure ...



SerDes Test Application -- New Device1

File View Tools Help

Set Up **Select Tests** Configure Connect Run Automate Re

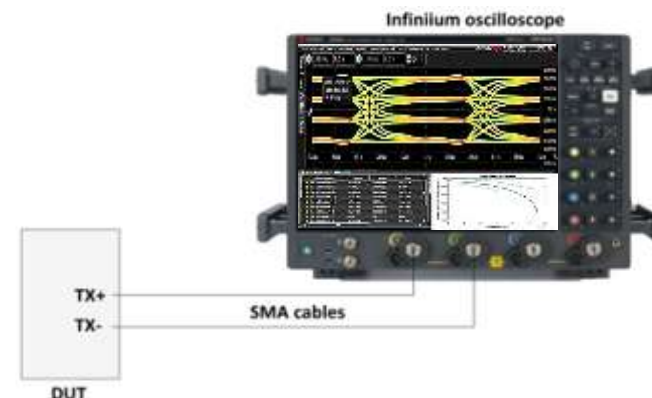
- ☐ SerDes Tests
 - ☐ MiPi Tests
 - ☐ Speed Grade 1 (2G)
 - ☐ Speed Grade 2 (4G)
 - ☒ Speed Grade 3 (8G)
 - ☐ Test Mode 1 Tests
 - ☐ Transmitter Power Spectral Density
 - ☐ Test Mode 2 Tests
 - ☐ TX Maximum Output Droop (Positive)
 - ☐ TX Maximum Output Droop (Negative)
 - ☐ Test Mode 3 Tests
 - ☐ Transmitter Timing Jitter
 - ☐ TX Symbol Rate Accuracy
 - ☐ Test Mode 4 Tests
 - ☐ PAM-X TX Linearity RMS
 - ☐ PAM-X TX Linearity Peak
 - ☐ Return Loss
 - ☐ Speed Grade 4 (12G)
 - ☐ Speed Grade 5 (16G)
 - ☐ Test Mode 1 Tests
 - ☐ Transmitter Power Spectral Density

AE2010T A-PHY/ASA Transmitter Test Coverage

MIPI A-PHY 1.0 CTS version 0.7

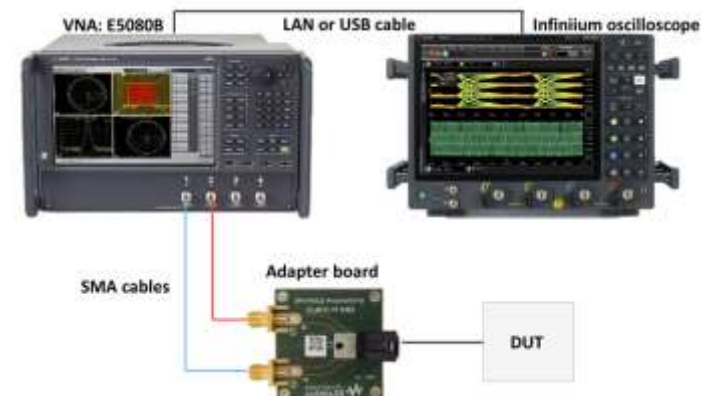
PMD Transmitter Electrical Test for Source Devices (Downlink)	
2.1.1	TX Power Spectral Density Mask
2.1.2	TX Maximum Output Droop
2.1.3	TX Timing Jitter
2.1.4	TX Symbol Rate Accuracy
2.1.5	NRZ Downlink TX Eye Opening
2.1.6	PAM-X Transmitter Linearity
2.1.7	Downlink TX Return Loss

PMD Transmitter Electrical Test for Sink Devices (Uplink)	
2.3.1	TX Power Spectral Density Mask
2.3.2	TX Maximum Output Droop
2.3.3	TX Timing Jitter
2.3.4	TX Symbol Rate Accuracy
2.3.5	Uplink TX Return Loss



ASA Specification 1.01²

Standard test number	Description
4.4	PMA Electrical Parameters
4.5.4	MDI Return Loss



AE6960A Keysight SMA to H-MTD adapter board

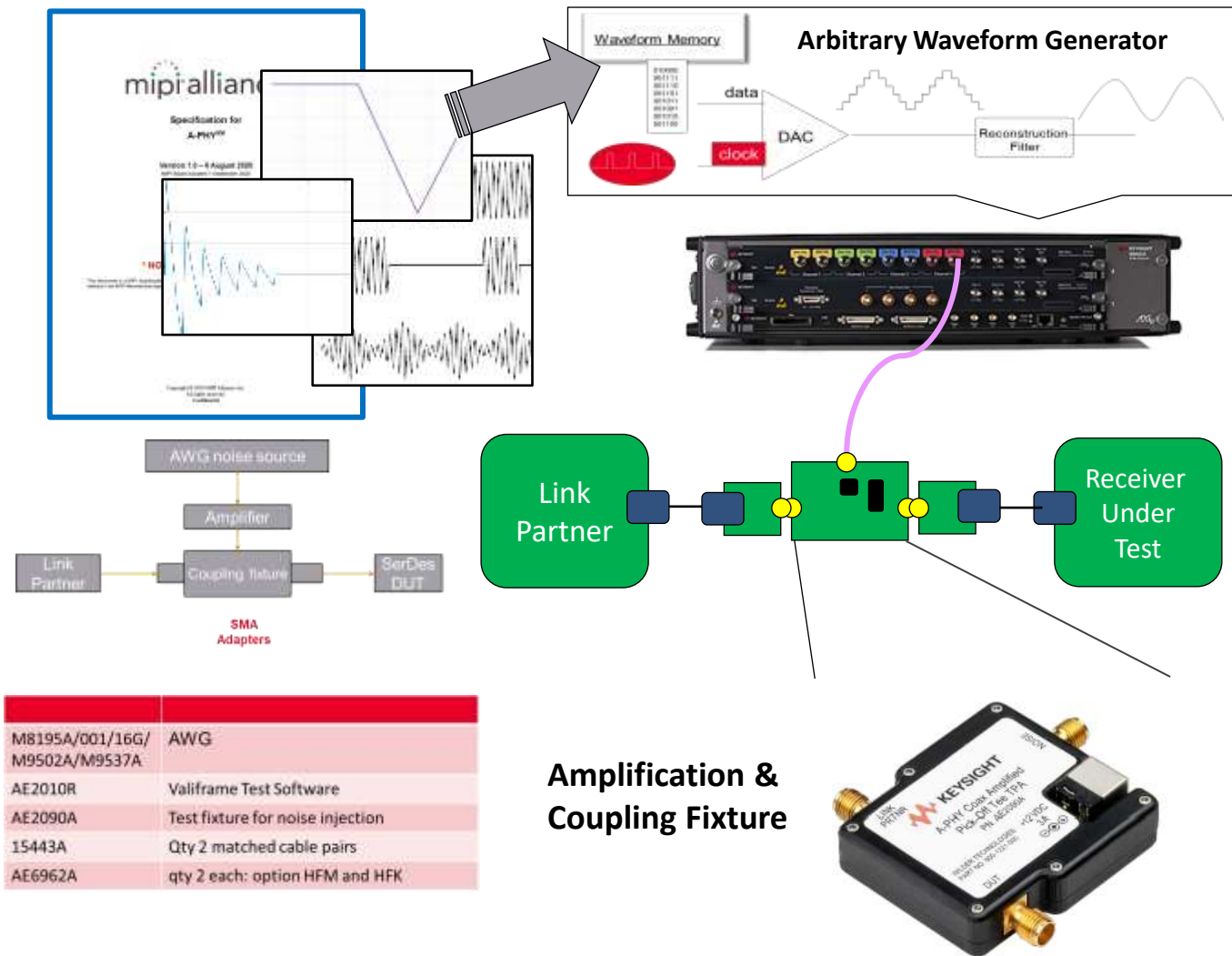


AE6965A Rosenberger H-MTD to 2.92 Y adapter

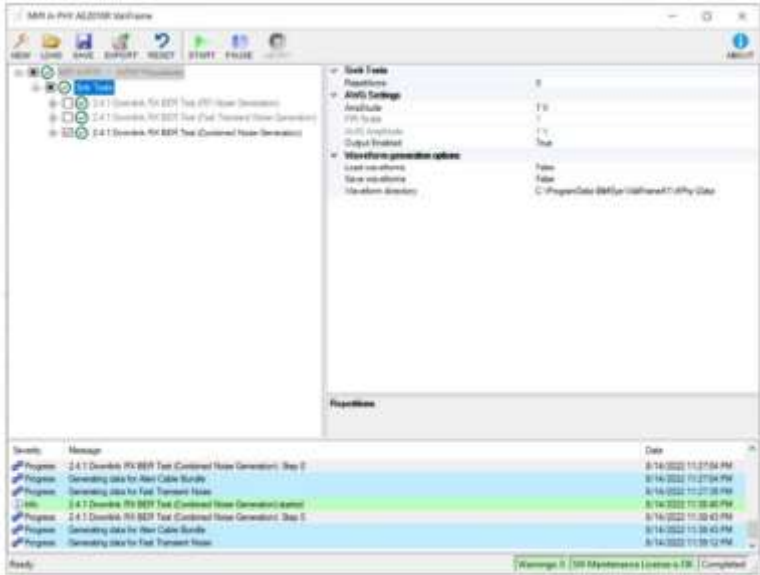


AE6962A Rosenberger HFM (High-speed FAKRA Mini) to 2.92

AE2010R Automotive SerDes MIPI A-PHY Receiver Test Solution



- Noise will be coupled to an active link
- DUT's Receiver circuitry will be stressed to maintain BER
- Error count will be maintained in DUT register space
- Register space accessed in-band or through sideband access



AE2010L Automotive SerDes Channel Test Solution

MIPI A-PHY 1.0

Section	Description	Test parameter
6.6.2	Cable Transmission Line Interconnect Structure	IL, RL, Coupling/screening/unbalanced attenuation
6.6.3	End Node Interconnect Structure	IL, RL, ANEXT

Measurement descriptions for the listed test parameters.

Descriptions and Definitions	
IL (S_{dd21})	Insertion Loss (Differential Mode)
RL (S_{dd11} , S_{dd22})	Return Loss (Differential Mode)
ANEXT B, C, D, E (S_{dd31} , S_{ddx1})	Alien Near End Crosstalk loss

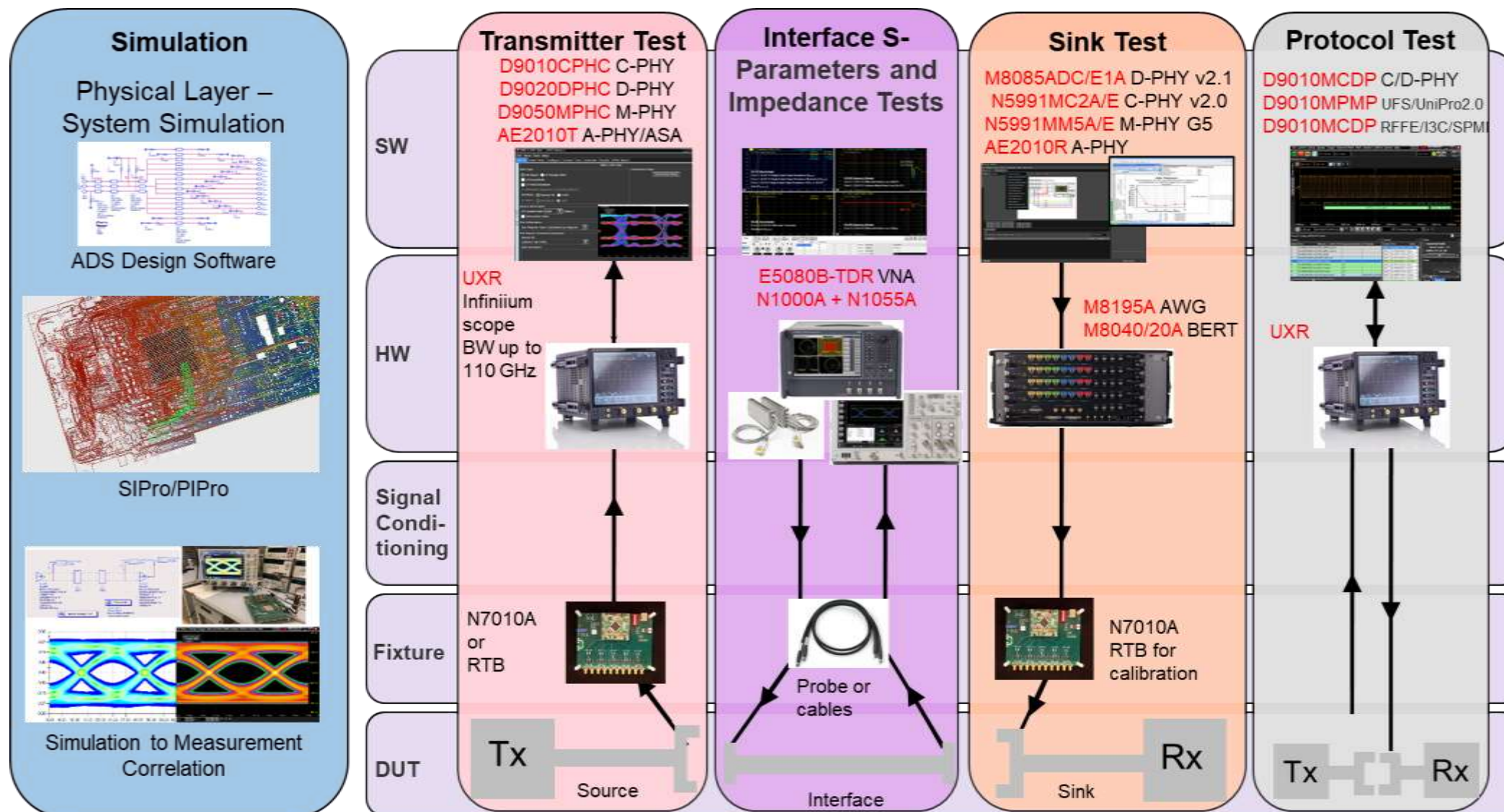
There are both coax (Single ended: Syx) and SDP (Differential: Sddyx) test modes.

 Keysight AE2010L/AE2010L Automotive Channel Test Software	
GENERAL INFORMATION	
Location	C:\Program Files\Keysight\1 Test Automation\Package\Automotive\Channel\AE2010L 1.0.0\Files
Version	000001
Specification	MIPI Alliance A-PHY Interface, Version 1.0, 8 August 2013
Test Mode	Coaxial
Data Rate	2000 Mbps (Serial 1)
Instrument	Keysight Technologies, CS080B, AN5530546, A.13.90.00
Total Use Ports	8 out of 8
Port Name	MIPI04_123456_02
Measurement Setup Type	Predefined Setup
Source Start	0.1 MHz
Source Stop	4500 MHz
Sweep Type	Logarithmic
Sweep Points	1000
Output Power	-10 dBm
Min. Bandwidth	0.0005 MHz
Imp. Differential Mode	200 Ohm
Imp. Common Mode	200 Ohm
Enable Crosstalk	False
Humidity	30%
Temperature	23°C

Software - compliance test software is automated. PLTS adds customization.		
Required	Test Automation Platform, Developer's System	KS8400B
Required	Channel compliance core software	AE6800C
Required	Automotive SerDes Channel Compliance Test Software	AE2010L



Keysight MIPI Solution



Thank you