

»Features

- Fast Switching Speed
- Ultra_Low RDS(ON)
- RoHS Compliant & Halogen-Free

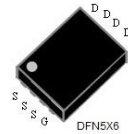
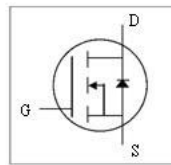
BVDSS	100V
RDS(ON) _{Typ}	4.5mΩ
I _D	85A

»Description

CT10NR005B is from Coretong innovated design and silicon process technology to achieve the lowest possible on- resistance and fast switching performance. It provides the designer with an extreme efficient device for use in a wide range of power applications.

The package is special for voltage conversion application using standard infrared reflow technique with the backside heat sink to achieve the good thermal performance.

»Schematic & PIN Configuration



PDFN5x6

»Absolute Maximum Ratings@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Rating	Units
V _{DS}	Drain-Source Voltage	100	V
V _{GS}	Gate-Source Voltage	±20	V
I _D @T _C =25°C	Drain Current, V _{GS} @ 10V	85	A
I _D @T _C =100°C	Drain Current, V _{GS} @ 10V	52	A
I _{DM}	Pulsed Drain Current ¹	140	A
P _D @T _A =25°C	Total Power Dissipation	5	W
P _D @T _C =25°C	Total Power Dissipation	85	W
P _D @T _C =100°C	Total Power Dissipation	34	W
I _{AS}	Avalanche Current, Single pulse ²	16	A
E _{AS}	Avalanche Energy, Single pulse ²	15	mJ
T _{STG}	Storage Temperature Range	-55 to 150	°C
T _J	Operating Junction Temperature Range	150	°C

»Thermal Data

Symbol	Parameter	Value	Unit
R _{thj-c}	Maximum Thermal Resistance, Junction-case	1.4	°C/W
R _{thj-a}	Maximum Thermal Resistance, Junction-ambient ₃	50	°C/W

»Electrical Characteristics@T_j=25 oC(unless otherwise specified)

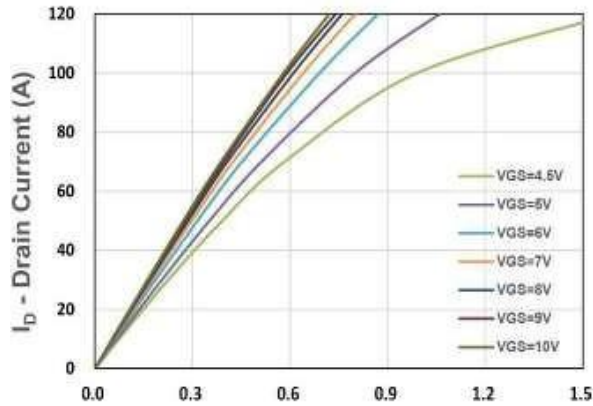
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250uA	100	-	-	V
R _{DS(ON)}	Static Drain-Source On-Resistance ₄	V _{GS} =10V, I _D =20A	-	4.6	5.5	mΩ
		V _{GS} =4.5V, I _D =10A	-	6.6	9	mΩ
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250uA	1	2	3	V
g _{fs}	Forward Transconductance	V _{DS} =5V, I _D =20A	-	45	-	S
I _{DSS}	Drain-Source Leakage Current	V _{DS} =80V, V _{GS} =0V	-	-	1	uA
I _{GSS}	Gate-Source Leakage	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
Q _g	Total Gate Charge	I _D =20A	-	71	-	nC
Q _{gs}	Gate-Source Charge	V _{DS} =50V	-	12	-	nC
Q _{gd}	Gate-Drain ("Miller") Charge	V _{GS} =10V	-	21	-	nC
t _{d(on)}	Turn-on Delay Time	V _{DS} =50V I _D =1A R _G =3Ω V _{GS} =10V	-	18	-	ns
t _r	Rise Time		-	13	-	ns
t _{d(off)}	Turn-off Delay Time		-	12	-	ns
t _f	Fall Time		-	110	-	ns
C _{iss}	Input Capacitance	V _{GS} =0V	-	4200	-	pF
C _{oss}	Output Capacitance	V _{DS} =50V	-	3200	-	pF
Crss	Reverse Transfer Capacitance	f=1.0MHz	-	1000	-	pF
R _g	Gate Resistance	f=1.0MHz	-	0.5	-	Ω

»Source-Drain Diode

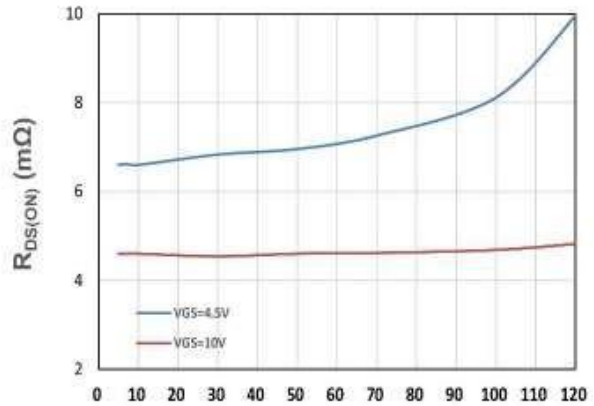
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V _{SD}	Forward On Voltage ₄	I _S =20A, V _{GS} =0V	-	0.85	1.1	V
t _{rr}	Reverse Recovery Time	I _S =20A, V _R =50V	-	56	-	ns
Q _{rr}	Reverse Recovery Charge	dI/dt=100A/μs	-	110	-	nC

Notes:

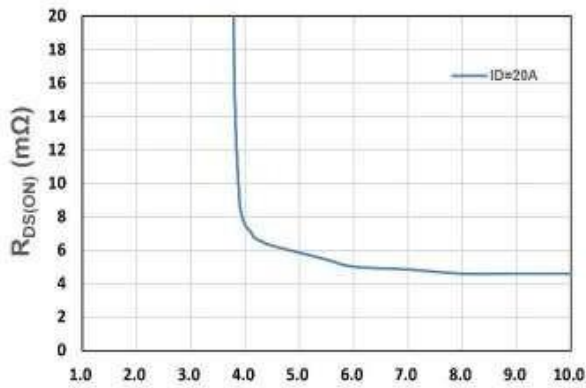
- Maximum current limited by bonding wire
- UIS tested pulse width are limited by maximum junction temperature 150°C
- Surface mounted on 1 in² 2oz copper pad of FR4 board, t <10sec ; 135oC/W when mounted on min. copper pad.



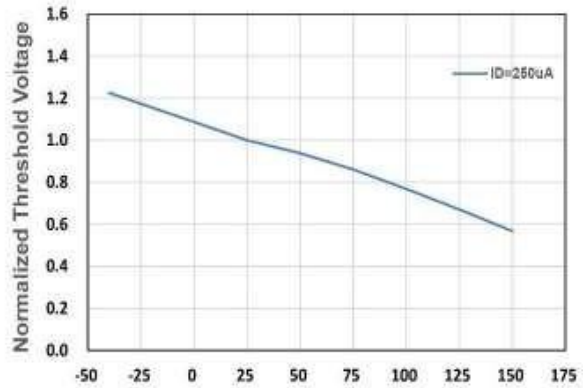
V_{DS} - Drain - Source Voltage (V)
Figure 1. Output Characteristics



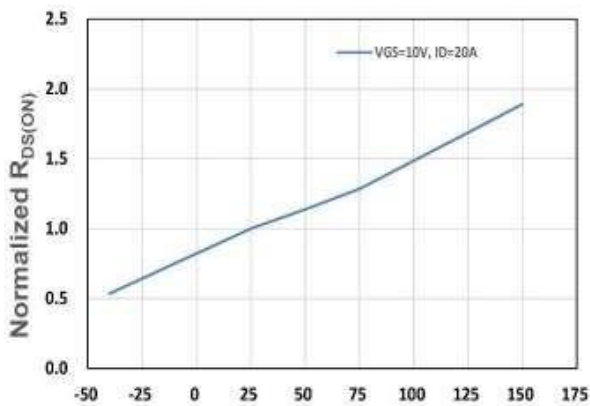
I_D - Drain Current (A)
Figure 2. On-Resistance vs. I_D



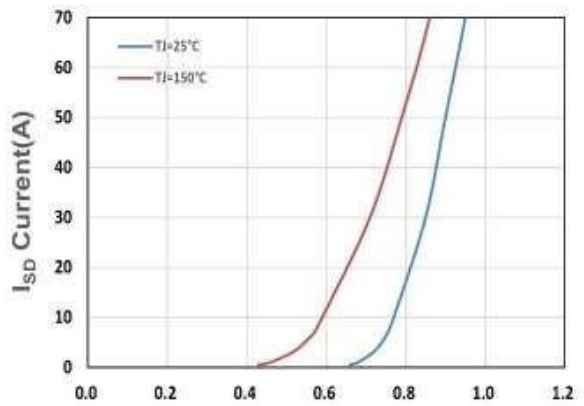
V_{GS} - Gate - Source Voltage (V)
Figure 3. On-Resistance vs. V_{GS}



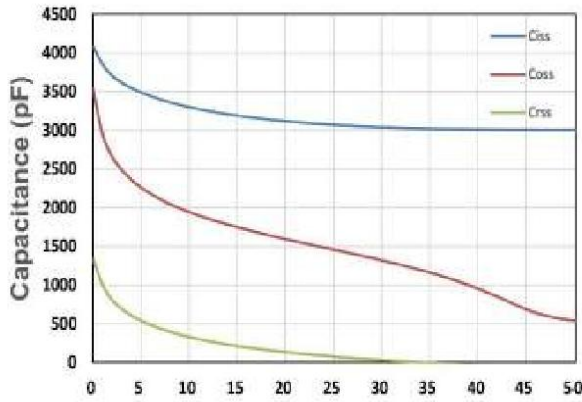
T_j , Junction Temperature($^{\circ}C$)
Figure 4. Gate Threshold Voltage



T_j , Junction Temperature($^{\circ}C$)
Figure 5. Drain-Source On Resistance

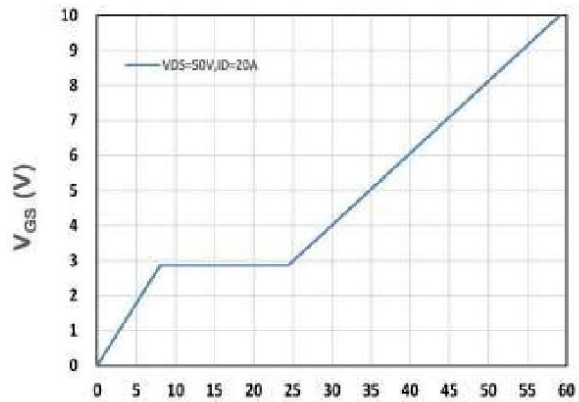


V_{SD} , Source-Drain Voltage(V)
Figure 6. Source-Drain Diode Forward



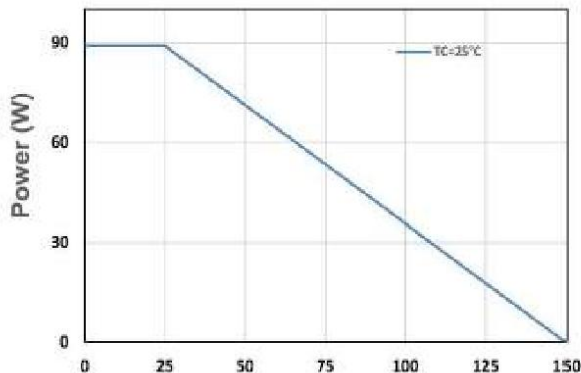
V_{DS} - Drain - Source Voltage (V)

Figure 7. Capacitance



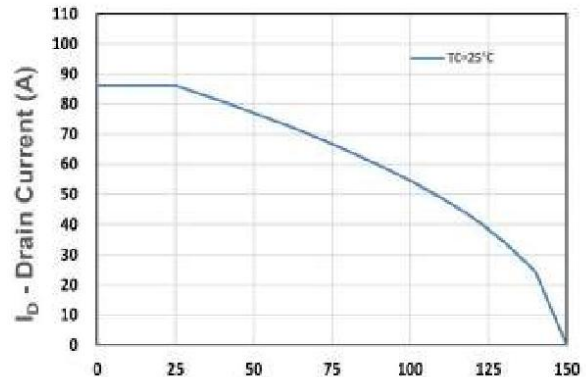
Q_g , Total Gate Charge (nC)

Figure 8. Gate Charge Characteristics



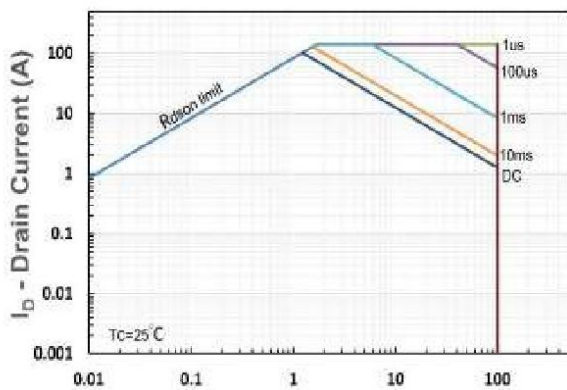
T_j - Junction Temperature (°C)

Figure 9. Power Dissipation



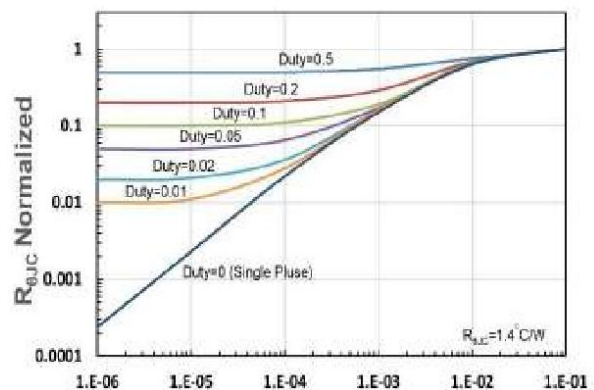
T_j - Junction Temperature (°C)

Figure 10. Drain Current



V_{DS} - Drain-Source Voltage (V)

Figure 11. Safe Operating Area



t_1 , Square Wave Pulse Duration(s)

Figure 12. $R_{\theta JC}$ Transient Thermal Impedance

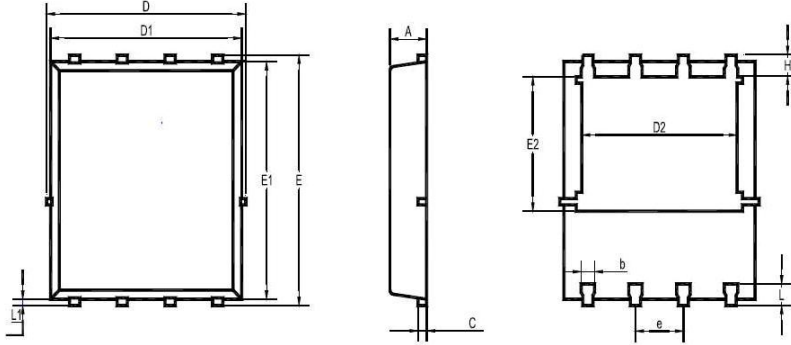
»Marking Information



Package	PDFN5x6	
XXXX	Part Number	
Y	Year	F=2020 , G=2021,
WW	Weeks	Ex. 10/27=44weeks, 11/3=45weeks
FF	Wafer lot	Lot No.
A	Serial	Serial No.
Dot	First pin	

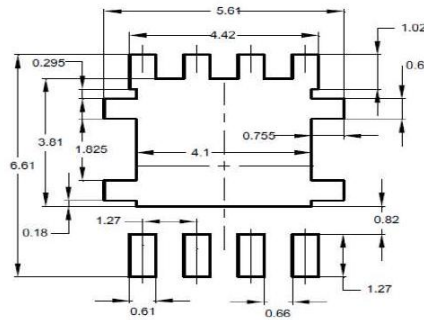
Package Outline Dimensions (Units: mm)

PDFN5x6



UNIT	A	b	C	D	D1	D2	E	E1	E2	e	L	L1	H
mm	1.12	0.51	0.34	5.26	5.1	4.5	6.25	6	3.66	1.37	0.71	0.2	0.71
	0.9	0.33	0.11	4.7	4.7	3.56	5.75	5.6	3.18	1.17	0.35	0.06	0.35

Recommended Soldering Footprint



Packing information

Package	Tape Width (mm)	Pitch		Reel Size		Per Reel Packing Quantity
		mm	inch	mm	inch	
PDFN5x6	12	8 ± 0.1	0.315 ± 0.004	330	13	5,000